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Scaling Down Effect on Low Frequency Noise in Polycrystalline Silicon Thin-Film Transistors

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ABSTRACT Scaling down effects on conduction and low frequency noise characteristics are investigated in a set of p-type polycrystalline silicon thin-film transistors (poly-Si TFTs) with fixed channel width ($W=8\ \mu\text{m}$) and different channel lengths ($L=2, 4, 8, 12,$ and $20\ \mu\text{m}$). First, short channel effects on threshold voltage, field effect mobility, and sub-threshold swing are examined, while the presence of contact may induce to the degradation of field effect mobility in the short channel devices. Subsequently, the drain current noise power spectral densities are measured at varied effective gate voltages and drain currents. The slopes of normalized noise against effective gate voltage are varied from -1.1 to -2 with decreasing channel length, which indicates that poly-Si TFTs varied from bulk dominated devices to interface dominated devices. Based on $\Delta N-\Delta\mu$ model, the flat-band voltage noise spectral density and coulomb scattering coefficient are extracted. Therefore, measured normalized noises are simulated by considering of contact resistance. Finally, short channel effects on some noise parameters (such as Hooge's parameter, etc.) are studied and discussed.

INDEX TERMS Polycrystalline silicon, thin film transistor, low frequency noise, channel length.

I. INTRODUCTION

As switching devices and peripheral circuits, low-temperature polycrystalline silicon (poly-Si) thin film transistors (TFTs) have been widely used in high-performance active-matrix flat panel displays [1], [2]. To obtain a low-temperature manufacture process and high-performance TFTs, excimer laser annealing (ELA) is proposed for achieving high-quality poly-Si layer [3]. However, this low-temperature process may induce to nonuniform and high source/drain parasitic contact resistances, which are caused by low dopant activation efficiency [3].

Low frequency noise (LFN) is essential for analog applications [4], [5] and it always sets the lower limit of the signal level which can be detected and processed in the following circuits [6]. In addition, the LFN may up-convert to high frequencies which is a considerable contributor to phase noise, and then adversely affecting the operation of poly-Si TFTs

in analog and RF applications [5], [7]. The low frequency noises in poly-Si TFTs have been measured and analyzed by many groups [8]–[12]. According to localized states in the grain boundary [13], [14], the noise levels in poly-Si TFTs are higher than those observed in crystalline silicon MOSFETs.

In order to integrate of both switching elements and driving circuits on the same substrate, the channel length of poly-Si TFTs should be reduced from typical values of $L=10\ \mu\text{m}$ to $L=1-2\ \mu\text{m}$, or less [15]. Therefore, short channel effects in scaled down poly-Si TFTs may play a significant role and it should be controlled for proper operation of these devices [15], [16]. Up till now, the effect of channel length on I-V curves and conduction parameters has been examined. However, the dependence of LFN on channel length of poly-Si TFTs has less been reported [17]. Therefore, it is helpful

TABLE 1. Conduction and noise parameters in the poly-Si TFTs with different gate lengths.

W	8				
L (μm)	2	4	8	12	20
V_{th} (V)	-3.99	-4.54	-4.24	-4.18	-4.15
μ (cm^2/Vs)	58.7	71.7	76.3	82.3	86.1
SS (V/dec)	0.30	0.31	0.30	0.30	0.35
$S_{V_{fb}}$ (V^2/Hz)	2.19×10^{-7}	1.44×10^{-7}	4.58×10^{-8}	1.95×10^{-8}	1.03×10^{-8}
$S_{R_{sd}}/R_{sd}^2$ (Hz^{-1})	1.45×10^{-8}	2.91×10^{-8}	5.82×10^{-8}	7.28×10^{-8}	1.45×10^{-7}

to study the variation of LFN with decreasing channel length.

In this paper, scaling down behaviors of poly-Si TFTs are studied with channel lengths down to 2 μm . Firstly, the electrical parameters are extracted and the degradations in device conduction performance due to contact resistances are discussed. Secondly, low frequency noise are measured in these devices. The variation of the dominant mechanism of low frequency noise with decreasing channel length is subsequently discussed. In the last, the effects of channel length on noise parameters (such as Hooge's parameter, flat-band voltage noise power spectral density) are extracted and examined.

II. DEVICE TECHNOLOGY AND EXPERIMENTAL DETAILS

The devices used in this work are p-type poly-Si TFTs with top-gate structure. Firstly, the a-Si thin film was crystallized to poly-Si thin film by ELA process. Then, the poly-Si layer was patterned into active islands by use of wet etch, followed by a 50-nm-thick SiO_2 deposition using LPCVD. This low-temperature oxide (LTO) was used as the gate dielectric. Subsequently, a 300-nm thick Al was deposited by sputtering and patterned as the gate electrode. Self-aligned source and drain regions were implanted with boron at a dose of $4 \times 10^{15}/\text{cm}^2$ and an energy of 20 keV. A 500-nm thick SiO_2 was deposited by LPCVD as the passivation layer before the contact holes were defined. A 700-nm thick Al-1% Si was sputtered and patterned as the metal leads. Finally, the devices were sintered in forming gas for 30 min at 420 $^\circ\text{C}$. The channel width (W) is about 8 μm and the channel lengths (L) are varied from 2 μm to 20 μm . The grain size of the poly-Si in this study is about 30-40 nm estimated from Scherrer equation. Thus, the devices with long channel length have more grain boundaries in the active channel as compared to those with short channel length.

The I-V measurements were performed by use of a Keysight B1500 and Cascade probe station (Summit 12000). Low frequency noises were measured by use of a Keysight E4727A LFN analyzer, which includes a dynamic signal analyzer, filters and amplifiers [4].

III. CONDUCTION CHARACTERISTICS

The transfer characteristics of p-type poly-Si TFTs with varied channel lengths are plotted in Fig. 1. The conduction parameters (threshold voltage, field effect mobility and sub-threshold swing) are listed in Table 1, which are extracted at $V_{ds} = 0.1$ V.

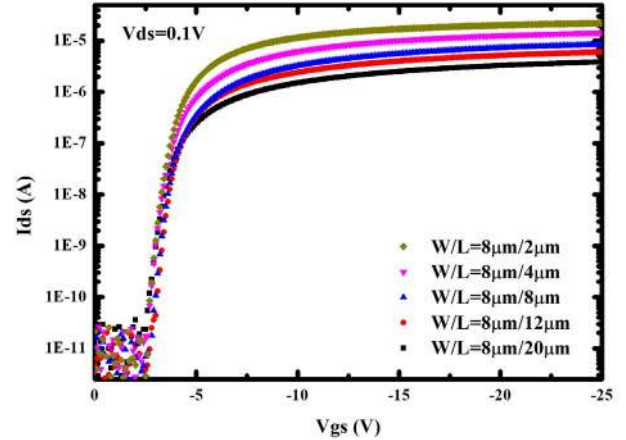


FIGURE 1. Measured $I_{ds} - V_{gs}$ curves in the p-type poly-Si TFTs with varied channel length.

As shown in Table 1, a little variation of threshold voltage (V_{th}) with decreasing channel length was observed in these devices. It implies carrier diffusion effects from doped source/drain to the channel can be neglected in our devices, which always induce the variation of threshold voltage in the short channel devices [18], [19]. Moreover, the extracted sub-threshold swing (SS) values from transfer curves keep the range of 0.3-0.35 V/dec, which suggests that the localized states existed in the Si/ SiO_2 interface are very similar in the poly-Si TFTs with different channel lengths.

The degradation of extracted field effect mobility is caused by the presence of parasitic source/drain (S/D) contact resistances in series to the channel resistance [3], [20]. In the long channel poly-Si TFTs, channel resistance ($R_{channel}$) is much greater than the S/D contact resistance (R_{sd}), and the field effect mobility is less dependent on the contact resistance. However, with decreasing channel length, the electrical performance of poly-Si TFTs would be seriously affected by contact resistance and the field effect mobility would be degraded significantly [3].

To examine the effect of parasitic resistance on conduction and noise performance, the contact resistance was extracted by the transmission line method [21], as shown in Fig. 2(a). When $V_{ds} = 0.1$ V, the extracted contact resistance is about 4.32 k Ω at $V_{gs} - V_{th} = -4$ V and is about 2.62 k Ω at $V_{gs} - V_{th} = -8$ V. Extracted contact resistance exhibits slightly $V_{gs} - V_{th}$ dependence, which can be expressed by [22], [23]

$$R_{sd}(V_{gs}) = R_{sd0}(V_{gs} - V_{th})^{-\beta} \quad (1)$$

In this work, R_{sd0} is about 38.65 k Ω and β is about 1.57.

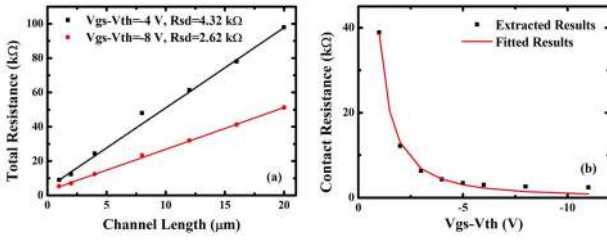


FIGURE 2. (a) Total resistance versus channel length, (b) contact resistance versus $V_{gs} - V_{th}$ in poly-Si TFTs.

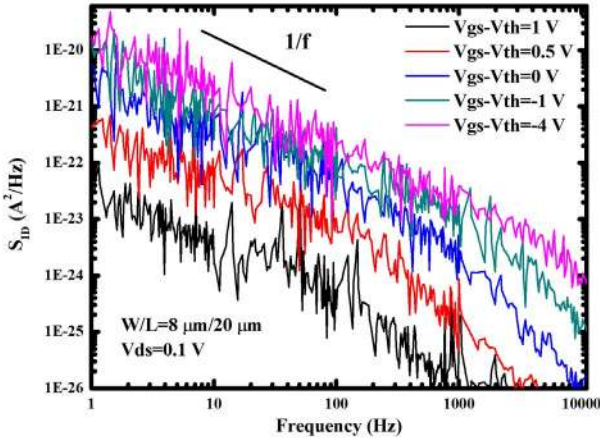


FIGURE 3. Drain current noise power spectral densities versus frequency in the poly-Si TFTs, measured at different gate voltages.

IV. LOW FREQUENCY NOISE CHARACTERISTICS

To examine the dependence of low frequency noise on channel length, the typical low frequency noise characteristics are plotted in Fig. 3, evaluated at different gate voltages in the poly-Si TFTs with $W/L=8 \mu\text{m}/20 \mu\text{m}$. The drain current noise power spectrum densities (S_{ID}) clearly show a pure $1/f$ -type spectrum. This phenomenon suggests that the trap density is uniform in depth from the Si/SiO₂ interface to the interior of the gate oxide [24].

To determine the origin of low frequency noise, there are two principal mechanisms: carrier number fluctuation (ΔN) theory and mobility fluctuation ($\Delta\mu$) theory. In the classic ΔN theory (McWhorter model), the drain current fluctuation are induced by the fluctuations of interfacial charges, which are related to the trapping and de-trapping processes of free carriers into localized states in the grain boundary and border traps in the gate oxide. Thus, the normalized drain current noises (S_{ID}/I_{ds}^2) can be expressed by [4], [14]

$$\frac{S_{ID}}{I_{ds}^2} = \frac{k^*}{fC_{ox}WL(V_{gs} - V_{th})^2} \quad (2)$$

where C_{ox} is the gate oxide capacitance per unit area, K^* is a fitting parameter which considering the carrier tunneling process between the channel and gate oxide traps [14].

In the opposite of ΔN theory, Hooge suggested the $1/f$ noise may arises from noise in lattice scattering, which in turn causes random mobility fluctuation [25], [26].

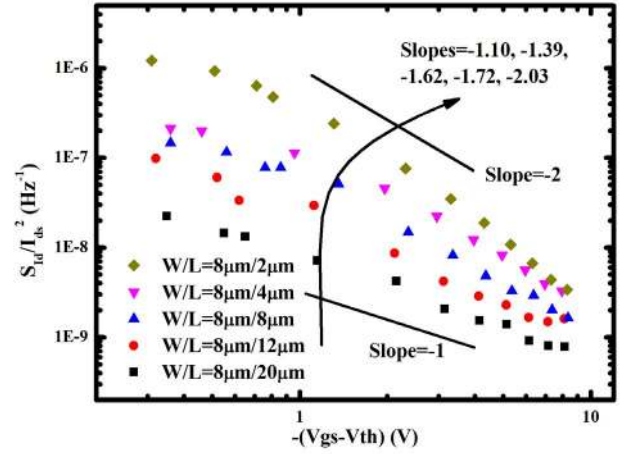


FIGURE 4. Normalized drain current noise versus $V_{gs} - V_{th}$ for poly-Si TFTs with different channel lengths ($f=10$ Hz).

According to Hooges empirical $\Delta\mu$ relationship, S_{ID}/I_{ds}^2 can be expressed by [14], [26]

$$\frac{S_{ID}}{I_{ds}^2} = \frac{\alpha_H}{N_{tot}f} = \frac{\alpha_H q}{fC_{ox}WL(V_{gs} - V_{th})} \quad (3)$$

where α_H is Hooges empirical parameter and strongly dependent on the technology and material. N_{tot} is the total number of free charge carriers in the channel.

According to Eq. (2) and (3), the normalized current noise has the power law dependence with the effective gate voltage ($V_{gs}-V_{th}$). The normalized current noises versus $V_{gs}-V_{th}$ are shown in the Fig. 4, and the extracted power law coefficients are in the range of -1 and -2 . In the long channel devices, the slopes of $\log(S_{ID}/I_{ds}^2) - \log(V_{gs} - V_{th})$ are close to -1 which are expected to be dominated by $\Delta\mu$ theory. However, the slopes in short channel devices are close to -2 which are expected to be dominated by ΔN theory.

As shown in Fig. 4, the reduction of channel length may lead to a modification of the slope of S_{ID}/I_{ds}^2 against $V_{gs}-V_{th}$ from -1 to -2 . These phenomena may be caused by the variation of the origin of flicker noise [4], [14], [27]. The presence of bulk defects in the grain boundary is essential in long channel devices, and it may push the bulk effect noise to be the predominant origin of the whole noise. However, in the short channel devices, the quality of Si/SiO₂ interface is crucial, and the carrier number fluctuation induced by trapping/detrapping of free carriers becomes more important [4], [14], [27]. Thus, poly-Si TFTs may be varied from bulk dominated devices to interface dominated devices with decreasing channel length. Moreover, the improvement of crystal quality in the short channel devices may also be an occasion of this phenomenon [27]. The above findings may result in the modification of the law followed by S_{ID}/I_{ds}^2 against $V_{gs} - V_{th}$ with decreasing channel length.

As plotted in Fig. 4, the slopes of S_{ID}/I_{ds}^2 against $V_{gs} - V_{th}$ are in the range of -1 and -2 . Therefore, these phenomena can be modeled and described by use of the

carrier number with correlated mobility fluctuations (ΔN - $\Delta\mu$) model [14], [28], [29]. According to ΔN - $\Delta\mu$ model, the fluctuation of interfacial charges may lead to a supplementary change of the mobility which induces an extra drain current fluctuation. Thus, the drain current noise can be evaluated as [14], [28], [29]

$$\frac{S_{ID}}{I_{ds}^2} = (1 \pm \alpha_c \mu_{eff} C_{ox} I_{ds} / g_m) \left(\frac{g_m}{I_{ds}} \right)^2 \cdot S_{vfb} \quad (4)$$

where g_m is the device transconductance, α_c is a fitting parameter which may relate to the coulomb scattering. A high value of α_c means more sensitivity of the mobility to the insulator charge [4], [28]. For a pure ΔN model, $\alpha_c \approx 0$. S_{vfb} is the flat-band voltage noise power spectral density which can be calculated by [29]

$$S_{vfb} = \frac{q^2 K T \lambda N_t}{W L C_{ox}^2 f \gamma} \quad (5)$$

where λ is the tunneling attenuation coefficient, which is about 0.1 nm for SiO₂. N_t is the trap density near the SiO₂/Si interface.

In the linear region, the gate voltage noise spectral density (S_{vg}) can be expressed by [28], [30]

$$S_{vg} = \frac{S_{ID}}{g_m^2} = S_{vfb} [1 \pm \alpha_c \mu_{eff} C_{ox} (V_{gs} - V_{th})]^2 \quad (6)$$

In order to find the value of α_c and S_{vfb} in the Eq. (4), the extra mobility fluctuations due to the change in the scattering rate induced by the interface charge fluctuations are examined according to Eq. (6). Fig. 5 shows the variations of $S_{vg}^{1/2}$ as a function of $V_{gs} - V_{th}$ in the poly-Si TFTs with varied channel lengths. In strong inversion conditions, $S_{vg}^{1/2}$ changes linearly with $V_{gs} - V_{th}$, thus S_{vg} has a parabolic dependence on the gate voltage which varying superlinearly with $V_{gs} - V_{th}$. This behavior can be attributed to Hooge's equation. However, the plateau of noise in the weak inversion can be due to trapping noise model. To take account these two effects, ΔN - $\Delta\mu$ model may be most appropriate to explain the above phenomena [30]. Based on Eq. (6) and Fig. 5, the S_{vfb} values can be extracted, as shown in the Table 1. The value of S_{vfb} approximately linear increases with decreasing channel length, which is conform to the prediction of Eq. (5).

In addition, the variation slopes of S_{vg} with the gate voltage are dependent on the channel length and channel width [28], [30]. Thus, the variation rate may increase as the channel length is decreased. Similar behaviors are also reported in MOSFETs [28], [30] and IZO TFTs [4].

According to Eq. (6), the scattering parameters α_c can be extracted from the slopes of $S_{vg}^{1/2}$ - $V_{gs} - V_{th}$ curves in the strong inversion. As a result, the values of α_c are in the range of 1.55×10^4 and 3.21×10^4 Vs/C which decrease with the decrement of channel length. As discussed above, the flicker noises in the short channel devices are dominated by carrier number fluctuation, and then induce to the decrement of extracted α_c .

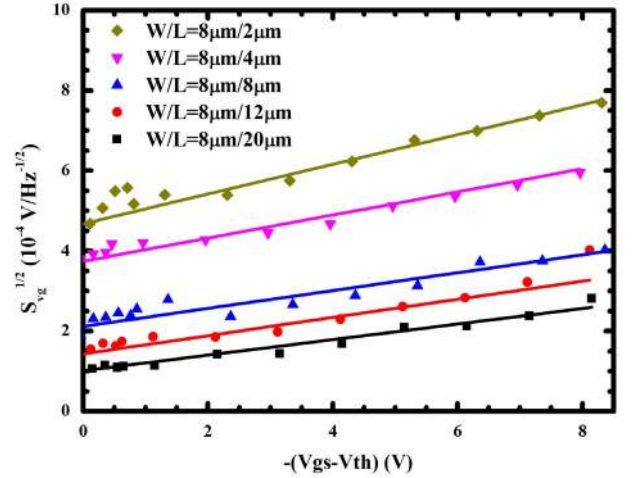


FIGURE 5. Variation of the root square gate voltage noise spectral density with the effective gate voltage in the Poly-Si TFT. The continuous lines are fit to (1) $\alpha_c = 3.21 \times 10^4$ Vs/C ($L=20 \mu\text{m}$); (2) $\alpha_c = 2.79 \times 10^4$ Vs/C ($L=12 \mu\text{m}$); (3) $\alpha_c = 1.99 \times 10^4$ Vs/C ($L=8 \mu\text{m}$); (4) $\alpha_c = 1.55 \times 10^4$ Vs/C ($L=4 \mu\text{m}$); (5) $\alpha_c = 1.94 \times 10^4$ Vs/C ($L=2 \mu\text{m}$).

The normalized drain current noises versus drain current are shown in Fig. 6. Based on ΔN - $\Delta\mu$ model, the measured noises in the linear region can be simulated, and in good agreement with the simulating results by use of the above extracted parameters, as shown by dash lines in Fig. 6. However, under higher drain current intensities, discrepancies occur between measured results and fitting results. This phenomenon is the result of the contribution of the contact resistance.

As reported, both of the channel and contact may contribute to low frequency noise. Thus, the total noise is the total of the channel noise and contact noise [22], [23], [31]. The measured noises are dominated by the channel under low current intensities and dominated by the contact under high current intensities. By considering contact resistance, the noise can be calculated by [22], [23], [31]

$$\frac{S_{ID,R}}{I_{ds}^2} = \frac{S_{ID}}{I_{ds}^2} + \left(\frac{I_{ds}}{V_{ds}} \right)^2 \frac{S_{Rsd}}{R_{sd}^2} R_{sd}^2 \quad (7)$$

here S_{Rsd}/R_{sd}^2 is the normalized noise power spectral density of the contact resistance. Based on Eq. (7), the measured noise can be approximated under high current intensities, as shown by solid lines in Fig. 6.

As shown in Table 1, S_{Rsd}/R_{sd}^2 may decrease linearly with the decreasing channel length. Under high current intensities, contact may play a key role and its related noise can be calculated by an empirical model [23], [28]

$$S_{Rsd}/R_{sd}^2 = \alpha_H / W L f N \propto 1/I_{ds} \propto L \quad (8)$$

Thus, the scaling of S_{Rsd}/R_{sd}^2 with channel length is consistent with Eq. (7). Similar results have also been reported in OTFTs [23] and ITZO TFTs [22]. As reported [32], the

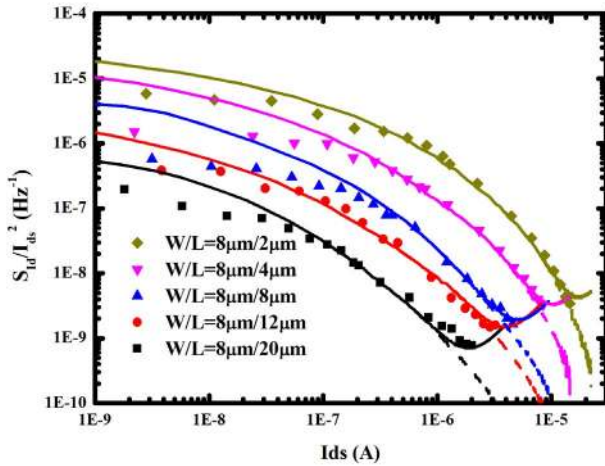


FIGURE 6. Normalized current noises versus drain current in the ohmic region ($f=10$ Hz). (Dots: Measured results, Solid Lines: With contact resistance, Dash Lines: Without contact resistance.)

contact resistance noise may also contribute to the total resistance noise which cannot be neglected in the TFTs with longer channel lengths ($100 \mu\text{m}$ or more longer).

To evaluate the quality of these devices, α_H can be calculated from measured noises in the above threshold region. Based on Eq. (3), α_H can be expressed by

$$\alpha_H = \left(\frac{S_{ID}}{I_{ds}^2} \right) \frac{fWLC_{ox}}{q} (V_{gs} - V_{th}) \quad (9)$$

As shown in Fig. 7, the extracted α_H keeps nearly a constant in the long channel poly-Si TFTs, which indicate the noises are dominated by the mobility fluctuation mechanism. However, the extracted α_H decreases with increasing $V_{gs} - V_{th}$ in the short channel devices, which indicates the noises are dominated by the number fluctuation mechanism. These phenomena are consistent with the above analysis and discussions. Moreover, the inaccuracy of the extracted V_{th} may result in an increment of α_H under low $V_{gs} - V_{th}$.

The average α_H are about 4.99×10^{-2} , 7.74×10^{-2} , 10.64×10^{-2} , 8.42×10^{-2} and 14.64×10^{-2} respectively. With the decrement of channel length, the flicker noise may be more dependent on the quality of the Si/SiO₂ interface and the S/D contact. It may results in the increment of α_H with the decrement of channel length. The average α_H can be further decreased by the improved of fabrication processes.

As reported in the BSIM3 noise model [14], [33], with a small V_{ds} , the measured noise in the linear region can be approximated by following Hooge's theory [34], [35]

$$\begin{aligned} S_{ID}(f) &= \frac{KT\mu_{eff}I_{ds}}{C_{ox}L_{eff}^2fEF} V_{ds}C_{ox} \cdot NOIB \\ &= \frac{KT\mu_{eff}^2W_{eff}C_{ox}V_{ds}^2}{L_{eff}^3fEF} (V_{gs} - V_{th}) \cdot NOIB \quad (10) \end{aligned}$$

here, $NOIB$ is a noise fitting parameter, which can be calculated by $NOIB = q\alpha_H/KT$.

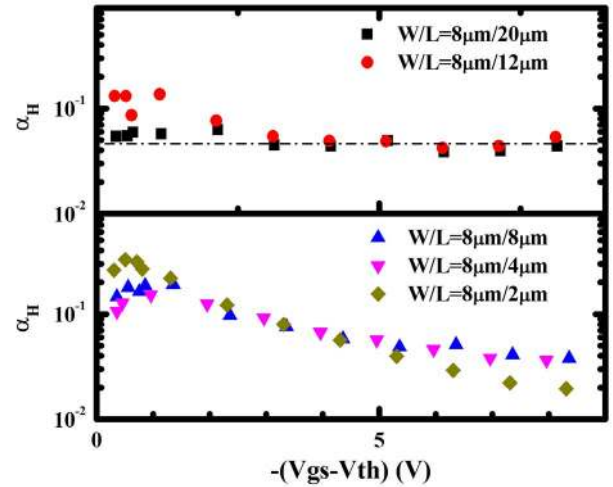


FIGURE 7. Extracted Hooge's parameters (α_H) versus $V_{gs} - V_{th}$ in the linear region for poly-Si TFT with five channel lengths.

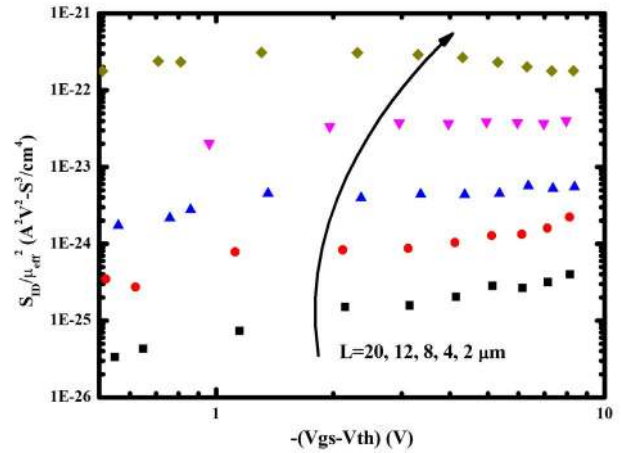


FIGURE 8. Typical evolutions of S_{ID}/μ_{eff}^2 in the ohmic region, versus the effective gate voltage ($f=10$ Hz).

As discussed above, low frequency noises in the long channel devices are dominated by mobility fluctuation model, thus α_H and $NOIB$ may independent of $V_{gs} - V_{th}$. According to Eq. (10), S_{ID}/μ_{eff}^2 may increase with the increment of $V_{gs} - V_{th}$ in the long channel devices ($L=12, 20 \mu\text{m}$). This phenomenon is in agreement with the measured results which plotted in the Fig. 8. However, low frequency noises in the short channel devices are dominated by number fluctuation model, thus α_H and $NOIB$ may decrease with the increment of effective gate voltage. Therefore, S_{ID}/μ_{eff}^2 may keeps nearly a constant in the short channel devices ($L=2, 4, 8 \mu\text{m}$).

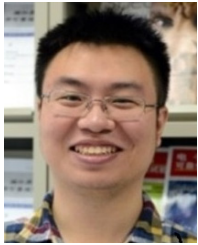
V. CONCLUSION

The scaling down effects on conduction and low frequency noise characteristics in the poly-Si TFTs are examined. The dependence of threshold voltage, sub-threshold swing and field effect on channel length is investigated. The presence

of parasitic S/D contact resistances may induce the degradation of extracted field effect mobility. In addition, measured low frequency noises show a pure $1/f$ type spectrum. The measured results indicate that flicker noises are dominated by the mobility fluctuation mechanism in the long channel devices, which are dominated by the number fluctuation mechanism in the short channel devices. By use of $\Delta N - \Delta \mu$ model, some noise parameters (S_{vfb} , α_c) are extracted and then the measured noises are simulated. Finally, the variations of α_H and S_{ID}/μ_{eff}^2 with the effective gate voltages are discussed.

REFERENCES

- [1] S. Deng *et al.*, "Fabrication of high-performance bridged-grain polycrystalline silicon TFTs by laser interference lithography," *IEEE Trans. Electron Devices*, vol. 63, no. 3, pp. 1085–1090, Mar. 2016, doi: [10.1109/TED.2016.2520081](https://doi.org/10.1109/TED.2016.2520081).
- [2] L. Maiolo *et al.*, "Flexible sensing systems based on polysilicon thin film transistors technology," *Sensor Actuators B Chem.*, vol. 179, pp. 114–124, Mar. 2013, doi: [10.1016/j.snb.2012.10.093](https://doi.org/10.1016/j.snb.2012.10.093).
- [3] N. V. Duy *et al.*, "Effect of series resistance on field effect mobility at varying channel lengths and investigation into the enhancement of source/drain metallized thin-film transistor characteristics," *Jpn. J. Appl. Phys.*, vol. 50, no. 2R, Feb. 2011, Art. no. 024101, doi: [10.1143/JJAP.50.024101](https://doi.org/10.1143/JJAP.50.024101).
- [4] Y. Liu *et al.*, "Analysis and simulation of low-frequency noise in indium-zinc-oxide thin-film transistors," *IEEE J. Electron Devices Soc.*, vol. 6, no. 1, pp. 271–279, Dec. 2018, doi: [10.1109/jeds.2018.2800049](https://doi.org/10.1109/jeds.2018.2800049).
- [5] A. Jerng and C. G. Sodini, "The impact of devices type and size on phase noise mechanisms," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 360–369, Feb. 2005, doi: [10.1109/JSSC.2004.841035](https://doi.org/10.1109/JSSC.2004.841035).
- [6] T. Noulis, S. Siskos, and G. Sarraayrouse, "Analysis and selection criteria of BSIM4 flicker noise simulation models," *Int. J. Circuit Theory Appl.*, vol. 36, no. 7, pp. 813–823, Oct. 2008, doi: [10.1002/cta.461](https://doi.org/10.1002/cta.461).
- [7] Y. Liu *et al.*, "Low-frequency noise characteristics in the MOSFETs processed in 65 nm technology," *J. Semicond.*, vol. 37, no. 6, Jun. 2016, Art. no. 064012, doi: [10.1088/1674-4926/37/6/064012](https://doi.org/10.1088/1674-4926/37/6/064012).
- [8] C. A. Dimitriadis, G. Kamarinos, and J. Brini, "Model of low frequency noise in polycrystalline silicon thin-film transistors," *IEEE Electron Device Lett.*, vol. 22, no. 8, pp. 381–383, Aug. 2001, doi: [10.1109/55.936350](https://doi.org/10.1109/55.936350).
- [9] M. X. Wang and M. Wang, "A new model for the $1/f$ noise of polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 61, no. 9, pp. 3258–3264, Sep. 2014, doi: [10.1109/TED.2014.2336250](https://doi.org/10.1109/TED.2014.2336250).
- [10] M. Behravan and D. T. Story, " $1/f$ noise characterization of n- and p-type polycrystalline-silicon thin-film transistors," *IEEE Trans. Device Mater. Rel.*, vol. 9, no. 3, pp. 372–378, Sep. 2009, doi: [10.1109/TDMR.2009.2023080](https://doi.org/10.1109/TDMR.2009.2023080).
- [11] Y. Liu, Y.-F. En, and W.-X. Fang, "Analysis of low frequency noise characteristics in p-type polycrystalline silicon thin film transistors," *Mod. Phys. Lett. B*, vol. 31, nos. 19–21, Jul. 2017, Art. no. 1740020, doi: [10.1142/S0217984917400206](https://doi.org/10.1142/S0217984917400206).
- [12] L. Pichon, A. Boukhenoufa, B. Cretu, and R. Rogel, "Improvement in the determination by $1/f$ noise measurements of the interface state distribution in polysilicon thin film transistors in relation with the compensation law of Meyer Neldel," *J. Appl. Phys.*, vol. 105, no. 10, May 2009, Art. no. 104503, doi: [10.1063/1.3126706](https://doi.org/10.1063/1.3126706).
- [13] C. A. Dimitriadis, F. V. Farmakis, G. Kamarinos, and J. Brini, "Origin of low-frequency noise in polycrystalline silicon thin-film transistors," *J. Appl. Phys.*, vol. 91, no. 12, pp. 9919–9923, Jun. 2002, doi: [10.1063/1.1481964](https://doi.org/10.1063/1.1481964).
- [14] D. Rigaud, M. Valenza, and J. Rhayem, "Low frequency noise in thin film transistors," *IET Proc. Circuits Devices Syst.*, vol. 149, no. 1, pp. 75–82, Feb. 2002, doi: [10.1049/ip-cds:20020063](https://doi.org/10.1049/ip-cds:20020063).
- [15] G. Fortunato, A. Valletta, P. Gaucci, L. Mariucci, and S. D. Brotherton, "Short channel effects in polysilicon thin film transistors," *Thin Solid Films*, vol. 487, nos. 1–2, pp. 221–226, Sep. 2005, doi: [10.1016/j.tsf.2005.01.069](https://doi.org/10.1016/j.tsf.2005.01.069).
- [16] J.-T. Lin and Y.-C. Eng, "A novel blocking technology for improving the short-channel effects in polycrystalline silicon TFT devices," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3238–3244, Dec. 2007, doi: [10.1109/TED.2007.908893](https://doi.org/10.1109/TED.2007.908893).
- [17] C. T. Angelis *et al.*, "Dimension scaling of low frequency noise in the drain current of polycrystalline silicon thin-film transistors," *J. Appl. Phys.*, vol. 86, no. 12, pp. 7083–7086, Dec. 1999, doi: [10.1063/1.371721](https://doi.org/10.1063/1.371721).
- [18] A. Valletta *et al.*, "Threshold voltage in short channel polycrystalline silicon thin film transistors: Influence of drain induced barrier lowering and floating body effects," *J. Appl. Phys.*, vol. 107, no. 7, Apr. 2010, Art. no. 074505, doi: [10.1063/1.3359649](https://doi.org/10.1063/1.3359649).
- [19] D. H. Kang, J. U. Han, M. Mativenga, S. H. Ha, and J. Jang, "Threshold voltage dependence on channel length in amorphous-indium-gallium-zinc-oxide thin-film transistors," *Appl. Phys. Lett.*, vol. 102, no. 8, Feb. 2013, Art. no. 083508, doi: [10.1063/1.4793996](https://doi.org/10.1063/1.4793996).
- [20] Y. Liu, R.-H. Yao, and B. Li, "A physical model with the effects of self-heating and variable resistance in above-threshold region for hydrogenated amorphous silicon thin film transistor," *Jpn. J. Appl. Phys.*, vol. 47, no. 6, pp. 4436–4440, Jun. 2008, doi: [10.1143/JJAP.47.4436](https://doi.org/10.1143/JJAP.47.4436).
- [21] Y. Xu, T. Minari, K. Tsukagoshi, J. A. Chroboczek, and G. Ghibaudo, "Direct evaluation of low-field mobility and access resistance in pentacene field-effect transistors," *J. Appl. Phys.*, vol. 107, no. 11, Jun. 2010, Art. no. 114507, doi: [10.1063/1.3432716](https://doi.org/10.1063/1.3432716).
- [22] Y. Liu *et al.*, "Low frequency noise in hybrid-phase-microstructure ITO-stabilized ZnO thin film transistors," *IEEE Electron Device Lett.*, vol. 39, no. 2, pp. 200–203, Feb. 2018, doi: [10.1109/LED.2017.2784844](https://doi.org/10.1109/LED.2017.2784844).
- [23] Y. Xu *et al.*, "Origin of low-frequency noise in pentacene field-effect transistors," *Solid-State Electron.*, vol. 61, no. 1, pp. 106–110, Jul. 2011, doi: [10.1016/j.sse.2011.01.002](https://doi.org/10.1016/j.sse.2011.01.002).
- [24] R. Jayaraman and C. G. Sodini, "A $1/f$ noise technique to extract the oxide trap density near the conduction band edge of silicon," *IEEE Trans. Electron Devices*, vol. 36, no. 9, pp. 1773–1782, Sep. 1989, doi: [10.1109/16.34242](https://doi.org/10.1109/16.34242).
- [25] T.-C. Fung, G. Baek, and J. Kanicki, "Low frequency noise in long channel amorphous In-Ga-Zn-O thin film transistors," *J. Appl. Phys.*, vol. 108, no. 7, Oct. 2010, Art. no. 074518, doi: [10.1063/1.3490193](https://doi.org/10.1063/1.3490193).
- [26] F. N. Hooge, " $1/f$ noise sources," *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 1926–1935, Nov. 1994, doi: [10.1109/16.333808](https://doi.org/10.1109/16.333808).
- [27] K.-S. Jeong *et al.*, "Crystal quality effect on low-frequency noise in ZnO TFTs," *IEEE Electron Device Lett.*, vol. 32, no. 12, pp. 1701–1703, Dec. 2011, doi: [10.1109/LED.2011.2167312](https://doi.org/10.1109/LED.2011.2167312).
- [28] G. Ghibaudo, O. Roux, C. Nguyenduc, F. Balestra, and J. Brini, "Improved analysis of low frequency noise in field-effect MOS transistors," *Phys. Status Solidi A*, vol. 124, no. 2, pp. 571–581, Apr. 1991, doi: [10.1002/pssa.2211240225](https://doi.org/10.1002/pssa.2211240225).
- [29] C. A. Dimitriadis, J. Brini, and G. Kamarinos, "Origin of low-frequency noise in polycrystalline silicon thin-film transistors," *Thin Solid Films*, vol. 427, nos. 1–2, pp. 113–116, Mar. 2003, doi: [10.1016/S0040-6090\(02\)01153-7](https://doi.org/10.1016/S0040-6090(02)01153-7).
- [30] T. Boutchacha, G. Ghibaudo, and B. Belmekki, "Study of low frequency noise in the 0.18 μm silicon CMOS transistors," in *Proc. Int. Conf. Microelectron. Test Struct.*, Goteborg, Sweden, 1999, pp. 84–88, doi: [10.1109/Icmts.1999.766221](https://doi.org/10.1109/Icmts.1999.766221).
- [31] H. He, X. Zheng, and S. Zhang, "Above-threshold $1/f$ noise expression for amorphous InGaZnO thin-film transistors considering series resistance noise," *IEEE Electron Device Lett.*, vol. 36, no. 10, pp. 1056–1058, Oct. 2015, doi: [10.1109/LED.2015.2469723](https://doi.org/10.1109/LED.2015.2469723).
- [32] Y. Xu *et al.*, "Extraction of low-frequency noise in contact resistance of organic field-effect transistors," *Appl. Phys. Lett.*, vol. 97, no. 3, Jul. 2010, Art. no. 033503, doi: [10.1063/1.3467057](https://doi.org/10.1063/1.3467057).
- [33] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "A physics-based MOSFET noise model for circuit simulators," *IEEE Trans. Electron Devices*, vol. 37, no. 5, pp. 1323–1333, May 1990, doi: [10.1109/16.108195](https://doi.org/10.1109/16.108195).
- [34] J. C. Vildeuil, M. Valenza, and D. Rigaud, "Extraction of the BSIM3 $1/f$ noise parameters in CMOS transistors," *Microelectron. J.*, vol. 30, no. 2, pp. 199–205, Feb. 1999, doi: [10.1016/S0026-2692\(98\)00108-6](https://doi.org/10.1016/S0026-2692(98)00108-6).
- [35] Y. Akue Allogo *et al.*, " $1/f$ noise measurements in n-channel MOSFETs processed in 0.25 μm technology," *Solid-State Electron.*, vol. 46, no. 3, pp. 361–366, Mar. 2002, doi: [10.1016/S0038-1101\(01\)00109-5](https://doi.org/10.1016/S0038-1101(01)00109-5).



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