Scaling in quantum transport in silicon nano-transistors

Online: 2009-10-28

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Keywords: Nano-transistor, scaling, quantum transport

We develop a theory for scaling properties of quantum transport in nano-field effect transistors. Our starting point is a one-dimensional effective expression for the drain current in the Landauer-Büttiker formalism. Assuming a relatively simple total potential acting on the electrons the effective theory can be reduced to a scale-invariant form yielding a set of dimensionless control parameters. Among these control parameters are the characteristic length l and -width w of the electron channel which are its physical length and -width in units of the scaling length $\lambda = \hbar (2m^* \varepsilon_F)^{-1/2}$. Here ε_F is the Fermi energy in the source contact and m^* is the effective mass in the electron channel. In the limit of wide transistors and low temperatures we evaluate the scale-invariant i-v characteristics as a function of the characteristic length. In the strong barrier regime, i. e. for $l \ge 20$ long-channel behavior is found. At weaker barriers source-drain tunneling leads to increasingly significant deviations from the longchannel behavior.

Introduction

The transistor density doubles every two years (Moore's law). Increased mobility in the transistor channel leads to higher performance and less energy consumption.

The size reduction in nano-FETs renders possible the application of new material systems in silicon based technology. Examples are the use of strained silicon with increased germanium fraction and Si-Ge closer to the channel. Beyond ~ 30 nm new options and challenges arise[1]: Substrat engineering (110) vs (100) orientation plus increased p-channel mobility, multi-gate FET's and high-µ material (Ge, compound materials). The shift from micrometer – to nanometer device dimensions is associated with a shift in the fundamental transport mechanisms. At the envisaged channel lengths of less than thirty nanometers it is to be expected that quantum transport will play an increasingly important role.

In view of this trend we develop a theory for the scaling properties of quantum transport in silicon nano-transistors. As well-known, with decreasing channel length the desired long-channel behavior of a transistor is degraded by short-channel effects [2, 3]. One major source of these short-channel effects is the multi-dimensional nature of the electrostatic field which causes a reduction of the gate voltage control over a short electron channel. A second source is the advent of quantum transport where, for example, source-drain tunneling prevents the transistor to assume a clear off-state. In early scaling concepts long-channel behavior could be assumed [4, 5]. With progressive miniaturization twodimensional effects in the electric field have been introduced in scaling [6, 7]. Here the electrostatic problem with two essential dimensions was approximated by a one-dimensional effective one in which the proper length scale λ results naturally.

We start from a one-dimensional effective model assuming ballistic transport (for a review see Ref. [9] and more recently Ref. [10]). We demonstrate that in such a relatively simple ballistiic approach the iv characteristics can be cast in a scale-invariant form, in which, similar to the case of the electrostatic problem, a scaling length can be defined. In quantum transport one obtains $\lambda = \hbar / \sqrt{2m^* \varepsilon_F}$, where $\varepsilon_{\scriptscriptstyle F}$ is the Fermi energy in the source contact and is the effective mass of the carriers. In the limit of wide transistors and low temperatures we evaluate the scale-invariant i-v characteristics as a function of the characteristic length $l = L/\lambda$ where L ist the physical length of the transistor channel. In the strong barrier regime, i. e. for $l \ge 20$ long-channel behavior is found. At weaker barriers source-drain tunneling leads to increasingly significant deviations from the long-channel behavior.

Theory

We consider a generic field effect transistor as illustrated in Fig. 1 for which a one-dimensional effective model we write for the drain current

$$I = \frac{2e}{h} \int_{0}^{\infty} d\varepsilon \left[S(\varepsilon - \mu) - S(\varepsilon - \mu + V_{D}) \right] \tilde{T}^{eff}(\varepsilon), \tag{1}$$

with $V_D = eU_D$ where U_D is the applied drain voltage. In a wide transistor the supply function S takes the form [10]

$$S(x) = \sqrt{\frac{m * k_B T}{2\pi \hbar^2}} W F_{-1/2} \left(-\frac{x}{k_B T} \right), \tag{2}$$

where $F_{-1/2}$ is the Fermi-Dirac integral of order -1/2, W is the width of the transistor, and μ is the chemical potential in the source contact.

Furthermore, $\tilde{T}^{eff} = k_D^{eff} \left| t^S \right|^2 \left(k_S^{eff} \right)^{-1}$ is the one-dimensional effective current transmission.

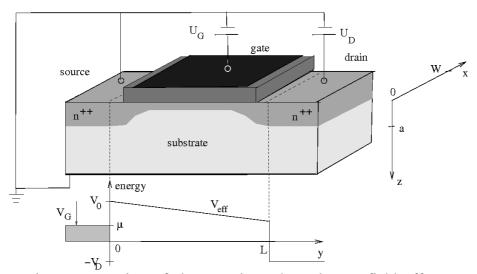


Figure 1: Schematic representation of the generic n-channel nano-field effect transistor and the effective one-dimensional potential $V_{\it eff}$ (see text).

It is calculated from a one-dimensional scattering problem

$$\left[-\frac{\hbar^2}{2m^*} \frac{d^2}{dy^2} + V^{eff}(y) - \varepsilon \right] \psi^{eff;S/D}(y,\varepsilon) = 0, \tag{3}$$

where the $\psi^{{\it eff;SD/D}}$ are the effective scattering functions emitted from source- and drain contact,

respectively. The former ones obey the asymptotic boundary conditions $\psi^{\text{eff};S}(y \geq L, \varepsilon) = (t^S(\varepsilon)/\sqrt{2\pi})e^{ik_{x_s}^{\text{eff}}(y-L)}$, where $k_S^{\text{eff}} = \sqrt{2m^*\varepsilon/\hbar}$, and $k_D^{\text{eff}} = \sqrt{2m^*(\varepsilon+V_D)/\hbar^2}$. For a derivation of a scale –invariant expression for the drain current it is necessary that the effective potential depend only on a small number of essential properties of the transistor. In this spirit we assume $V^{\text{eff}}(y \leq 0) = 0$, $V^{\text{eff}}(y \geq L) = -V_D$, and outside the contacts a piecewise linear potential, $V^{\text{eff}}(0 \leq y \leq L) = V_0 - V_D y/L$. As illustrated in Fig. 1 we peplace the unknown parameter V_0 by a parameter V_G representing the gate voltage which we define as the deviation of the chemical potential in the source-contact form the maximum of the source-drain barrier, i. e. $\mu = V_0 + V_G$.

We now rewrite Eq. (1) in a scale –invariant form. To this end we first normalize in Eq. (3) lengths to L and energies to V_0 defining $\hat{y} = y/L$ and $\hat{\varepsilon} = \varepsilon/V_0$ to obtain

$$\left[-\frac{1}{\beta} \frac{d^2}{d\hat{y}} + \hat{v}^{eff}(\hat{y}) - \hat{\varepsilon} \right] \hat{\psi}^{eff}(\hat{y}, \hat{\varepsilon}) = 0$$
(4)

Here $\beta = 2m * V_0 L^2 / \hbar^2$, $\hat{v}^{eff}(\hat{y}) = V^{eff}(y) / V_0$, and $\hat{\psi}^{eff}(\hat{y}, \hat{\varepsilon}) = \psi^{eff}(y, \varepsilon) = \psi^{eff}(L\hat{y}, V_0 \hat{\varepsilon})$. Applying the latter relation to the scattering states yields

$$\widetilde{T}^{eff}(\varepsilon) = \hat{k}_D^{eff}(\hat{\varepsilon}) |\hat{t}^S(\hat{\varepsilon})|^2 [\hat{k}_S^{eff}(\hat{\varepsilon})]^{-1} = \widetilde{T}(\hat{\varepsilon}; \beta, \hat{v}_D) = \widetilde{T} \left[\hat{\varepsilon}; l^2(m - v_G), \frac{v_D}{m - v_G}\right]. \tag{5}$$

Here $\widetilde{T}(\hat{\varepsilon},\beta,\hat{v}_D)$ is the current transmission in the scaled effective problem Eq. (4). It depends only on the parameters β and $\hat{v}_D = V_D/V_0$. Furthermore, one has $\hat{k}_S^{eff}(\hat{\varepsilon}) = \sqrt{\beta}\hat{\varepsilon}$, $\hat{k}_D^{eff}(\hat{\varepsilon}) = \sqrt{\beta}(\hat{\varepsilon}+\hat{v}_D)$, and $\hat{t}^S(\hat{\varepsilon}) = t^S(\varepsilon)$. In the last step of Eq. (5) we introduce the gate voltage-independent parameters $v_D = V_D/\varepsilon_F$, $v_G = V_G/\varepsilon_F$, and $m = \mu/\varepsilon_F$ so that $V_0/\varepsilon_F = m - v_G$ and $\beta = l^2(m - v_G)$ with the characteristic length of the electron channel $l = \sqrt{2m^*\varepsilon_F L^2}/\hbar$.

For the scaling of the supply function in Eq. (2) we define

$$s(\hat{x}) \equiv S(V_0 \hat{x}) = \frac{1}{2\sqrt{\pi}} w \sqrt{u} F_{-1/2} \left[(v_G - m) \frac{\hat{x}}{u} \right], \tag{6}$$

where $w = \sqrt{2m^*W^2\varepsilon_F}/\hbar$ is the characteristic width of the electron channel, $u = k_BT/\varepsilon_F$ is the normalized thermal energy, and $\hat{x} = x/V_0$. At a given thermal energy the chemical potential m is given by

$$m(u) = uX_{1/2} \left(\frac{4}{3\sqrt{\pi}} u^{-3/2} \right). \tag{7}$$

Here we assume a wide enough transistor and a sufficient junction depth a (see Fig. 1) so that the electrons in the contacts can be treated as a three-dimensional non-interacting electron gas. We now recast Eq. (1) in a dimensionless form

$$i = (m - v_G) \int_{0}^{\infty} d\hat{\varepsilon} \left[s \left(\hat{\varepsilon} - \frac{m}{m - v_G} \right) - s \left(\hat{\varepsilon} - \frac{m - v_D}{m - v_G} \right) \right] \widetilde{T}(\hat{\varepsilon}), \tag{8}$$

where $i = I/I_0$ with $I_0 = 2e\varepsilon_F/h$. Writing for the characteristic length $l = L/\lambda$ and the characteristic width $w = W/\lambda$ we introduce a scaling length $\lambda = \hbar/\sqrt{2m^*\varepsilon_F}$ for quantum transport.

Numerical results

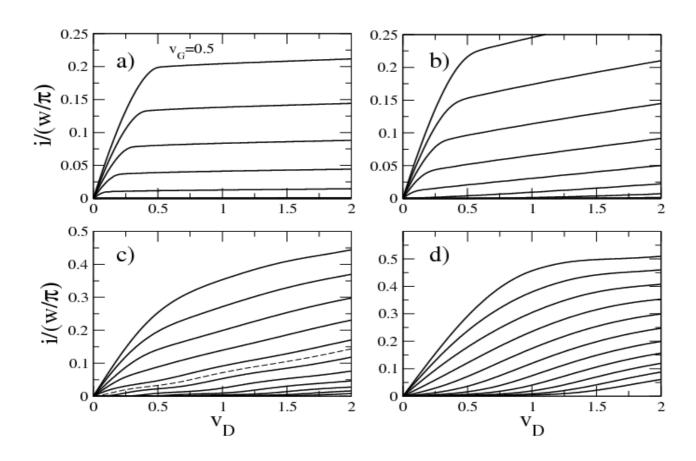


Figure 2: Calculated low-temperature drain characteristics (u=0.01) in the wide transistor limit, v_G starting from 0.5 with decrements of 0.1 (solid lines) a) 'ideal limit' l=500, b) 'strong barrier' l=40, c) 'transition regime' l=10, and d) 'weak barrier' l=5. In dashed lines for l=10 the best fit to a linear characteristic at v_G = 0.04.

We calculate the normalized drain current according to Eq. (8) in the limit of low temperatures, $u\sim0$, and wide transistors. From Figs. 2 (a) it can be seen that Eq. (8) yields a typical long-channel behavior at very large l (l=500 in our numerical examples): The drain characteristics show for small drain voltages an approximately linear dependence of the drain current turning quite abruptly into a saturation regime for larger drain voltages. In the strong barrier regime, represented by the calculation for l=40 (Fig. 2(b)), the drain characteristics still look similar to the long-channel characteristics. However, the traces close to threshold gate voltage $v_g \sim 0$ are not given by $i\sim0$. Instead, they can be described by a linear regression which increases in slope with decreasing characteristic length. This

nearly linear regression has already been found in the three-dimensional transistor model in Ref. [11] where it was called close-to-linear threshold characteristic (TH). Above the TH, in the ON-state regime, the i-v traces are similar to the ones in the long-channel limit, however, instead of a current saturation only a quasi-saturation with a marked residual slope di/dv_D is found. At $v_G < 0$, the transistor works as a tunneling transistor. Here another type of characteristic arises showing a positive bending as opposed to the negative bending at $v_g > 0$. In the transition regime to weak barriers $(l \sim 10$, see part (c) of Fig. 2) the traces for positive V_G in the drain characteristics become more and more rounded do that it becomes difficult to define a saturation regime. As shown in Fig. 2 (d) in the weak barrier limit, $l \le 5$, the i-v traces differ qualitatively from the long-channel characteristics because of very strong source-drain tunneling. In particular no TH can be defined.

To conclude, we present a scaling-approach for quantum-transport in nano-transistor with an abitrary material. In a simple model we find a scaling length for quantum transport and an expression for the dimensionless drain current as a function of five dimensionless parameters. These parameters are the normalized drain voltage, -gate voltage and -temperature as well as the characteristic length and width of the electron channel. For a wide transistor and low temperature, we evaluate numerically the scaleinvariant drain characteristics.

We thank J. Emtage and M. Krahlisch for valuable discussions.

- [1] P. Gargini, SEMI Industry Strategy Symposium Europe, Dresden, Febr. 1 3, 2009.
- [2] M. Radosavljevic, IEDM 2007 and 2008.
- [3] S. M. Sze, *Physics of Semiconductor Devices* (John Wiley & Sons, New York, 1981).
- [4] R. H. Dennard, F. H. Gaensslen, H.-N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, IEEE J. Solid-State Circuits **SC-9**, 256 (1974).
- [5] J. R. Brews, W. Fichtner, E. H. Nicollian, and S. M. Sze, IEEE Electron Devices 36, 504 (1989).
- [6] K. K. Young, IEEE Trans. Electron Devices 36, 504 (1989).
- [7] R.-H. Yan, A. Ourmazd, and K. F. Lee, IEEE Trans. Electron Devices 39, 1704 (1992).
- [8] C.P. Auth and J. D. Plummer, IEEE Trans. Electron Devices 18, 74 (1997).
- 55, 313 (2008).
- [9] M. Lundstrom and J. Guo, *Nanoscale Transistors* (Springer, Berlin, 2006)
- [10] J. L. Autran and D. Munteanu, J. Comp. Theor. Nanosci. 5, 1120 (2008).
- [11] G. A. Nemnes, U. Wulf, and P. N. Racec, J. Appl. Phys. 96. 596 (2004).
- [12] G. A. Nemnes, U. Wulf, and P. N. Racec, J. Appl. Phys. 98, 84308 (2005).