Scaling Trends of Digital Single-Event Effects: A Survey of SEU and SET Parameters and Comparison With Transistor Performance

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***Abstract*—The history of integrated circuit (IC) development is another record of human challenges involving space. Efforts have been made to protect ICs from sudden malfunctions due to single-event effects (SEEs). These effects are triggered by only a single strike of particle radiation, such as an α-ray or cosmic ray, originating from our solar activity and galactic events including supernovas. This article explores how SEEs have evolved along with the progress in complementary metal-oxide-semiconductor (CMOS) digital IC technology, or device scaling, from the early micrometer-scale generations to the current nanometer-scale generations. For this purpose, focusing on basic digital elements, that is, inverters and static random access memories (SRAMs), this study collected more than 100 sets of data on four characteristic parameters of single-event upsets (SEUs) and single-event transients (SETs), both of which are undesired flips in digital logic states. The results show that all the examined parameters, such as the SEU critical charge, decrease with the device feature size. Analysis involving structure classification, such as bulk versus silicon-on-insulator (SOI) substrates and planar versus fin channels, reveals relationships between the examined SEE parameters and other device features such as the power supply voltage. All the data collected in this survey are explicitly given in tables for future exploration of IC reliability.**

***Index Terms*—Error analysis, ion radiation effects, neutron radiation effects, semiconductor device reliability, single-event transients (SETs), single-event upsets (SEUs), soft errors, static random-access memories (SRAMs).**

I. Introduction

RADIATION causes a variety of reliability problems in integrated circuits (ICs). Even a single strike of particle radiation such as an α-ray can lead to a catastrophic malfunction. A single-event effect (SEE) is such an undesired effect due to a single strike of particle radiation. SEEs have been serious for more than half a century [1], causing actual financial losses in both space and terrestrial IC systems.

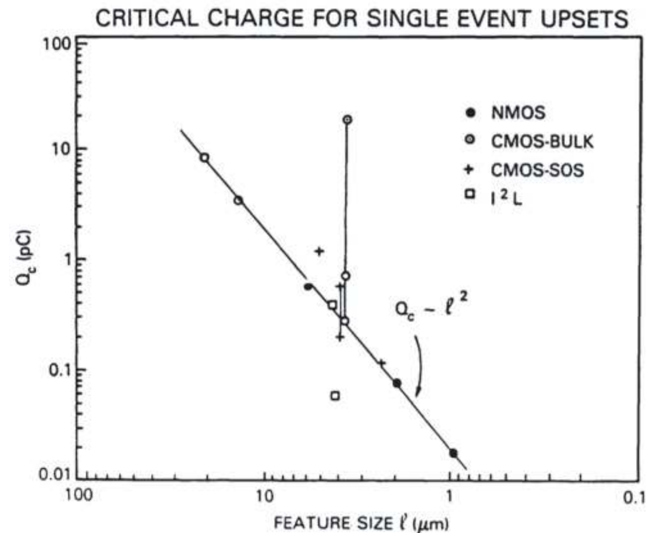

Fig. 1. Scaling trend revealed by Petersen *et al.* [4]. ©1982, IEEE.

Understanding the evolution of SEEs requires deep knowledge of the evolution of IC devices, including even parasitic elements, which are byproducts of the intended purposes of target devices. Without advance notice, an incidence of particle radiation deposits energy inside an IC chip along its track. This forcible injection of energy wrongly activates not only target devices but also parasitic elements, even though parasitic elements are originally designed not to be activated during normal operation. In particular, knowledge of device miniaturization or scaling, which is associated with Moore's law [2] and Dennard's rules [3], is important because of its crucial role in the progress of digital IC technology. In fact, the history of SEEs started from a theoretical discussion of their influence on the progress of device scaling [1].

In 1982, which was about five years after the first observations of SEEs in space [5] and on the ground [6], Petersen *et al.* [4] surveyed the literature on one type of SEE, a single-event upset (SEU), which is an undesired bit flip of digital memory caused by a single strike of particle radiation. They examined the minimum amount of charge, called the critical charge (Q_C), that is necessary for an SEU in dynamic and

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TABLE I
EXAMPLES OF PREVIOUS WORKS RELATED TO DEVICE SCALING EFFECTS ON SEEs

Ref.	Year	Feature size (l)	Structure (see Table III)	SEE	Note
[4]	1982	21 15 6 5 4.5 4 2.5 2 1	Bulk-Planar*, SOI-Planar‡, I^2L	SEU	
[7]	1982	4 3 2 1 0.8 0.6 0.4	Bulk-Planar*, SOI-Planar‡	SEU	Based on scaling rule
[13]	1982	2 1	Bulk-Planar (DRAM)	SEU	
[14]	1984	3.6 2.9 2.7 1.8	SOI-Planar‡	SEU	
[15]	1987	2 1	Bulk-Planar	SEU	
[16]	1990	2 1.8 1.6 1.5 1.25 1	Bulk-Planar	SEL	
[17]	1996	2 1 0.5 (in μm)	Bulk-Planar	SEU	
[18]	2000	800 600 350 100 (in nm)	Bulk-Planar	SEU	Based on scaling rule?
[19]	2003	280 250 210 200 180	Bulk-Planar	SEU	
[20]	2002	500 350 250 180 130 90	Bulk-Planar	SEU	
[21]	2002	350 280 180	Bulk-Planar	SEU	
[22]	2002	600 350 250 180 130 100 70 50	Bulk-Planar	SEU	Based on scaling rule
[23]	2003	250 180 130 90 65	Bulk-Planar	SEU	
[24]	2004	180 130 90	Bulk-Planar, SOI-Planar	SEU	
[25]	2005	180 130 90 65	Bulk-Planar	SEL	
[26]	2005	250 180 130 90 65	Bulk-Planar	SEL	
[27]	2006	180 130 90	Bulk-Planar	SEU	
[28]	2009	180 130 90 65 45		SEU	
[29]	2010	250 180 130 90 65 45 32 22	Bulk-Planar	SEU	Based on scaling rule
[30]	2010	130 90 65	Bulk-Planar	SET	
[31]	2011	250 220 210 180 170 160 150 140 ↩	Bulk-Planar*	SEU	Collection of error rates
		↪ 130 120 110 100 106 96 95 ↩			from various vendors
		↪ 92 90 80 70 65 45 40			
[32]	2011	250 180 90 65	Bulk-Planar	SEU, SET	
[33]	2011	65 55 45 40 32 22 16	Bulk-Planar	SEU	Based on scaling rule
[12]	2011	90 73 72 65 63 51 50	Bulk-Planar (Flash)	SEU	
[34]	2013	350 250 180 130 90 65 40 28	Bulk-Planar	SEU	
[35]	2013	250 180 130 90 65 45 32 28 14	Bulk-Planar, SOI-Planar	SEU	Comparison with [4]
[36]	2013	45 32	SOI-Planar	SET	
[37]	2014	65 40 28	Bulk-Planar	SEU	
[38]	2015	180 130 90 65 45 32 22 14	Bulk-Planer, Bulk-Fin	SEU, SET	
[11]	2017	500 120 90	SiGe BiCMOS	SET	
[39]	2018	14 10	Bulk-Fin	SEU	
[40]	2018	16 7	Bulk-Fin	SEU	

* Includes DRAMs.
‡ Silicon-On-Sapphire (SOS) structures were also examined. For simplicity, the present study classifies SOS structures as Silicon-On-Insulator (SOI) structures (see the text).

static random access memories (DRAMs and SRAMs). The energy injected by radiation creates a huge amount of charge. Once this charge exceeds Q_C, the struck memory exhibits an upset (see Section II for details). As shown in Fig. 1, Petersen *et al.* [4] revealed a scaling trend of $Q_C = 0.023l^2$, where l denotes the feature size of the device. In the same year, Pickel revealed a similar trend, $Q_C = 0.85(l/4)^{1.5}$, in his own work [7]. As listed in Table I,[1] since those pioneering studies, many other studies have investigated the impacts of device scaling on SEEs, including SEUs, single-event transients (SETs), and single-event latch-ups (SELs). These previous studies have tested a wide range of IC structures, from the standard complementary metal-oxide-semiconductor (CMOS) structure to state-of-the-art structures such as a SiGe bipolar CMOS (BiCMOS) [11] and flash memory [12]. To date, however, no attempt has been made to examine SEEs across all generations, from the early micrometer-scale generations to today's nanometer-scale generations.

Hence, the aim of this study is to explore the whole history of SEE evolution from the viewpoint of device scaling. For this purpose, as summarized in Table II, this study collected data on four key parameters for SEUs and SETs, both of which are particularly serious in the core of CMOS digital IC systems, where device scaling plays its crucial role. In this regard, other SEEs such as SELs and single-event functional interrupts (SEFIs) are not addressed in this study. Together with reasons for not addressing these SEEs, Section II gives detailed information about the examined SEEs (SEUs and SETs) and parameters, as well as the data collection and

[1] During the course of the review of this article, further works were presented [8]–[10].

analysis procedures used in this study. The bulk of this article consists of Section III, which shows how the parameters have evolved along with l. That section also seeks the physical mechanisms behind the revealed evolution, through comparison with various device features such as the power supply voltage (V_{DD}). Note that all the collected data are given in tabular form for future study.

II. Method

A. Tested SEEs and Devices

As illustrated in Fig. 2, CMOS digital ICs typically suffer from four kinds of SEEs: (a) SEUs, (b and b') SETs, (c) SELs, and (d) SEFIs. They all originate from charge injected by an incidence of particle radiation such as

1) α-rays: He nuclei from radioactive materials [41];
2) galactic cosmic rays (GCRs): charged nuclei originating in space, including heavy ions such as Fe nuclei [42]; and
3) terrestrial neutrons: constituents of terrestrial cosmic rays resulting from interactions between GCRs and Earth's atmosphere [41].

When entering Si, for example, a 4-MeV α-ray emitted from ^{238}U loses 150 keV of energy during its first 1 μm of passage [6]. Ionization consumes 99.9% of the energy. α-rays can excite electrons through Coulomb force because of their charge of $+2q$, where q represents the elementary charge. This ionization process deposits electron–hole pairs (ehps) with as much charge as 6.7 fC, which is obtained by dividing 150 keV by the pair-creation energy of 3.6 eV/ehp or 22.5 keV/fC [43]–[45]. Moreover, although terrestrial neutrons are not charged, they can cause the above-mentioned SEEs through the same charge-deposition process, but with additional nuclear reactions that create energetic nuclei.

Among the four SEEs, this study focuses on SEUs in SRAMs [Fig. 2(a)] and SETs in inverters [Fig. 2(b)]. These are continuous or instant flips in digital logic states. This study selected SRAMs and inverters as the target logic elements because they are the most basic building blocks of CMOS digital ICs, whose performance is crucially influenced by device scaling and often characterized in the literature to discuss the benefits of new ideas. In this regard, although CMOS digital IC circuitry is sometimes modified by using additional circuit elements for increasing SEE hardness (e.g., a dual interlocked storage cell or DICE [46]), this study does not concern such radiation hardening by design (RHBD). Instead, unless otherwise specified, it concentrates on standard (non-RHBD) SRAM cells and inverters to investigate the native responses of SEEs to device scaling.

Note that although this study focuses only on SEUs and SETs in the basic digital elements, it does not lessen the significance of the other SEEs. As illustrated in Fig. 2(b'), phase-locked loops (PLLs) are sensitive to SETs, which typically manifest themselves in analog or frequency domains with effects such as severe jitter and signal losses [47]–[49]. This PLL SET is not addressed in this study because of the small amount of literature data. An anomalous increase in current caused by an erroneous activation of parasitic thyristors, that is, an SEL [Fig. 2(c)], is still significant and exhibits complex responses to device design. As suggested in [50], SEL depends on parameters that do not always shrink along with device scaling, such as the dimension of wells and the depth of shallow-trench isolation (STI). Hence, SEL is not addressed here—A literature survey, however, suggests that CMOS digital ICs generally become less sensitive to SEL along with the scaling of V_{DD} [51, Fig. 39]. CMOS digital ICs also suffer from SEFIs [Fig. 2(d)], that is, interruptions in operation, such as a reset or lock-up while running a task [52]. SEFI is known to be caused by SEUs, SETs, and SELs in IC control blocks. Although it is interesting to see how SEFI has evolved, it is not addressed here because of the complexity that originates from the variety of tested circuitry. Furthermore, although not shown in Fig. 2, single-event displacement damage might soon become significant. As typified by nuclear reactions induced by neutrons, radiation transfers energy to matter through nonionizing processes, such as knockout, that cause displacement damage. Such single-event displacement damage has already been observed in various electronic devices (see [53] and references therein), but so far, it has been negligible in the logic elements of CMOS digital ICs; hence, this study ignores it. A very recent simulation study [54] predicted, however, that terrestrial neutrons may cause significant impacts on the electrical characteristics of transistors in the 6-nm generation. In this regard, note also that a large-scale study on simulating single-event displacement damage has been conducted in recent years [55]–[57].

TABLE II
Tested SEEs and Parameters

SEE	Device	Parameter	
		Symbol	Description
SEU	SRAM	Q_C	Critical charge (fC)
		L_T	Threshold LET† (MeVcm^2/mg)
		σ_∞	Saturated cross section (cm^2)
SET	Inverter	δ	Duration of digital flip (ps)

† Linear Energy Transfer, denoted by L in the text.

B. Tested Parameters

As explained above, this article investigates SEUs in SRAMs and SETs in inverters from the viewpoint of device scaling. Here, brief descriptions are given for the tested phenomena and parameters.

1) Single-Event Upsets: As conceptually illustrated in Fig. 2(a), which concerns a cross-coupled inverter latch in an SRAM cell, charge collection results in a nonzero current I, leading to an undesired voltage change at the output of the struck inverter (V_Q). In this example, particle radiation strikes an OFF-state n-type MOS transistor, hereinafter abbreviated as NMOS (along with PMOS for the counterpart p-type transistor). The struck NMOS collects electrons ($I < 0$), and thus V_Q drops from its original level at V_{DD} or logic 1. After propagating through the succeeding inverter, this V_Q drop turns off the pull-up PMOS connected to the struck NMOS.

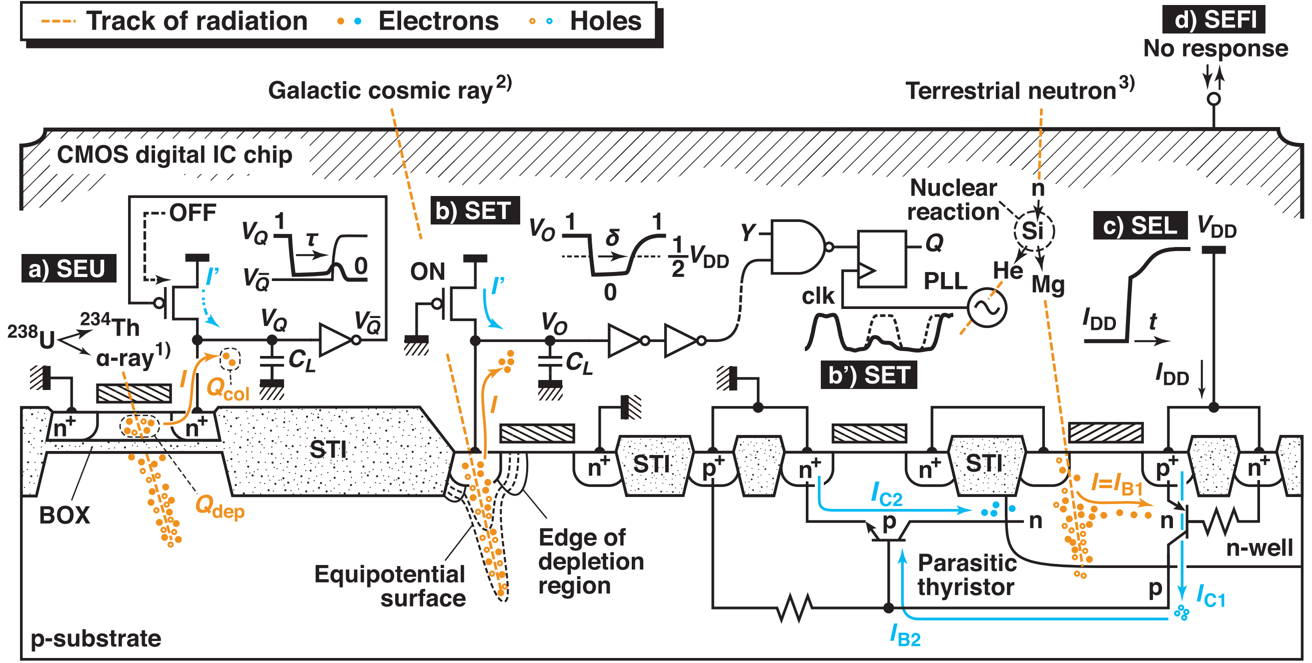


Fig. 2. Conceptual drawing of SEEs in a CMOS digital IC. A hybrid substrate structure (bulk+SOI) is assumed for illustrative purposes.

This feedback prevents the PMOS from providing current for recovery (I'). As a result, the memory state is completely flipped and becomes stable in the wrong state of logic 0 (see [58] for more details). This study investigates the following two parameters, which are commonly used to describe the threshold for this flip:

Q_C The minimum amount of charge required for an SEU, or the critical charge. This is typically gauged in terms of Q_{col}, the amount of charge collected at the drain terminal of a struck transistor (see also Section III-A).

L_T The minimum linear energy transfer (LET or L) necessary for an SEU, often called the threshold LET. The value of L describes the ability of radiation to deposit energy (or charge) along its track. This value is usually given in a charge-based unit (fC/nm) or an energy-based unit normalized by the target matter's density (MeVcm^2/mg). Unless otherwise specified, this study uses the latter energy-based unit; when needed, the former charge-based unit is converted with a conversion factor for Si: 1 fC/nm = 100 MeVcm^2/mg.

The study also investigates the following parameter that indicates sensitive locations in an SRAM cell:

σ_∞ Saturated cross section. In general, the cross section (σ) describes the sensitive area of a tested device and is often estimated through the following relationship when the device is a memory:

$$\sigma = \frac{U}{fM} \tag{1}$$

where U, f, and M denote the number of upsets observed, the total fluence of particle radiation during the irradiation, and the total number of memory cells

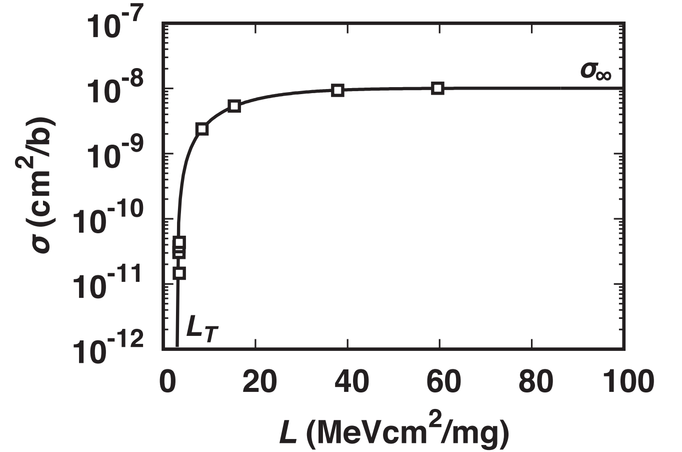


Fig. 3. Measured evolution of σ in an SOI-Planar SRAM as a function of L [59]. The symbols represent measurement results obtained from (1), while the line represents the best-fit Weibull function, $\sigma = \sigma_\infty \exp[-\{(L - L_T)/W\}^S]$, where W and S are arbitrary fitting parameters.

exposed to radiation, respectively. As shown in Fig. 3, in general, σ abruptly develops at L_T and saturates to σ_∞ as L increases. This study measures σ_∞ in the units of cm^2/b, where b denotes bit, with a proper unit conversion when necessary.

2) Single-Event Transients: When exposed to particle radiation [Fig. 2(b)], an inverter exhibits an instantaneous change in its output voltage (V_O). Unlike SRAM SEUs that rely on a self-shutoff mechanism, V_O returns to the original level after some time, because the struck transistor's counterpart, for example, the pull-up PMOS in the figure, continues to feed I'. Then, however, the resultant glitch or transient false state, also called "digital SET (DSET)," can propagate through the

TABLE III
FOUR CATEGORIES OF CMOS DEVICE STRUCTURES EXAMINED IN THIS STUDY

Channel	Substrate: Bulk	Substrate: SOI†
Planar	Bulk-Planar ●	SOI-Planar □
Fin*	Bulk-Fin ▲	SOI-Fin ◇

† Includes similar substrate structures such as SOS.
* Includes similar three-dimensional channel structures such as a tri-gate.

chains of logic gates and finally overwrite the bit information stored in flip-flops (FFs) at the ends (see [60] for more details). Hence, this study investigates the following parameter because of its importance for the propagation and latch probabilities [61]:

- δ The temporal width of a false state, specifically the SET pulsewidth measured at a logic threshold (when needed, this study uses $V_{\mathrm{DD}}/2$ as the threshold level). Because δ usually exhibits a range, this study investigates its maximum and minimum values. Moreover, the study makes no distinction between δ before and after propagation, although it can change while propagating through a logic chain [62].

C. Data Collection and Analysis

The four SEE parameters described above were collected from articles already published. The parameter values were simply copied when given numerically in the reference articles. When not given numerically, they were extracted from figures. In either case, this data collection process did not attempt to assess the validity of the collected values. In other words, the values were not subjected to any correction or selection process. Hence, the analysis in Section III mainly focuses on global trends in the groups of collected values.

To investigate the evolution of the SEE parameters, l values were also recorded from the reference articles. When an article did not explicitly give the value l, the gate length was used instead. Additional information such as the test conditions and device structures was also recorded for analysis. The device structures were classified into four categories as summarized in Table III, consisting of 2×2 combinations of channel and substrate structures. Although the silicon-on-insulator (SOI) substrates can be categorized as fully depleted (FD) and partially depleted (PD) SOI substrates, such further categorization was not applied because of the limited amount of data. Instead, the thicknesses of the SOI and buried oxide (BOX) layers (d_{SOI} and d_{BOX}, respectively) were collected whenever possible. Regarding the use of terms for structure classification, note that, for example, when the term of "Bulk" is used alone (e.g., "Bulk SRAM"), it includes both Bulk-Planar and Bulk-Fin SRAMs. The symbols in this table are consistently used in the following section's figures.

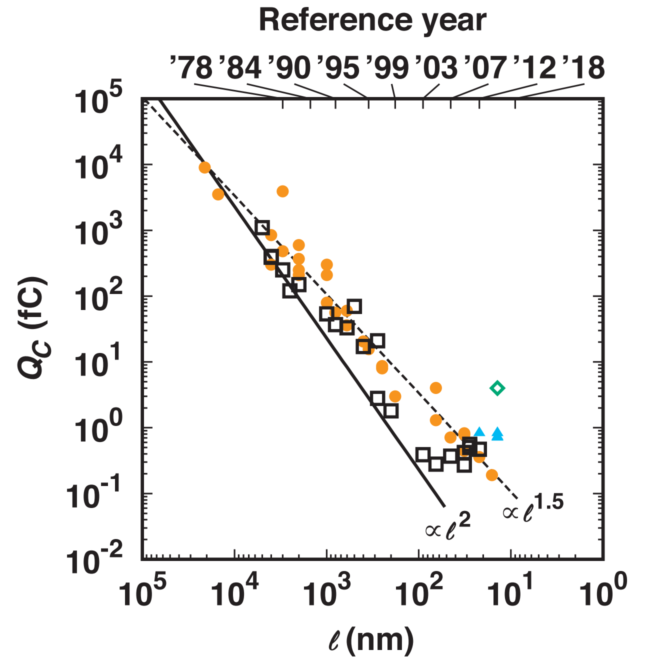


Fig. 4. Evolution of Q_C. The solid and dashed lines represent the trends reported by Petersen *et al.* [4] and Pickel [7], respectively.

III. RESULTS AND DISCUSSION

A. SRAM Q_C

Tables IV and V list SRAM Q_C values collected from the literature. Fig. 4 shows a graphical representation of this collection, displaying the evolution of Q_C as a function of l. In general (regardless of the categories of device structures), Q_C constantly decreases with l across five orders of magnitude. Interestingly, this scaling trend seemingly halts at $Q_C \approx 0.5$ fC. Note that the top axis in this figure provides a reference timescale that corresponds to the progress of Intel logic technologies, summarized in Table VI [84].

Fig. 4 shows that the data conform well overall to the trends predicted by Petersen *et al.* [4] and Pickel [7] in 1982. A closer look suggests that Petersen's l^2 trend provides the lower boundary of all the data, consisting mainly of the data for SOI-Planar SRAMs. On the other hand, the Bulk-Planar data spread around Pickel's $l^{1.5}$ trend. Note that although Pickel investigated trends for both SOI-Planar and Bulk-Planar SRAMs, Fig. 4 presents only the Bulk-Planar trend for illustrative purpose (see also the last paragraph of this section).

The following analysis suggests that the revealed trends depend mainly on the scaling trends of V_{DD} and load capacitance (C_L), where C_L represents the total capacitance of the inverter output node in an SRAM cell. As explained in Section II-B1, an SEU is triggered by a V_Q drop due to undesired dissipation of signal charge, that is, $C_L V_{\mathrm{DD}}$. Hence, Q_C is widely expressed as $Q_C = aC_L V_{\mathrm{DD}}$, with the constant a varying across articles. This study uses $a = 2$ according to [85], which models Q_C as follows:

$$Q_C = C_L V_{\mathrm{DD}} + I_{\mathrm{ON}} \tau. \tag{2}$$

The second term on the right-hand side corresponds to additional charge due to the recovery current I'. In (2), this

TABLE IV
SEU Q_C VALUES COLLECTED FROM THE LITERATURE FOR THE BULK STRUCTURES (SEE TABLE V FOR SOI)

l (nm)	Q_C (fC)	Q_{col} [†]	Exp.[*]	Structure	Reference	Note[♭]
				Bulk-Planar		
21 000	9000	✓		●	[4, Table I]	Theory: $0.8C_LV_{DD}$ [63]
15 000	3500	✓		●	[4, Table I]	Theory: $0.8C_LV_{DD}$ [63]
4000	300		✓	●	[4, Table I]	$L_T d_{DR}$ [64]
4000	840	✓		●	[7, Fig. 4]	SPICE
3000	478	✓		●	[7, Fig. 4]	↓
2000	249	✓		●	[7, Fig. 4]	↓ Miniaturized from 4000 nm
1000	78.8	✓		●	[7, Fig. 4]	↓ through a scaling rule
800	55.4	✓		●	[7, Fig. 4]	↓
600	36.0	✓		●	[7, Fig. 4]	↓
400	20.3	✓		●	[7, Fig. 4]	↲
3000	3900	✓		●	[65, Fig. 1]	SPICE; R: 3600–4250 fC
2000	600	✓		●	[65, Fig. 2]	SPICE
2000	210	✓		●	[66, Table III]	Theory: C_LV_{DD}; l from [67]
2000	360	✓		●	[68, Fig. 3]	SPICE
1500	300	✓		●	[69, Table 1]	SPICE
1000	210	✓		●	[70]	SPICE
250	8	✓		●	[71, Table II]	SPICE
180	3	✓		●	[71, Table II]	SPICE
600	60	✓		●	[72, Fig. 2]	TCAD; R: 60–98 fC
350	16	✓		●	[72, Fig. 2]	TCAD; R: 16–22 fC
250	8.6	✓		●	[72, Fig. 2]	TCAD; R: 8.6–15 fC
65	4.0	✓		●	[73, Table I]	SPICE
65	1.3	✓		●	[33, Table I]	SPICE
45	0.71	✓		●	[33, Table I]	↓
32	0.44	✓		●	[33, Table I]	↓ Miniaturized from 65 nm
22	0.36	✓		●	[33, Table I]	↓ through a scaling rule
16	0.19	✓		●	[33, Table I]	↲
32	0.83	✓		●	[74, Table I]	SPICE
32	0.78	✓		●	[75, Table IV]	TCAD+SPICE
				Bulk-Fin		
22	0.83	✓		▲	[74, Table I]	SPICE
14	0.71	✓		▲	[74, Table I]	SPICE
14	0.73	✓		▲	[75, Table IV]	TCAD+SPICE

[†] Q_C was defined by Q_{col}. The other values were defined by Q_{dep}.
[*] Q_C was determined experimentally. The other values were obtained by theory or simulation (see the "Note" column: "SPICE" indicates that the analysis used a circuit simulator, while "TCAD" indicates a numerical device simulator).
[♭] Some papers reported a range of Q_C values. For those cases, the second column lists a representative value, while the "Note" column gives the range, denoted by"R:".

additional charge was estimated from the time taken for the V_Q drop to be latched (τ) and the ON-current (I_{ON}), that is, the saturated drain current in the ON-state transistor when $|V_{GS}| = |V_{DS}| = V_{DD}$, where V_{GS} and V_{DS} represent the gate– and drain–source voltages, respectively. This study further assumes that τ is given by an inverter propagation delay model as $0.79C_LV_{DD}/I_{ON}$ [86], thus giving $a \approx 2$.

Fig. 5 compares $2C_LV_{DD}$ with the literature data for Bulk SRAMs. The dashed line indicates $2C_LV_{DD}$, where C_L is assumed to be the same as the intrinsic gate capacitance of the succeeding inverter

$$C_g = 2\frac{\varepsilon_{OX}}{d_{OX}} l w. \tag{3}$$

Here ε_{OX}, d_{OX}, and w represent parameters of a single transistor in a cell, that is, the gate oxide film's permittivity, its thickness, and the gate width, respectively. The factor of 2 is used for estimating the capacitance of the inverter input. The transistor parameters were extracted from a survey of Bulk SRAM cells, as shown in Fig. 6 [87], [88], and modeled as follows:

$$V_{DD} = 0.005l + 0.7 \tag{4}$$

$$C_g = 0.003l \tag{5}$$

$$w = \begin{cases} 2l, & \text{for } l \geq 40 \text{ nm;} \\ 80, & \text{for } l < 40 \text{ nm.} \end{cases} \tag{6}$$

TABLE V

SEU Q_C VALUES COLLECTED FROM THE LITERATURE FOR THE SOI STRUCTURES (SEE TABLE IV FOR BULK)

l (nm)	Q_C (fC)	Q_{col}†	Exp.*	Structure	Reference	Note♭		
				SOI-Planar		d_{SOI} (nm)	d_{BOX} (nm)	
5000	1100		✓	□	[4, Table I]	500		$L_T d_{SOI}$ [64]; see Table VIII
4000	400		✓	□	[4, Table I]	550		$L_T d_{SOI}$ [76]; see Table VIII; R: 200–600 fC
2500	120		✓	□	[4, Table I]	500		$L_T d_{SOI}$ [77]; see Table VIII; l = 2000 nm?
4000	390	✓		□	[7, Fig. 6]	400		SPICE
3000	251	✓		□	[7, Fig. 6]	↓		↓
2000	149	✓		□	[7, Fig. 6]	↓		↓ Miniaturized from 4000 nm
1000	53.8	✓		□	[7, Fig. 7]	↓		↓ through a scaling rule
800	37.0	✓		□	[7, Fig. 7]	↓		↓
600	32.9	✓		□	[7, Fig. 6]	↓		↓
400	17.1	✓		□	[7, Fig. 7]	↲		↲
500	70		✓	□	[78]	85	400	$L_T d_{SOI}$; see Table VIII
280	21	✓		□	[79, Fig. 4]	100	500	TCAD+SPICE; R: 21–42 fC
280	2.8			□	[79]	100	500	TCAD+SPICE
200	1.8		✓	□	[71, Table II]	50	100	$L_T d_{SOI}$; d_{SOI}, d_{BOX} from [59]
90	0.39			□	[80, Table I]			TCAD
65	0.28			□	[80, Table I]			TCAD; Exp. R: 0.38–0.47 fC
45	0.37			□	[80, Table I]			TCAD
32	0.27			□	[80, Table I]			TCAD; Exp. R: 0.27–0.36 fC
32	0.42			□	[80, Table I]			TCAD; Exp. R: 0.53–0.69 fC
22	0.47			□	[80, Table I]			TCAD
28	0.56	✓		□	[81, Table IV]	70	100	SPICE; d_{SOI}, d_{BOX} from [82]
28	0.5	✓		□	[83]	7	25	SPICE; R: 0.5 or 0.1 fC
				SOI-Fin				
14	4.0			◇	[80, Table I]			TCAD; R: > 4.0 fC

† Q_C was defined by Q_{col}. The other values were defined by Q_{dep}.
* Q_C was determined experimentally. The other values were obtained by theory or simulation (see the "Note" column: "SPICE" indicates that the analysis used a circuit simulator, while "TCAD" indicates a numerical device simulator).
♭ Some papers reported a range of Q_C values. For those cases, the second column lists a representative value, while the "Note" column gives the range, denoted by"R:".

As is evident in Fig. 5, the assumption of $C_L = C_g$ well describes the evolution of Q_C in Bulk-Planar SRAMs across generations (note that the three latest generations, denoted by "a" in the figure, are results forecast by simulation based on a scaling rule). The observed agreement suggests the reason why Q_C decreases in proportion to $l^{1.5}$ rather than l^2. Although the scaling of C_g keeps pace with l^1, as shown in Fig. 6, that of V_{DD} is roughly proportional to $l^{0.5}$, because it gradually departs from the beginning l^1 trend and finally becomes almost constant at 0.7 V. Fig. 5 also demonstrates that the $C_L = C_g$ assumption underestimates and exhibits a discrepancy as large as one order of magnitude in comparison with Bulk-Fin SRAMs. This discrepancy almost disappears when $C_L = C_g + C_p$, where C_p denotes the parasitic capacitance. This study estimated C_p from w and a unit value of 0.7e−3 fC/nm, extracted from [89, Fig. 7], which suggests that the total parasitic components of the gate capacitance, such as overlap and fringe capacitance (see the inset and caption of Fig. 5), are almost constant at this value for a wide range of technology generations (l = 11–130 nm). The significance of C_p as revealed in Fig. 5 accords with the famous issue of Fin devices: Their RF performance is severely restricted by a relatively large C_p inherently due to their 3-D gate structure [90]–[92]. In this regard, efforts have been made to boost the speed of Fin devices by decreasing C_p, but note that such efforts essentially involve undesired Q_C degradation. Successfully solving this C_p dilemma will require close collaboration between SEE researchers and device or process professionals from a deep level of device development such as material selection (see also Section III-B).

TABLE VI

REFERENCE YEARS FOR THE SCALING TREND, WITH VALUES OBTAINED BY DIGITIZING [84, FIG. 2], WHICH SHOWS THE SCALING TREND FOR INTEL LOGIC TECHNOLOGIES

Year	l (nm)	Year	l (nm)	Year	l (nm)
1978	3000	1995	350	2007	45
1984	1500	1999	180	2012	22
1990	800	2003	90	2018	9

Although future study will be needed to identify the mechanism behind the l^2 trend for SOI-Planar SRAMs (Fig. 4), one should first take into account that the definition of Q_C varies

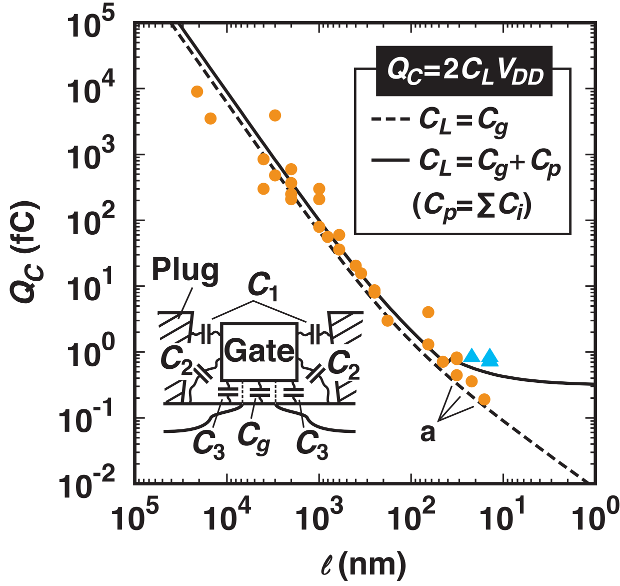


Fig. 5. Comparison of Bulk SRAM Q_C values between the literature data (symbols) and model estimations (lines). The inset conceptually illustrates the components of C_p used in this calculation; C_1: gate-to-plug capacitance, C_2: outer fringe capacitance, and C_3: overlap capacitance.

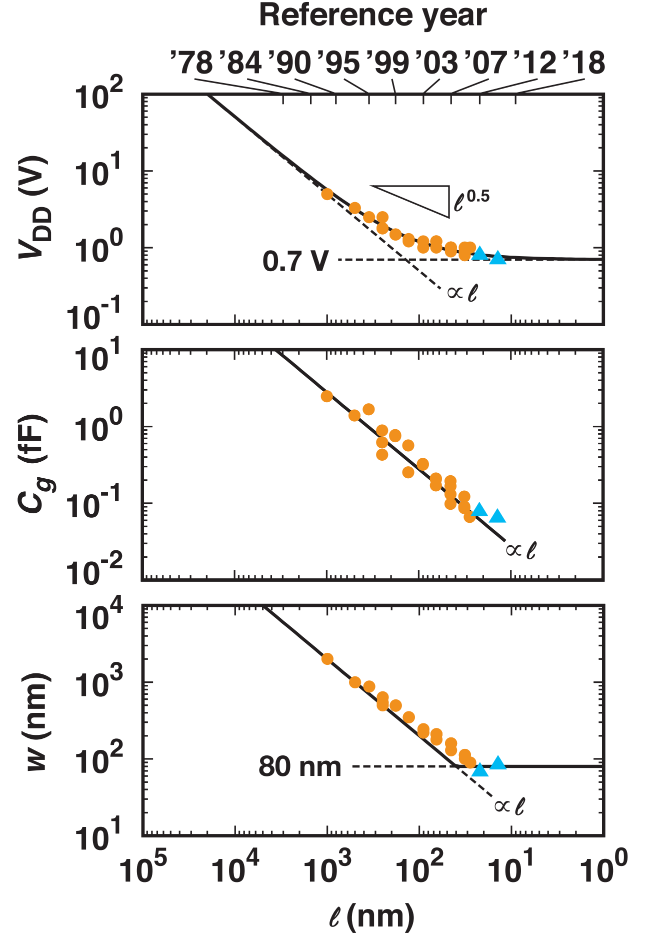


Fig. 6. Evolutions of transistor parameters in Bulk SRAM cells [87], [88]. C_g and w denote the gate capacitance and width of a single transistor, respectively. The symbols represent the data in [88], except for the w values for Bulk-Fin SRAMs. Those w values for Bulk-Fin SRAMs are not reported in [88] and hence were estimated by the author of the present study as $2H_{\text{fin}}$, where H_{fin} denotes the Fin height reported in [88]. The lines are eye guides (see text). The triangle for V_{DD} shows a reference slope for the dependence on l.

across articles. As seen in Table IV, the Q_C of Bulk SRAMs is mostly defined by Q_{col}. On the other hand (Table V), SOI SRAMs often rely on Q_C measured in terms of Q_{dep}, which represents the amount of charge deposited in a region in question, such as a body region [Fig. 2(a)]. Although Fig. 4 shows that the Q_C of SOI SRAMs is lower overall than that of Bulk SRAMs, the comparison is not straightforward because of this difference in definition. In SOI SRAMs, Q_C defined by Q_{col} is usually larger than that defined by Q_{dep}. For example (Table V), the 280-nm SOI SRAM tested in [79] exhibited 21 fC of Q_C as defined by Q_{col}, which is 10 times larger than the 2.8 fC as defined by Q_{dep}. The physical mechanism behind the factor of 10 is related to the existence of the BOX layer (see Section III-B for the details). Hence, Fig. 7 again compares Bulk and SOI SRAMs, but with Q_C only defined by Q_{col}. Interestingly, the l^2 trend disappears and is instead replaced by a universal curve showing the $l^{1.5}$ trend. The appearance of this universal curve seems inconsistent with the common agreement that SOI SRAMs have lower Q_C than Bulk SRAMs do—even when both Q_C values are defined by Q_{col}—because of their lower parasitic (junction) capacitance. This inconsistency is attributed to the limited amount of data in this survey and the spread of its distribution, which do not allow one to identify the difference between the SOI and Bulk SRAM data. A close look at Fig. 7 suggests that the SOI Q_C is approximately half the Bulk Q_C for $l \geq 400$ nm, for which all the data came from Pickel's simulation study [7]. His simulation relied on well-controlled SOI-Planar and Bulk-Planar SRAM samples, which both consisted of the same transistors except for the presence or lack of BOX.

B. SRAM L_T

Tables VII and VIII compile L_T values collected in this survey. As revealed in Fig. 8, except for the dramatic increase in L_T for the recent SOI-Planar SRAMs denoted by "a" and "b," L_T globally exhibits a scaling trend that is roughly proportional to $l^{1.5}$. Note that this study determined the slope parameter of 1.5 from the Q_C trend (Fig. 4) and the value of 1.6 ± 0.2 predicted by Brucker *et al.* [14] for SOI-Planar SRAMs. Fig. 8 also presents three reference values (L_1–L_3) that correspond to the typical upper bounds of the distribution of L in various radiation environments. Comparing L_T with these reference values underscores the increasing complexity of SEE mechanisms in the context of the variety of radiation, as follows.

First, Fig. 8 shows that L_T was already lower than L_1 in the very early 4-μm generation. This L_1 of 100 MeVcm^2/mg corresponds to the maximum value of L in the space radiation environment, or more specifically GCRs. Hence, the L_1 comparison suggests that CMOS SRAMs have been sensitive to GCRs since their inception, which dates back to the late 1970s, as seen from the top axis in the figure. This period corresponds to the historic year of 1975 when Binder *et al.* first demonstrated GCR-induced satellite anomalies [5]—It seems challenging to find a meaning behind this agreement, because

TABLE VII
SEU L_T VALUES COLLECTED FROM THE LITERATURE FOR THE BULK STRUCTURES (SEE TABLE VIII FOR SOI)

l (nm)	L_T (MeVcm^2/mg)	Exp.*	Structure	Reference	Note♭
			Bulk-Planar		
2000	32.8	✓	●	[66]	
2000	3.5	✓	●	[66, Table III]	l from [67]
1300	3	✓	●	[93, Table I]	NMOS cell
1000	4	✓	●	[93, Table I]	NMOS cell
1000	3	✓	●	[93, Table I]	NMOS cell
800	10	✓	●	[93, Table I]	
2000	25		●	[17, Fig. 5]	TCAD; Exp. R: 14–30 MeVcm^2/mg
1000	6.6		●	[17, Fig. 5]	TCAD
500	4.2		●	[17, Fig. 5]	TCAD; Exp. R: 2.34–6.99 MeVcm^2/mg
600	7		●	[94, Fig. 3]	TCAD
600	10	✓	●	[95, Fig. 4]	
600	8		●	[85]	TCAD
350	2.5		●	[85]	TCAD
130	0.88		●	[96, Fig. 10]	TCAD
90	1.08		●	[96, Fig. 10]	TCAD
60	0.58		●	[96, Fig. 10]	TCAD
250	2.0	✓	●	[97]	
250	4.1	✓	●	[98]	
60	0.01	✓	●	[99]	Block RAM of FPGA
45	1.2	✓	●	[100]	
32	0.48		●	[75]	
			Bulk-Fin		
14	1.12		▲	[75]	

* L_T was determined experimentally. The other values were obtained by theory or simulation (see the "Note" column: "SPICE" indicates that the analysis used a circuit simulator, while "TCAD" indicates a numerical device simulator).
♭ Some papers reported a range of L_T values. For those cases, the second column lists a representative value, while "Note" column gives the range, denoted by "R:".

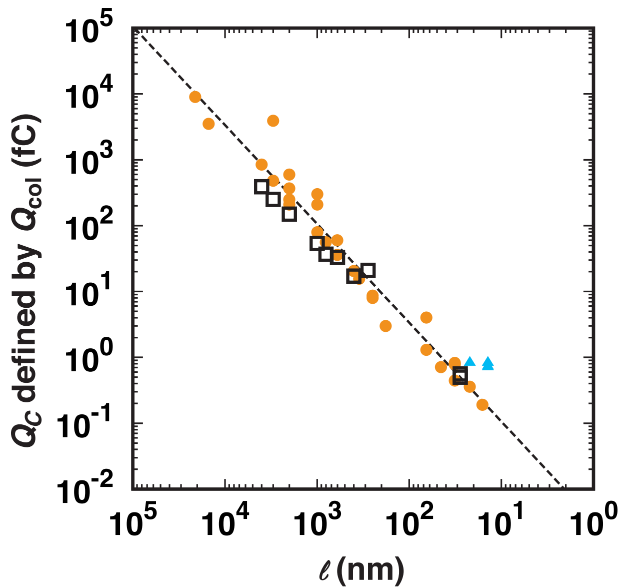
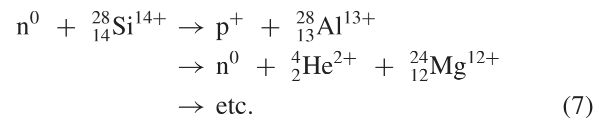


Fig. 7. Copy of Fig. 4 but with Q_C measured only in terms of $Q_{\rm col}$. The line represents the trend reported by Pickel [7].

their study was based on an FF fabricated in a bipolar-junction-transistor (BJT) process, not on a CMOS SRAM. Note that one would obtain a similar result when using 30 MeVcm^2/mg for comparison instead of 100 MeVcm^2/mg. Here, 30 MeVcm^2/mg corresponds to the maximum L produced by Fe in GCRs and is widely used as a GCR reference because of its abundance [77].

Next, Fig. 8 confirms that device scaling to the submicrometer generations results in $L_T < L_2$ or 16 MeVcm^2/mg, which is the maximum value of L produced by nuclear reactions between Si and space protons [112] or terrestrial neutrons [113]. For their small charge and Coulomb barrier, high-energy protons and neutrons can collide with nuclei in device materials and produce various secondary charged particles, as in the following example [114]:[2]



$$\begin{aligned} \mathrm{n}^0 + {}^{28}_{14}\mathrm{Si}^{14+} &\rightarrow \mathrm{p}^+ + {}^{28}_{13}\mathrm{Al}^{13+} \\ &\rightarrow \mathrm{n}^0 + {}^{4}_{2}\mathrm{He}^{2+} + {}^{24}_{12}\mathrm{Mg}^{12+} \\ &\rightarrow \text{etc.} \end{aligned} \tag{7}$$

The resultant secondary ions such as Al^{13+} then deposit charge along their tracks through ionization, as with GCRs. The year axis suggests that the concern for indirect ionization has been serious since the late 1980s, which correspond to the years when a team of International Business Machines Corporation (IBM) conducted an extensive study on SEEs

[2]The author of the present study added atomic and charge numbers to the original expressions for clarity.

TABLE VIII
SEU L_T VALUES COLLECTED FROM THE LITERATURE FOR THE SOI STRUCTURES (SEE TABLE VII FOR BULK)

l (nm)	L_T (MeVcm^2/mg)	Exp.*	Structure	Reference	Note♭		
			SOI-Planar		d_{SOI} (nm)	d_{BOX} (nm)	
5000	40	✓	□	[64]	500		
4000	38	✓	□	[76]	550		
4000	49.2	✓	□	[77]	500		
3600	260	✓	□	[14, Table II]	530		R: > 260 MeVcm^2/mg
3600	245	✓	□	[14, Table II]	530		
3600	152	✓	□	[14, Table II]	530		
3600	98	✓	□	[14, Table II]	530		
3600	95	✓	□	[14, Table II]	530		
2900	37	✓	□	[14, Table II]	530		
2700	37	✓	□	[14, Table II]	530		
2500	25	✓	□	[101, Fig. 4]	550	500	
2000	24	✓	□	[77]	500		l = 2500 nm? [4]
1800	30	✓	□	[14, Table II]	530		
1200	46	✓	□	[102, Table II]	150		
800	17	✓	□	[102, Table II]	1200		
500	80	✓	□	[78]	85	400	
500	15	✓	□	[102, Table II]	150		R: < 15 MeVcm^2/mg
500	9.21	✓	□	[103]	260	130	
350	5.87	✓	□	[103]	260	130	
350	7	✓	□	[95]	250	200	
250	3.7	✓	□	[98]	150	400	
200	3.6	✓	□	[104]	50	100	
150	3.5	✓	□	[105]	150		
90	0.46	✓	□	[106]	70	145	l, d_{SOI}, and d_{BOX} from [107]
65	0.5	✓	□	[108, Fig. 1]			
45	0.5	✓	□	[108, Fig. 1]			
65	2		□ "a"	[109, Fig. 19]	10	12	TCAD
28	15.5		□ "b"	[110, Table III]	7	25	TCAD
28	3.5		□ "b"	[83]	7	25	TCAD; R: 3.5 or 7 MeVcm^2/mg
28	1.5	✓	□ "b"	[111, Fig. 3]	7	25	
			SOI-Fin (Not reported)				

* L_T was determined experimentally. The other values were obtained by theory or simulation (see the "Note" column: "SPICE" indicates that the analysis used a circuit simulator, while "TCAD" indicates a numerical device simulator).
♭ Some papers reported a range of L_T values. For those cases, the second column lists a representative value, while "Note" column gives the range, denoted by "R:".

caused by terrestrial neutrons and other cosmic rays [115]. Today's IC makers thus need knowledge of astronomy, such as solar activity, to assure the reliability of their products, even if they are producing devices only for terrestrial use. This is because terrestrial neutrons are products of reactions between GCRs and Earth's atmosphere, and their abundance depends on solar activity and galactic events. IC makers further need knowledge of their products at the atomic level. Evaluating the risk of this indirect ionization process becomes more complex with the introduction of new elements into devices. In this regard, the impacts of tungsten (W) are often discussed [116]–[119]. In addition to its proximity to transistors (W is used to make the plug connecting the source/drain region to a metal wire), it has a nuclear-reaction cross section larger than that of Si, and it generates secondary ions heavier than Si because of its high atomic number ($Z = 74$). The use of W thus increases the frequency of secondary ion strikes and also increases L, which may exceed L_2 and reach 30 MeVcm^2/mg [120, Fig. 6]. Even the residue of gases during fabrication cannot be ignored. Studies [121]–[123] suggest that ^{10}B atoms from the B_2H_6 gas used for W-plug formation remain inside final products and cause SEUs through a fission process, in which a ^{10}B nucleus absorbs a low-energy (thermal) neutron and breaks into two charged particles, that is, ^{4}He and ^{7}Li nuclei [124]. Note that heavy ions with energy sufficiently high to overcome the Coulomb barrier can collide and induce the indirect ionization process [118], [125], [126].

Fig. 8 also shows that further scaling results in $L_T < L_3$ or 0.54 MeVcm^2/mg, which corresponds to the maximum value of L produced by protons though direct ionization. The

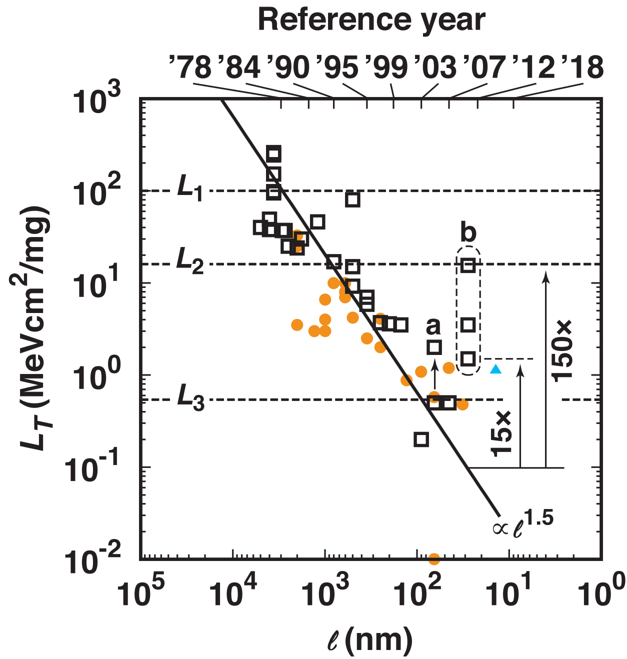


Fig. 8. Evolution of L_T. The solid line is an eye guide, given by $L_T = 20\,(l/1000)^{1.5}$. The dashed lines represent references for comparison: $L_1 = 100$ MeVcm^2/mg, the maximum value of L produced by GCRs through direct ionization in Si; $L_2 = 16$ MeVcm^2/mg, the maximum value of L produced by nuclear reactions between Si and protons or neutrons; $L_3 = 0.54$ MeVcm^2/mg, the maximum value of L produced by protons through direct ionization in Si.

proton charge is small but no longer negligible in sub-100-nm SRAMs dating from the 21st century onward. In fact, since this SEU was experimentally demonstrated for the first time in a 65-nm SRAM in 2007 [127], it has been observed in succeeding generations [108], [128], [129]. Moreover, $L_T < L_3$ induces SEUs due to positive muons in the Earth's atmosphere, which have as much charge as protons do. In fact, 31 years after the prediction by Ziegler and Lanford in 1979 [130], Sierawski *et al.* [131] tested Bulk SRAMs with $l \leq 65$ nm and presented the first experimental evidence of the positive-muon-induced SEUs. It is now imperative to evaluate the risk of SEUs due to muons, including negative ones [132], [133], for terrestrial applications, although the risk has so far been claimed as insignificant because of the overwhelming frequency of neutron SEUs [33], [74].

A close look at Fig. 8 indicates that the tested SOI SRAMs have higher L_T, in general, than their Bulk counterparts do

$$L_{T(\mathrm{SOI})} \geq L_{T(\mathrm{Bulk})}. \tag{8}$$

This is opposite to the finding and common belief for Q_C (note that Q_C is hereafter defined by Q_{col})

$$Q_{C(\mathrm{SOI})} \leq Q_{C(\mathrm{Bulk})}. \tag{9}$$

The following paragraph discusses this reversal of order.

Regardless of the structure category (SOI or Bulk), the SEU criterion is widely given as $Q_{\mathrm{col}} \geq Q_C$. Then, Q_{col} can be expressed as

$$Q_{\mathrm{col}} = \eta Q_{\mathrm{dep}} \tag{10}$$

where typically

$$\eta = \begin{cases} \alpha \leq 1, & \text{for Bulk} \quad (11a) \\ \beta \geq 1, & \text{for SOI.} \quad (11b) \end{cases}$$

Here, α and β represent the charge collection efficiency and parasitic BJT amplification factor, respectively. Assuming a certain region of Si, called a sensitive volume (SV), Q_{dep} can be estimated from Ls, where L is given in a charge-based unit (e.g., fC/nm) and s represents a chord length, that is, the travel distance of an incident radiation particle across the SV [134]. Note that here L is assumed to be constant along s to simplify the integration to obtain Q_{dep}. As a result, the two critical and threshold parameters can be linked as follows:

$$Q_C = \eta L_T s. \tag{12}$$

Because both η and L_T are larger for SOI SRAMs than for Bulk SRAMs, this equation necessitates $s_{(\mathrm{SOI})} \leq s_{(\mathrm{Bulk})}$ to establish the reversed order for Q_C. In fact, such superiority of SOI over a Bulk substrate in the context of s is often highlighted [35]. As illustrated in Fig. 2(a), SOI substrates rely on BOX to separate transistors electrically from the bottom substrate. This separation makes the SV physically restricted by d_{SOI}, which is typically on the order of 10 (FD) or 100 nm (PD). As illustrated in Fig. 2(b), on the other hand, a Bulk substrate has an open-bottom structure, which can collect charge deposited in the substrate's deep region. This collection process is associated with the dramatic stretch-out of the electric field profile, which is called field funneling. It works as if a funnel were drawing charge from the deep region. As a result, Bulk SVs typically range over 100–10 000 nm in depth, ~10× deeper than SOI SVs.

Precise description of field funneling requires a set of differential equations for high-level injection, for which an exact solution cannot be obtained analytically. Hence, researchers often use an *a posteriori* approach to determine s from measured Q_{col} and L via $s = Q_{\mathrm{col}}/L$; the resultant s is called the funnel length [135], [136].[3] Similarly, this study estimated the funnel length from L_T/Q_C. L_T was obtained directly from Table VII and Q_C from $Q_C = 2(C_g + C_p)V_{\mathrm{DD}}$ in Fig. 5. For comparison, this study also calculated two theoretical reference values, which are related to d_{DR}, the length of the depletion region (DR) that is originally established in a p-n junction. Assuming a one-sided abrupt p-n junction in a p-type Si substrate, this study obtained d_{DR} from the textbook formula [137]

$$d_{\mathrm{DR}} = \sqrt{\frac{2\varepsilon_{\mathrm{Si}}}{qN}(\phi_b + V_{\mathrm{DD}})}. \tag{13}$$

Here, $\varepsilon_{\mathrm{Si}}$ and N represent the substrate's permittivity and carrier density, respectively, while ϕ_b denotes the built-in

[3]This estimation relies on $\eta\ (= \alpha) = 1$ in (11a), and this unity assumption is commonly used for α. This study explicitly uses (11a) for ease of comparison between the Bulk and SOI cases by providing a universal expression for both structures. Building the universal expression took into account the case of $\alpha < 0$ that is used in a multiple-SV model [97], in which an SV is modeled with a combination of arbitrary regions. Here, Q_{coll} is given by $\sum_i \alpha_i L_i s_i$, where i represents the index of each region, and $\sum_i \alpha = 1$.

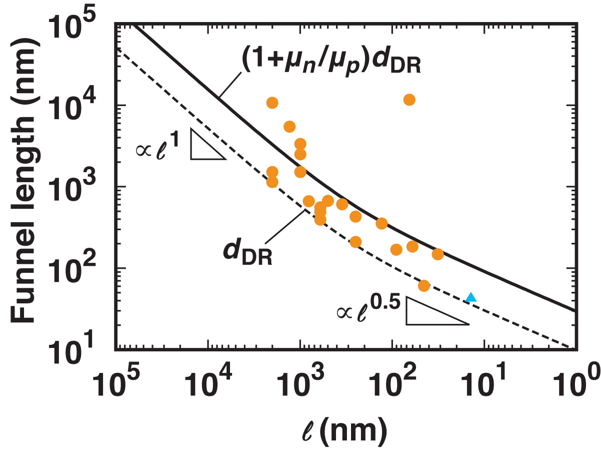


Fig. 9. Estimated funnel lengths of Bulk SRAMs. Estimations from Q_C/L_T (symbols) are compared with the depletion length for a one-sided abrupt junction (d_{DR}) and Hu's funnel length model giving $(1+\mu_n/\mu_p)d_{\mathrm{DR}}$. The two triangles show reference slopes for the dependence l.

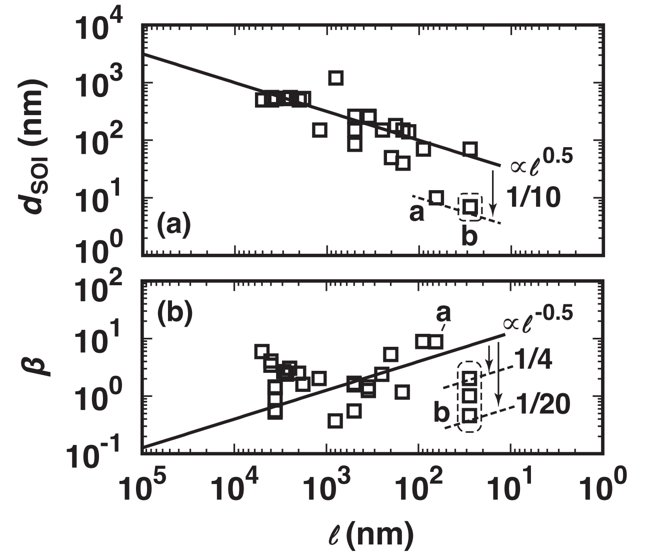


Fig. 10. (a) d_{SOI} values collected from the literature. The solid line is an eye guide, given by $d_{\mathrm{SOI}} = 10l^{0.5}$. (b) β values calculated from the literature data. The solid line is an eye guide, given by $\beta = 40l^{-0.5}$.

potential of the p-n junction in question. Here ϕ_b was also theoretically estimated from

$$\phi_b = 2\frac{kT}{q}\ln\left(\frac{N}{n_i}\right) \tag{14}$$

where k, T, and n_i denote the Boltzmann constant, temperature, and the intrinsic carrier density, respectively. Regardless of the type of channel structure (Planar or Fin), this study simply used $N = (5\times10^{15})\cdot(5000/l)$ [cm^{-3}], which was extracted from [3]. The other reference value was the funnel length modeled by Hu [138], given by $\left(1+\mu_n/\mu_p\right)d_{\mathrm{DR}}$ where μ_n and μ_p denote the respective mobilities of electrons and holes in the substrate. This study used a constant mobility ratio across generations, that is, $\mu_n/\mu_p = 980/410$ [138], after confirming that the ratio remains almost intact (within a factor of ~2) even when considering the mobility dependence on N, at least in the range examined in this study. As shown in Fig. 9, this attempt found that the *a posteriori* funnel length obtained from the literature data (Q_C/L_T) decreased along the evolution of the two reference values related to d_{DR}. The funnel lengths obtained from the literature data are clearly longer than d_{DR}. This result confirms that the tested Bulk SRAMs underwent field funneling and collected charge from the region deeper than d_{DR}. Fig. 9 also shows that Hu's model overall describes the upper bound of the funnel lengths obtained from the literature data (particularly for $l \lesssim 1000$ nm). This agreement between the upper bound and Hu's model is interesting. Some studies have suggested that Hu's model underestimates the funnel length for high-L ions because of the lack of an additional charge component due to diffusion [139]. Hu derived his model by assuming a strike of a low-L ion, or more specifically an α-ray, that is, $L \leq 1.5$ MeVcm^2/mg. As seen in Table VII, however, L_T values in the literature are mostly larger than this value. Despite such underestimation, Hu's model has provided the upper bound in this analysis. This is probably due to the influence of τ in (2). Both the discussion in [139] and that of Hu are based on a constant-biased discrete p-n diode. Without any time constraints, they both counted charge as long as charge flows. In contrast, the funnel length estimated from Q_C/L_T is a result of the circuit response, with charge counted only for the duration of τ [140]. The diffusion process for additional charge could be too slow in comparison with τ, thus being insignificant in relation to Q_C and the resultant funnel length. In this regard, Fig. 9 indicates that Hu's model can underestimate funnel lengths in the early micrometer-scale generations ($l \gtrsim 1000$ nm). In these generations, the responses of the tested Bulk SRAMs could be slow, and their τ values could be comparable to the time for the total charge collection.

Moreover, Fig. 9 shows that the funnel length of the tested Bulk SRAMs is around ~100 nm when $l \lesssim 100$ nm. This suggests that the superiority of SOI over Bulk in the context of s can no longer always be expected. In fact, some SOI SRAMs exhibit L_T lower than that of Bulk SRAMs when $l \lesssim 100$ nm (Fig. 8). Furthermore, Fig. 9 indicates that the funnel length of the tested Bulk-Fin SRAM was shorter than would be predicted by Hu's model. Although further investigation is needed because of the small amount of data, this finding seemingly agrees with the narrow-fin effect [38], [39]: fin width reduction narrows the path from a transistor to its substrate and restricts charge collection from the substrate's deep region.

Similarly, this paragraph analyzes the L_T values of SOI-Planar SRAMs, but in terms of β, because s of SOI devices is explicitly given by d_{SOI}, unlike their Bulk counterparts. Fig. 10(a) shows the d_{SOI} data collected from the literature. Overall, d_{SOI} exhibits a monotonically decreasing trend, which is roughly proportional to $l^{0.5}$. This slope parameter of 0.5 was mathematically determined from $Q_C = L_T d_{\mathrm{SOI}}$, with Q_C defined by Q_{dep}, not by Q_{col}. To satisfy this relationship, the parameter must be 0.5 because, as shown in Figs. 4 and 8, Q_C and L_T are proportional to l^2 and $l^{1.5}$, respectively.

Fig. 10(a) also highlights that the two recent generations labeled "a" and "b" attained a large ($\sim 1/10$) reduction in d_{SOI}. The increase in L_T observed in Fig. 8 is attributed to this d_{SOI} reduction. The factor of $1/10$ is seemingly too small, however, to explain the large (15–150×) L_T increase at the latest node, "b", although this large increase might be an artifact because it is measured with respect to the solid line or an extrapolation of the $l^{1.5}$ trend (Fig. 8). Moreover, the L_T variations observed in the node "b" cannot be explained by the d_{SOI} reduction because the three cases examined here all rely on the same d_{SOI}. On the other hand, Fig. 10(b) shows β values calculated from (12) by combining the collected data (L_T and d_{SOI}) and Pickel's $l^{1.5}$ trend for Q_C as defined by Q_{col}. An increasing trend is evident for β, roughly conforming to $l^{-0.5}$, where the exponent of -0.5 was mathematically deduced as with d_{SOI}. The node "b" departs, however, from this trend and demonstrates a large (1/4–1/20×) reduction. This reduction in β could cause the dramatic L_T increase in concert with the reduction in d_{SOI}.

To seek the physical mechanism behind this β reduction, this paragraph further analyzes β by using a model developed by Musseau *et al.* [141][4]:

$$\beta = c\frac{1+0.65w}{l\sqrt{L_T d_{\mathrm{SOI}}}} + 1 \tag{15}$$

where c is a technology-independent parameter, assumed here to have a constant value of 3. Interestingly, as shown in Fig. 11, this model reproduces the $l^{-0.5}$ trend but not the reduction at "b." This discrepancy suggests that β is influenced by a parameter other than those in the model. In this regard, Fig. 12 indicates that the two generations in question, "a" and "b," also achieved a significant reduction in d_{BOX}. The fact that $d_{\mathrm{BOX}} \approx d_{\mathrm{SOI}} \approx 10$ nm suggests that the transistors in those generations operate in a double-gate mode. In such a mode, the body potential is tightly controlled from both the top metal gate and the bottom Si gate (substrate), with the latter fixed at a certain voltage such as 0 V. As seen from its definition, β quantifies the parasitic BJT amplification. Particle radiation provides charge, and the resultant majority carriers can accumulate in the body region, which electrically floats because of the presence of BOX. This accumulation can change the body potential and turn on a parasitic BJT that inherently consists of the source–body–drain connection in the transistor. As a result, the drain terminal collects not only charge created by radiation but also charge injected from the source. Hence, how large β is strongly depends on how much the body floats. In this regard, double-gate transistors are known to have a fairly stable body region because of the tight electrical connection to the top and bottom gates [142]. The reduction in β observed at the node "b" in Fig. 10(b) could reflect this double-gate feature because of d_{BOX} and d_{SOI} both scaling down to 10 nm. Of course, the cause of the variations in β must be examined in the future. Interestingly, Fig. 10(b) also indicates that the node "a" does not receive the benefit of the double-gate mode, despite its thin d_{SOI} and d_{BOX}. Further analysis of the differences between generations "a" and "b" would help locate the threshold at which the double-gate feature takes effect.

[4]The second term consisting of 1 on the right-hand side indicates the difference in the definitions of β between their study and the present study. They defined $Q_{\mathrm{col}} = (1+\beta)Q_{\mathrm{dep}}$, which is also widely used.

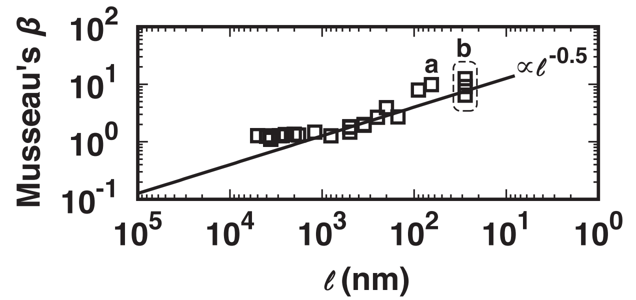


Fig. 11. β calculated from a model developed by Musseau *et al.* (see text). The solid line is the same eye guide as in Fig. 10(b).

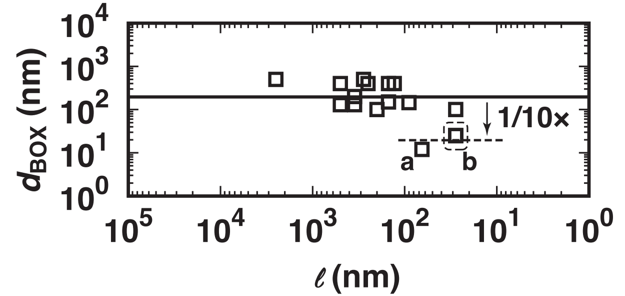


Fig. 12. d_{BOX} values collected from the literature. The solid line is an eye guide, given by $d_{\mathrm{BOX}} = 200$.

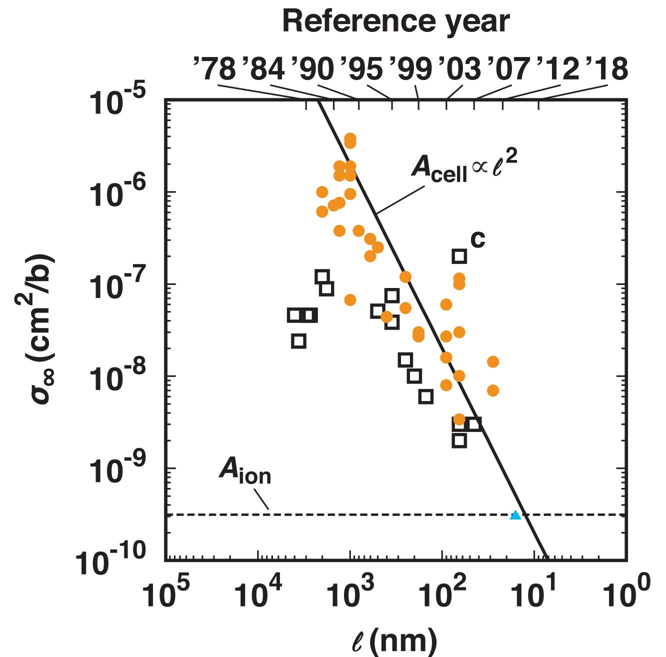


Fig. 13. σ_∞ values collected from the literature. The solid line represents the evolution of the SRAM cell area A_{cell} (see the text). The dashed line represents the typical area of an ion track (A_{ion}), as estimated from πr^2 with $r = 100$ nm.

C. SRAM σ_∞

Tables IX and X list σ_∞ values collected from the literature, while Fig. 13 shows how this parameter has evolved.

TABLE IX
SEU σ_∞ VALUES COLLECTED FROM THE LITERATURE FOR THE BULK STRUCTURES (SEE TABLE X FOR SOI)

l (nm)	σ_∞ (cm^2/b)‡	Exp.*	Structure	Reference	Note♭
			Bulk-Planar		
2000	1×10^{-6}	✓	•	[66, Fig. 4]	l from [67]
2000	6.1×10^{-7}	✓	•	[77, Fig. 1]	C
1500	71×10^{-8}	✓	•	[69]	R: 71 ± 18 ($\times10^{-8}$ cm^2/b) Visually quantified with a scanning ion microprobe
1300	3.8×10^{-7}	✓	•	[93, Table 1]	C; NMOS cell
1300	7.6×10^{-7}	✓	•	[93, Table 1]	C; NMOS cell
1300	1.5×10^{-6}	✓	•	[93, Table 1]	C; NMOS cell
1300	1.9×10^{-6}	✓	•	[93, Table 1]	C; NMOS cell
1000	3.8×10^{-6}	✓	•	[93, Table 1]	C; NMOS cell
1000	3.4×10^{-6}	✓	•	[93, Table 1]	C; NMOS cell
1000	1.5×10^{-6}	✓	•	[93, Table 1]	C; NMOS cell
1000	6.7×10^{-8}	✓	•	[93, Table 1]	C; NMOS cell
1000	1.9×10^{-6}	✓	•	[93, Table 1]	C; NMOS cell
1000	9.5×10^{-7}	✓	•	[93, Table 1]	C; NMOS cell
800	3.8×10^{-7}	✓	•	[93, Table 1]	C
600	3.1×10^{-7}	✓	•	[95, Fig. 3]	C
600	2×10^{-7}	✓	•	[143, Fig. 5]	
180	3×10^{-8}	✓	•	[143, Fig. 7]	
400	4.4×10^{-8}	✓	•	[117, Fig. 2]	
250	1.2×10^{-7}	✓	•	[98]	
250	5.5×10^{-8}	✓	•	[97]	
90	2.7×10^{-8}	✓	•	[144, Fig. 2]	R: 1.3–4.0 ($\times10^{-8}$ cm^2/b)
65	1.0×10^{-8}	✓	•	[145, Fig. 5]	R: 0.8–1.2 ($\times10^{-8}$ cm^2/b)
65	3×10^{-8}	✓	•	[73, Fig. 5]	
180	2.7×10^{-8}	✓	•	[32]	R: 2.5–3 ($\times10^{-8}$ cm^2/b)
90	6×10^{-8}	✓	•	[32, Fig. 11]	
65	1×10^{-7}	✓	•	[32, Fig. 12]	
65	1.15×10^{-7}	✓	•	[99]	Block RAM of FPGA
500	2.5×10^{-7}	✓	•	[146]	Unit corrected by consulting [147]
90	1.6×10^{-8}	✓	•	[146]	Configuration memory of FPGA
65	3.4×10^{-9}	✓	•	[146]	
90	8×10^{-9}	✓	•	[148, Fig. 2]	
28	1.43×10^{-8}	✓	•	[149, Fig. 1]	Configuration memory of FPGA
28	7×10^{-9}		•	[150, Fig. 6]	Block RAM of FPGA
			Bulk-Fin		
16	3×10^{-10}	✓	▲	[151, Fig. 2]	

‡ Units were converted to cm^2/b when they were given in a different format such as cm^2/chip, assuming prefixes based on powers of two, e.g., "k" denoting 2^{10} [152]. The "Note" column indicates such cases by "C."
* σ_∞ was determined experimentally. The other values were obtained by theory or simulation.
♭ Some papers reported a range of σ_∞ values. For those cases, the second column lists a representative value, while the "Note" column gives the range, denoted by "R:".

Regardless of the structure category, σ_∞ decreases roughly along the solid line A_{cell}, which depends on l^2. This line shows the evolution of the area of SRAM cells and was extracted from Intel data [154]–[159], shown in Fig. 14.

Detailed investigation indicates an upper bound ($\sigma_\infty \lesssim A_{\text{cell}}$) in early generations ($l \gtrsim 100$ nm), but later this bound disappears. This disappearance is manifest only in Bulk-Planar SRAMs, except for the SOI case denoted by "c." Because of their open-bottom structure, Bulk transistors are connected to each other thorough the substrate. They can share the influence of charge deposited by a single strike of particle radiation, thus exhibiting simultaneous upsets. Such a single-strike-induced multiupsets phenomenon is called a multicell upset (MCU).[5] MCUs are known to be particularly serious in recent Bulk SRAMs that rely on a triple-well structure [96], [162]–[166].

In this structure, illustrated in Fig. 15, the surface of a Si substrate is processed to produce a stripe pattern of narrow p- and n-wells, both of which are supported by a large plate-like

[5] A similar term, multibit upset (MBU), is also used. Historically, the term MBU was introduced earlier and used to describe this single-strike-induced multiupsets phenomenon (see [160], for example). Recently, MCU is widely used in this broad sense, while MBU is instead assigned to a specific MCU phenomenon that produces multiple upsets *in the same word*, which cannot be corrected by an error-correction code (ECC) [161].

TABLE X

SEU σ_∞ COLLECTED FROM THE LITERATURE FOR THE SOI STRUCTURES (SEE TABLE IX FOR BULK)

l (nm)	σ_∞ (cm²/b)‡	Exp.*	Structure	Reference	Note♭		
			SOI-Planar		d_{SOI} (nm)	d_{BOX} (nm)	
4000	4.6×10^{-8}	✓	□	[77, Fig. 2]	500		C
3600	2.4×10^{-8}	✓	□	[14, Table 3]	530		C; R: 1.8–3.1 ($\times10^{-8}$ cm²/b)
2900	4.6×10^{-8}	✓	□	[14, Table 3]	530		C; R: 3.7–5.5 ($\times10^{-8}$ cm²/b)
2700	4.6×10^{-8}	✓	□	[14, Table 3]	530		C; R: 3.7–5.5 ($\times10^{-8}$ cm²/b)
1800	8.9×10^{-8}	✓	□	[14, Table 3]	530		C; R: 7.3–10 ($\times10^{-8}$ cm²/b)
2000	1.2×10^{-7}	✓	□	[77, Fig. 3]	500		C
500	5.07×10^{-8}	✓	□	[103]	260	130	
350	3.86×10^{-8}	✓	□	[103]	260	130	
350	7.5×10^{-8}	✓	□	[95]	250	200	R: 7–8 ($\times10^{-8}$ cm²/b)
250	1.5×10^{-8}	✓	□	[98]	150	400	
200	1×10^{-8}	✓	□	[59, Fig. 1]	50	100	
150	6.0×10^{-9}	✓	□	[105]	150		
65	2×10^{-9}	✓	□	[153, Fig. 4]		10	
65	2×10^{-7}	✓	□ "c"	[153, Fig. 4]		10	Under a certain back-bias condition
65	3×10^{-9}	✓	□	[108, Fig. 1]			
45	3×10^{-9}	✓	□	[108, Fig. 1]			
			SOI-Fin (Not reported)				

‡ Units were converted to cm²/b when they were given in a different format such as cm²/chip, assuming prefixes based on powers of two, e.g., "k" denoting 2^{10} [152]. The "Note" column indicates such cases by "C."

* σ_∞ was determined experimentally. The other values were obtained by theory or simulation.

♭ Some papers reported a range of σ_∞ values. For those cases, the second column lists a representative value, while the "Note" column gives the range, denoted by "R:".

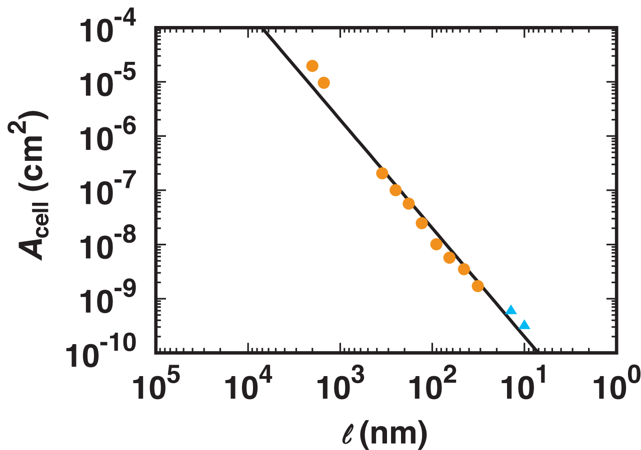


Fig. 14. Evolution of A_{cell} in Intel SRAMs. The line represents a best-fit curve, given by $A_{cell} = 2 \times 10^{-12}\, l^2$.

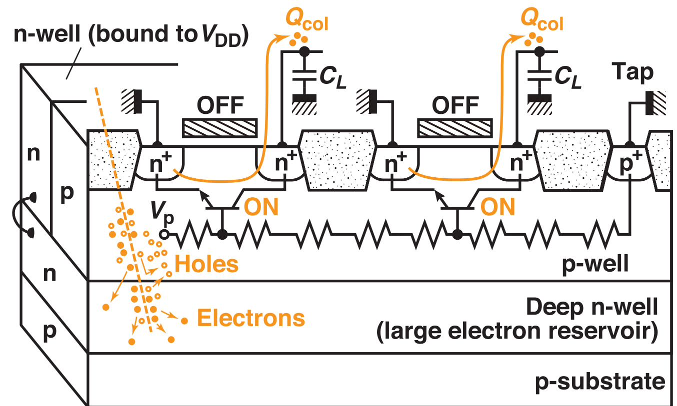


Fig. 15. Conceptual drawing of an MCU in a Bulk-Planar SRAM with a triple-well structure. As highlighted by the wire symbol on the left, the n-well is tightly connected to the large plate-type deep n-well with low resistance, making it electrically stable in comparison with its counterpart p-well.

deep n-well. The potential of each well is fixed by well contacts, typically called taps, that are formed at the far ends of the well strip. Deposition of charge inside a p-well can increase the potential around the struck region (V_p), because holes remain there for a while, typically 0.1–10 ns, until they diffuse into the taps [163], [166]. Electrons, on the other hand, quickly move out of the p-well to the side and bottom (deep) n-wells, which are electrically stable because of the deep n-well's large size. The resultant increase in V_p is distributed through the p-well. This potential perturbation turns on parasitic BJTs and leads to an MCU. The upper bound disappearance in Fig. 13 ($\sigma_\infty > A_{cell}$) probably reflects this MCU issue in triple-well Bulk SRAMs. In fact, one can note the following:

1) Fig. 13 indicates that crossing of the A_{cell} bound is obvious for $l \lesssim 100$ nm. This range of l agrees fairly well with the generations in which the triple-well MCU is serious, that is, $l \lesssim 150$ nm [162].

2) Fig. 13 shows that σ_∞ may become $10\times$ larger than A_{cell}. This multiplicity[6] agrees fairly well with that typically observed in triple-well MCU studies [163].

In contrast to Bulk SRAMs, as demonstrated in Fig. 13, SOI SRAMs continue to stay within the A_{cell} bound across generations, except for the value labeled by "c." This favorable restriction stems from the presence of BOX [167]. Because of the closed-bottom structure due to the BOX, transistors are electrically isolated from each other. Hence, SOI SRAMs rarely exhibit an MCU, and even when they do, its multiplicity is limited to only a few bits. In this regard, the exception at "c" is quite interesting; it demonstrates a multiplicity as high as 100, despite its SOI structure. As already seen in the β discussion, recent SOI generations use a very thin BOX layer ($d_{\text{BOX}} \approx 10$ nm). Some of them further rely on a triple-well structure, which is similar to that in Bulk case but not directly connected to the transistors, because it is formed underneath the BOX. This buried-well option is favorable for low power consumption, because it enables control of the transistors' threshold voltage (V_T) by feeding back-bias voltages through the capacitance coupling principle [168], [169]. The transistors are no longer completely isolated from each other however, and a potential perturbation in a well can thus spread among cells. The large MCU observed at "c" results from this adverse reaction with the buried-well option [153], [170]. Technology computer-aided design (TCAD) investigations [171], [172] have suggested that a careful design of the back-bias voltages would make it possible to take advantage of adaptive V_T control with a sufficiently reduced risk of MCUs.

Fig. 13 also shows that despite its Bulk structure, the tested Bulk-Fin SRAM had σ_∞ lower than A_{cell}, as with the conventional SOI SRAMs. Although a further study will be required because of the very limited amount of data here, this SOI-like response is possibly due to the narrow-fin effect already explained, which increases the transistor–substrate resistance and may disturb charge sharing through the substrate. Furthermore, the Bulk-Fin σ_∞ is as large as the reference value A_{ion}, which represents the typical area of the charge column, called the ion track, initially created along the path of particle radiation. This study estimated the typical area of the column as πr^2, with $r = 100$ nm [173]–[175] representing the track's radius. This agreement ($\sigma_\infty \approx A_{\text{ion}}$) suggests from a geometrical viewpoint that σ_∞ will no longer become smaller than A_{ion} even if A_{cell} is further decreased. All the SRAM SEU parameters investigated in this study (Q_C, L_T, and σ_∞) have revealed scaling trends with decreasing l. Among them, only σ_∞ benefits from the miniaturization: Its reduction favorably decreases the rate of SEUs. The finding that $\sigma_\infty \approx A_{\text{ion}}$ suggests, however, that this benefit of miniaturization may no longer apply in the future. Furthermore, SEU hardness assurance in this new era will need to deal with additional complex mechanisms associated with A_{ion} [175]–[177].

[6]The factor of 10 means that a single strike of particle radiation can upset 10 cells. In this regard, another σ metric is also used in MCU studies: the event cross section, obtained by dividing (1) by the multiplicity.

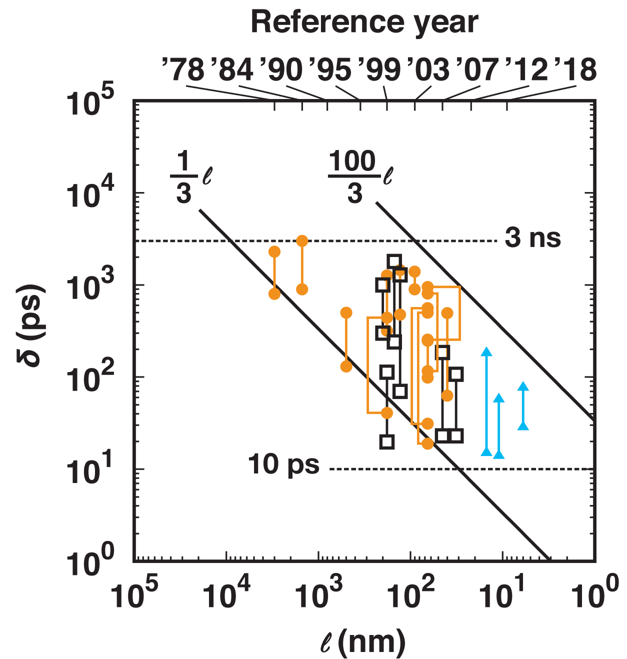


Fig. 16. Inverter δ values collected from the literature. The solid and dashed lines represent reference trends (see the text).

D. Inverter δ

Table XI compiles inverter δ values collected from the literature. Fig. 16 shows that δ decreases overall with l, roughly in proportion, but with a widespread at each l (along the vertical axis). This spread is attributed to various differences in factors such as L and the strike position, as well as the degree of broadening during propagation, as discussed later. Interestingly, Fig. 16 reveals that the spread ranges overall between $l/3$ and $100l/3$. Here, $l/3$ corresponds to the empirical rule that provides τ_{FO4}, the propagation delay of a fan-out of 4 (FO4) inverter [193], [194],[7] which is widely used in technology comparisons. This empirical rule appears to be applicable over a wide range of l, but possibly not when $\tau_{\text{FO4}} \lesssim 10$ ps, as shown in Fig. 17.

Regarding the lower bound ($\delta \gtrsim l/3$), it is expected to be spurious and artificially created by measurement systems. Measuring δ requires a dedicated on-chip circuit, because the drive currents of the logic gates inside ICs are too small to drive the input of an external measurement apparatus such as an oscilloscope. For this purpose, various circuits have been developed [179], [182], [185], [192], [204]–[206], and many of them rely on a time-to-digital converter (TDC), as conceptually illustrated in Fig. 18(a). In this example [204], a chain of target logic gates (inverters) is connected to the inputs of two TDCs. The chain works as an antenna that receives particle radiation and sends an SET to the TDCs. Each TDC then digitizes and records the SET as a bit string. Fig. 18(b) exemplifies the TDC circuitry, in which the SET propagates through an inverter chain (inverter delay line) and triggers FFs with its own edge,

[7]Ref. [193] is often cited, but its publication information is unavailable. It is expected that it was written before 1998, because a figure from [193] was also presented in [194].

TABLE XI
INVERTER δ VALUES COLLECTED FROM THE LITERATURE

	δ (ps)									
l (nm)	Min.	Max.	L (MeVcm^2/mg)	Chain♯	Exp.*	Structure	Reference	Note		
						Bulk-Planar				
3000	800	2300		✓		●	[178, Table I]	SPICE; Range from V_{DD}: 10–4 V		
1500	900	3000		✓	✓	●	[179]	Range from E_p: 85–179 pJ‡		
500	130	500	8.77–23.46			●	[180, Fig. 4]	SPICE; Inverter?		
180	41	442	3–30			●	[181, Fig. 2(a)]	TCAD		
180	319	1258	11.5–64	✓	✓	●	[182, Fig. 5]	Inverter?		
130	477	1440	9.8–59	✓	✓	●	[30, Fig. 1]			
90	900	1400	1.8–59	✓	✓	●	[30, Fig. 1]			
65	99	248	2.5–59	✓	✓	●	[30, Fig. 1]			
65	19	500	3.6–60	✓	✓	●	[183, Fig. 8]			
65	254	952	95	✓	✓	●	[184, Fig. 5]	Collected from DUT1		
65	116	807	0.57†	✓	✓	●	[185]			
65	31	560	3.2–37.3	✓	✓	●	[186, Fig. 5]	Before proton irradiation		
40	62.8	491	0.8–5			●	[187, Table 4]	SPICE. Range from V_{DD} and T as well as L		
						Bulk-Fin				
14/16	15	182	6–59	✓	✓	▲	[188, Fig. 5]	Collected from V_{DD} of 0.8 V		
11	14	57	5–35			▲	[189, Figs. 2&4]	TCAD		
6	28	77	5–35			▲	[189, Figs. 2&4]	TCAD		
						SOI-Planar		d_{SOI} (nm)	d_{BOX} (nm)	
200	300	1000	40–92	✓	✓	□	[190, Fig. 3]	50	100	
180	20	113	5–30			□	[181, Fig. 2(b)]	180		TCAD
150	240	1800	25	✓	✓	□	[191, Fig. 6]	40	400	Tier 1
130	70	1282		✓	✓	□	[192, Fig. 6]	140	400	E_p at 78 pJ‡
45	23	185	59	✓	✓	□	[36, Fig. 2]			
32	23	107	59	✓	✓	□	[36, Fig. 1]			
						SOI-Fin (Not reported)				

♯ δ was measured with a chain and was expected to be influenced by PIPB.
* δ was determined experimentally. The other values were obtained by theory or simulation (see the "Note" column: "SPICE" indicates that the analysis used a circuit simulator, while "TCAD" indicates a numerical device simulator).
† This experiment used α-rays from ^{241}Am; L was estimated by the author of the present study.
‡ These experiments used laser pulses; E_p denotes the pulse energy.

when arriving at node X. The measurement resolution is thus determined by the propagation delay of the delay unit, which typically consists of one or two inverters (see [179] for a one-inverter example). This resolution limit manifests itself as the lower bound in Fig. 16. Note that, although the delay unit usually uses an FO1 inverter, its actual delay is seemingly close to τ_{FO4} because of the two-inverter configuration and the additional load due to the FFs connected in parallel. Moreover, in terms of the lower bound, Fig. 16 indicates that δ in recent generations—in particular, for the Bulk-Fin cases—does not conform to this $l/3$ rule but remains at ~10 ps. This constant behavior is consistent with that implied for τ_{FO4} (Fig. 17), probably reflecting the speed penalty due to C_p, as already highlighted in Fig. 5.

As illustrated in Fig. 18(a), the target inverters form a chain to make a sufficiently large antenna for measurement. Hence, the δ observed in this chain-based system is, in essence, influenced by propagation-induced pulse broadening (PIPB) [62]: the SET becomes shorter or longer than its original value while propagating through the chain. Some articles report δ after removing the influence of PIPB [30], while others do not. This study simply collected and used data without any distinctions between δ values before and after propagation. The upper bound revealed in Fig. 16 thus suggests that even if δ becomes longer as a result of PIPB, it does not exceed $100l/3$, in general. The chain for δ measurement typically consists of 10–100 inverters, which is equal to or larger than the typical number of logic gates in a pipeline of microprocessors [207, Fig. 1]. This implies that the value of $100l/3$ can potentially provide a crude reference for estimating the risk of SET errors in microprocessors in a worst case scenario. Moreover, in terms of the maximum value of δ, Fig. 16 shows that δ departs from the upper bound of $100l/3$ when l becomes long (roughly $l \gtrsim 1000$ nm) and instead suppresses its extension at

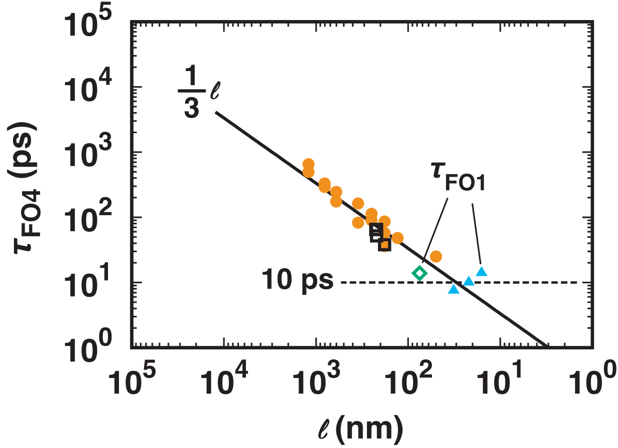


Fig. 17. Evolution of τ_{FO4} as collected from the literature, for Bulk-Planar [193], [195]–[199], Bulk-Fin [200]–[202], SOI-Planar [196], and SOI-Fin [203] devices. To increase the amount of data for the Fin case, the figure also shows a similar delay, but measured for inverters with fan-out of 1 (FO1). In essence, $\tau_{FO4} > \tau_{FO1}$ for the same process.

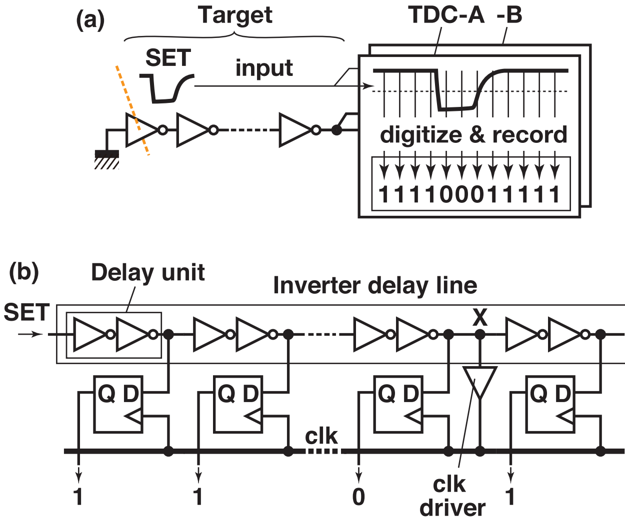


Fig. 18. Example of δ measurement circuitry (after [204] ©The Electrochemical Society. Reproduced by permission of the Institute of Physics (IOP) Publishing. All rights reserved). (a) Chain of target logic gates is connected to TDCs fabricated on the same chip. (b) TDC circuitry usually consists of an inverter delay line and FFs with a self-triggering mechanism. Note that TDC itself can receive particle radiation and generate an SET. To exclude such false signals, several techniques are used, such as redundant TDCs as in this example.

3 ns. Interestingly, this saturation value of 3 ns agrees with the typical duration of transient currents observed in discrete Si p-n and p-i-n diodes biased at a constant voltage [208]–[211]. In these early generations, δ might be determined mainly by the response of a discrete diode rather than that of the circuit, as implied in the discussion of the discrepancy between the estimated funnel length and Hu's model in Fig. 9.

As explained in Section II-B2, an SET is hazardous when it overwrites the bit information stored in FFs. The probability of this overwrite process is known to be proportional to δ/T_{clk} [61], where T_{clk} denotes the clock period. Therefore, this study extracted T_{clk} from a microprocessor history, shown in Fig. 19 [212], and compared it with δ, as shown in Fig. 20. This comparison shows that δ first exceeded T_{clk} when l

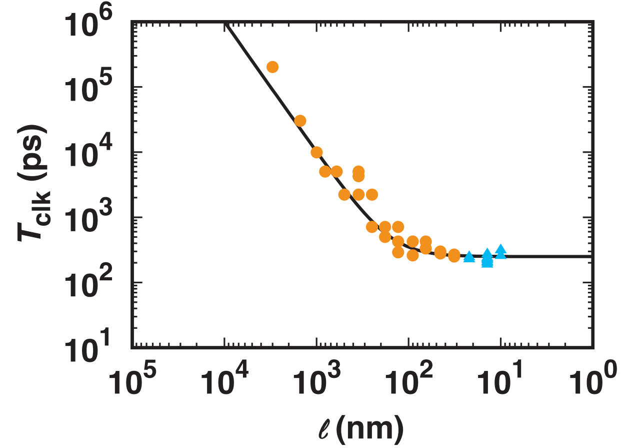


Fig. 19. Evolution of T_{clk} in Intel microprocessors. This study obtained T_{clk} as $1/f_{clk}$, where f_{clk} denotes the clock frequency, as compiled in [212]. The solid line is an eye guide, given by $T_{clk} = 0.01l^2 + 250$.

reached ~200 nm. This agrees with a common view that SETs became common in digital ICs around 2000 [60], when microprocessors achieved gigahertz operation; indeed, Intel processors achieved that speed at $l = 250$ nm.[8] Fig. 20 also reveals that δ again became shorter than T_{clk} when l reached ~20 nm, that is, in the Fin era. Although further investigations will be required, because the Fin data here consists of results from nonchain tests and are thus not influenced by PIPB, this finding suggests an advantage of Fin over Bulk technologies with respect to SETs. In fact, several studies have already demonstrated that the introduction of Fin technology results in a large reduction (~1/10) in the rates of SET-induced errors [38], [216]. Fig. 20 also shows a similar recovery in SOI-Planar devices, with $\delta \lesssim T_{clk}$ again when $l \lesssim 45$ nm. This recovery could be due to a favorable reduction in a floating-body effect, or more specifically, a history effect, which is a major source of PIPB in SOI devices [217].

This last paragraph discusses SEUs again but in terms of SETs. Fig. 5 compared Q_C with $2C_L V_{DD}$, which was obtained by transforming (2). Mathematically, (2) can also be transformed into a function of $I_{ON}\tau$. As already mentioned, τ represents the time required for a radiation-induced voltage drop to be latched after propagating through an inverter loop. On the basis of the similarity in definition between τ and the lower bound of δ revealed in Fig. 16, which corresponds to the pulse duration that can propagate through an inverter chain, this study assumed that

$$Q_C \approx I_{ON}\delta_C \tag{16}$$

where δ_C denotes the lower bound of δ. Furthermore, the analysis in Fig. 16 yielded

$$\delta_C \approx \tau_{FO4} = \begin{cases} l/3, & \text{for } l \geq 30 \text{ nm;} \\ 10, & \text{for } l < 30 \text{ nm.} \end{cases} \tag{17}$$

[8]Although this sentence and Table I might give the impression that SET is a new issue, it has a long history, dating back to 1980s. SET was first predicted by simulation in 1983 [178] (see also Table XI) and soon later confirmed by experiment [213], [214]. Note that SET was called single-event disturb (SED) errors in some articles at that time [215]. See [60] for further details about the history.

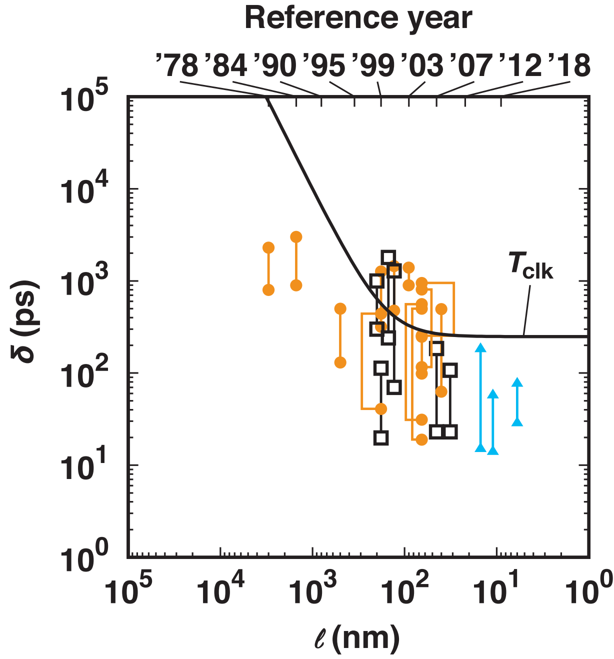


Fig. 20. Comparison of δ and $T_{\rm clk}$.

From Fig. 21, $I_{\rm ON}$ was modeled as

$$I_{\rm ON} = \begin{cases} 0.3w, & \text{for } l \geq 90 \text{ nm;} \\ 1w, & \text{for } l < 90 \text{ nm.} \end{cases} \tag{18}$$

Note that $I_{\rm ON}$ is usually normalized by w in the literature. Fig. 22 shows Q_C values estimated from (16)–(18), demonstrating that the above estimation well describes the Q_C evolution across generations. This δ_C-based estimation can potentially clear a hurdle in the capacitance-based approach. The latter approach requires C_p, which is hardly seen in the literature, and its extraction is often difficult, whereas δ_C inherently reflects it. Although measuring δ_C is also somewhat difficult, it can be estimated from $\tau_{\rm FO4}$, which can be measured with a simple inverter chain, that is, a ring oscillator.

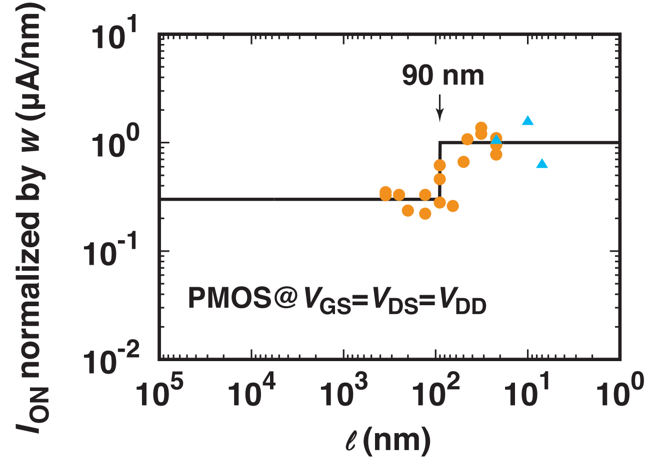


Fig. 21. PMOS $I_{\rm ON}/w$ values collected from the literature, for Bulk-Planar [156], [157], [218]–[227] and Bulk-Fin [158], [159], [228] devices. Note that the hump at $l = 90$ nm represents the result of mobility enhancement due to strain engineering and other techniques.

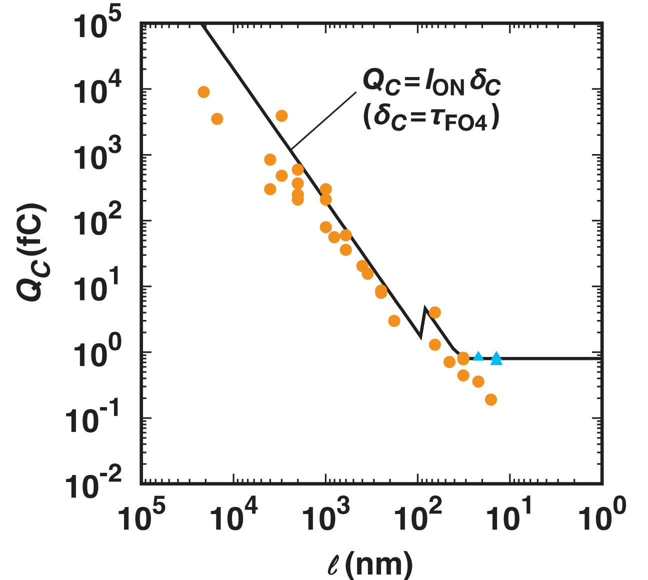


Fig. 22. Comparison of Q_C between the collected data and estimations, for the Bulk case only.

IV. Conclusion

This study collected 179 sets of SEE data from the literature and analyzed them in terms of device scaling or the feature size given by l, integrating the results with knowledge from more than 200 articles. This exploration gave the following conclusions:

1) The SEU critical charge (Q_C) of SRAMs constantly decreases with l, over almost five orders of magnitude, but the trend recently halts at ~0.5 fC. The Q_C values for SOI- and Bulk-Planar SRAMs depend on different scaling trends. The former case follows Petersen's l^2 trend, whereas the latter case follows Pickel's $l^{1.5}$.
   a) The revealed difference in Q_C trends between SOI- and Bulk-Planar SRAMs arises from the difference in the definition of Q_C. Use of the same Q_C definition makes the trend difference disappear, with Q_C converging on the same $l^{1.5}$ trend in both cases. On the surface, this disappearance contradicts the common view that SOI SRAMs have smaller Q_C than their Bulk counterparts do, but this inconsistency is seemingly due to a masking effect of the data distribution's spread.
   b) The revealed $l^{1.5}$ trend is well explained by the product of the C_L and the power supply voltage ($V_{\rm DD}$), that is, $2C_L V_{\rm DD}$. This product reveals the significant impact of the parasitic capacitance C_p on Q_C in the Bulk-Fin SRAMs. Bulk-Fin devices are known to have a relatively large C_p due inherently to their 3-D gate structures. This C_p degrades the speed of operation, but on the other hand, it favorably prevents Q_C reduction. Note that efforts have been made to decrease C_p to

boost the speed of Fin devices, but such efforts involve undesired Q_C degradation.

2) The SEU threshold LET (L_T) of SRAMs exhibits a scaling trend that is roughly proportional to $l^{1.5}$. For recent SOI-Planar SRAMs, however, L_T largely departs from the global trend, exhibiting a dramatic (150×) increase. A marginal difference in L_T between the examined structures is also observed: In general, SOI SRAMs have higher L_T than their Bulk counterparts do.
   a) The $l^{1.5}$ trend is useful for underlining the complexity of SEE mechanisms in the context of the variety of radiation phenomena, such as proton-induced direct ionization and neutron-induced indirect ionization.
   b) The L_T difference between SOI and Bulk SRAMs stems from the difference in charge collection between these structures:
      i) Bulk SRAMs rely on field funneling, which can collect charge from the deep region of a substrate. The revealed collection depth or funnel length is well described by Hu's model. That model also explains why some recent Bulk SRAMs ($l \lesssim$ 100 nm) exhibit L_T higher than that of their SOI counterparts. It also casts light on the narrow-fin effect, which can favorably restrict charge collection from the deep region.
      ii) Although the SOI SRAMs do not collect charge from the substrates because of the shielding effect of their BOX layer, they depend on the undesired charge enhancement effect of parasitic BJT amplification. The degree of this amplification (β) is the key to understanding the dramatic L_T increase in recent SOI-Planar SRAMs. These devices have SOI and BOX layers aggressively thinned down to 10 nm, causing a significant drop in β.

3) The saturated SEU cross sections of SRAMs (σ_∞) decrease roughly with the cell area (A_{cell}), which depends on l^2, and it has already reached the typical area of an ion track (A_{ion}) in the current Bulk-Fin generations. The A_{cell} trend provides an upper bound for σ_∞, but some Bulk-Planar SRAMs exceed it.
   a) The disappearance of the A_{cell} boundary is evident in Bulk-Planar SRAMs with $l \lesssim 100$ nm. It is attributed to MCUs, because Bulk transistors are connected to each other through the substrate.
   b) SOI SRAMs continue to stay within the A_{cell} boundary across generations because of the isolation effect of BOX. Recent technology progress has resulted in aggressive BOX thinning however, which degrades the isolation effect, causing large MCUs under certain bias conditions.
   c) In contrast to the other SRAM SEU parameters, the scaling trend of σ_∞ is favorable because it can reduce the rate of SEUs. In the future, however, this benefit may no longer be available, because σ_∞ is now almost the same as A_{ion}. This geometrical agreement suggests that σ_∞ will no longer become smaller than A_{ion} even if A_{cell} is further decreased.

4) The SET pulse of inverters (δ) monotonically decreases, roughly conforming to l, but with a large spread ranging between $l/3$ and $100l/3$ in each generation.
   a) The revealed lower bound $l/3$ is attributed to an artificial effect of the measurement resolution, showing good agreement with the FO4 inverter delay (τ_{FO4}). In recent Bulk-Fin generations ($l \lesssim 30$ nm), however, the lower bound departs from $l/3$ and remains at ~10 ps. This constant behavior is also observed for τ_{FO4} and is possibly due to the speed penalty from C_p. Interestingly, the lower bound has attractive potential for estimating Q_C, reflecting the impact of C_p.
   b) The revealed upper bound $100l/3$ seems useful for estimating the risk of SET errors in microprocessors and might cut the cost of δ characterization, which requires a dedicated measurement circuit. Interestingly, in very early generations ($l \gtrsim 1000$ nm), this upper bound is fixed at ~3 ns rather than $100l/3$. This disappearance of the upper bound suggests that an SET is mainly determined by the response of a discrete diode rather than that of the circuit in the very early generations.

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