Scan Chain Reordering-aware X-Filling and Stitching for Scan Shift Power Reduction

Sungyoul Seo[1], Yong Lee[1], Hyeonchan Lim[1], Joohwan Lee[2], Hongbom Yoo[2], Yojoung Kim[2], and Sungho Kang[1]
[1]Department of Electrical and Electronic Engineering
[1]Computer systems & reliable SoC Lab., Yonsei University, Seoul, Korea
[2]Samsung Electronics, Korea
[1]{sungyoul, daiginda, lhcy92}@soc.yonsei.ac.kr, shkang@yonsei.ac.kr

***Abstract*—As a scan-based testing enables higher test coverage and faster test time than alternative ways, it is widely used by most system-on-chip (SoC) designers. However, since the number of logic gates is over one hundred million gates, a number of scan cells lead to excessive power consumption and it produces a low shifting frequency during the scan shifting mode. In this paper, we present a new scan shift power reduction method based on a scan chain reordering (SR)-aware X-filling and a stitching method. There is no need to require an additional logic for reducing the scan shift power, just a little routing overhead. Experimental results show that this method improves scan shift power consumption on benchmark circuits in most cases compared to the results of the previous works.**

Keywords—scan based-testing; low power scan testing; shifting power reduction; low-shift power X-fill; design-for-testability (DFT)

I. INTRODUCTION

As technology processes scale up and design complexities grow, more intellectual property (IP) cores can be integrated into a single chip such as a system-on-chip (SoC). Actually, most modern designs are over a hundred million logic gates [1]. In these large designs, a variety of scan-based solutions have emerged as a reliable test scheme for testing complex sequential circuits for reducing automatic test pattern generation (ATPG) and boosting fault coverage level [2]. However, the power consumption is much more excessive during the scan test operation than during the functional operation [3]. A number of changing states occur in the scan flip-flops during the scan-based testing due to shift and/or capture the test patterns into the scan chains [4]. This problem produces many switching activities in the internal combinational logics and degrades the reliability of the scan testing. As a result, it causes a structural damage and a large voltage drop that lead to erroneous data transfer [5].

There are two major problems from the low power testing point of view: 1) capture power and 2) shift power. The capture power is generated by the same scan cells' value switching as the scan-in patterns are replaced to the captured responses. On the other hand, the shift power is generated by a two adjacent scan cells' value difference during the shift mode [6]. Therefore, these two issues should be dealt with differently [7]. For blocking the malfunction during at-speed testing, the capture power must be lowered not to generate excessive IR-drop and resulting delay. If the shift frequency and/or the test parallelism should be improved, it is necessary to reduce the shift power [8].

In this paper, we focus on the scan shift power reduction, which can reduce the test cost by speeding up the shift frequency during the shift mode. To achieve this, new methods, the X-filling and the scan cell stitching method, will be introduced. These two methods are interdependent. Hence, the new X-filling method is specialized for our scan stitching method and the new scan stitching method is performed after applying our X-filling method.

The remainder of this paper is organized as follows. Section II describes the preliminaries of related works in the scan shifting power reduction and the scan shifting power estimation. In Section III, the proposed scan shift power reduction methods, the scan chain reordering (SR)-aware X-filling and the low power scan stitching, are specifically introduced. The experimental results are shown in Section IV, and we conclude this paper in Section V.

II. PRELIMINARIES

A. Related Works

To solve the power issues, numerous power reduction methods during the scan-based testing have been proposed for satisfying not to reach a threshold power without reducing the test frequency. The low power scan test solutions can be classified into two categories: 1) ATPG-based and 2) design-for-testability (DFT)-based [9].

The ATPG-based solution analyzes and/or controls the configuration or the results of the ATPG for the test power reduction [10]. Many X-filling methods which are known to be the most typical ATPG-based solution are published [7, 11]. In addition, low power test pattern generation algorithms [12, 13] are used for the same purpose. This solution can take advantage of the conventional test flow through ATPG without any additional logic insertion, while it cannot obtain equivalent effects of the power reduction as the DFT-based solution. The DFT-based solution inserts the additional test control logics and/or modifies a scan chain configuration [10]. The examples of this solution include scan cell reordering [6], scan cell gating [3, 8], scan chain modification [14, 15], and scan clock gating [2, 4]. However, the scan cell gating and the scan clock gating affects clock skew problems in the normal mode, and the scan

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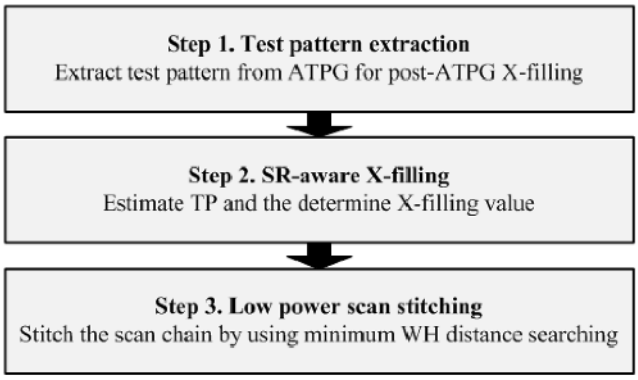


Fig. 1. Procedure for the proposed scan shift power reduction method.

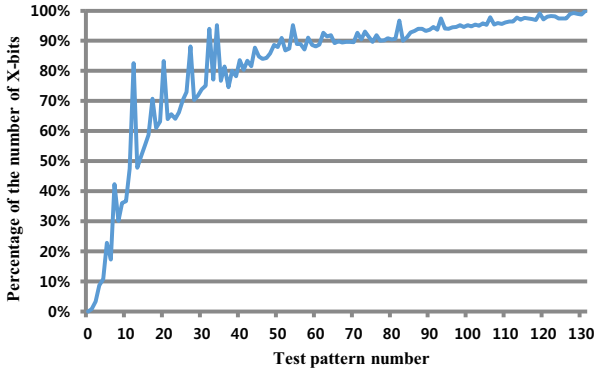


Fig. 2. Test data composition of s38584 benchmark circuit.

chain modification may degrades the coverage of un-modeled faults [15].

Recently, combination of the X-filling and the DFT-based solution is introduced for improving the test power efficiency [16]. In this paper, the proposed scan shift power reduction method adopted both two solutions, which is comprised of the X-filling and the scan cell reordering method, for the same purpose, although this method may increase computation time. The X-filling methods are generally used for improving a compression efficiency and/or saving the test power. Proposed X-filling method is for reducing the scan shifting power, but it does not impact directly on the power reduction. Hence, it is just SR aware method, which helps to improve the effectiveness of the proposed scan stitching method. Therefore, we propose an additional method for the low power scan stitching method based on a new weighted hamming distance (WHD) searching, which gives a priority to the low power consumption not a routing overhead. In Section III, we describe more detail of these methods and the achieved experimental results are presented in Section IV.

B. Scan Shifting Power Estimation

The power consumption in complementary metal-oxide-semiconductor (CMOS) integrated circuits (ICs) can be classified into two categories: 1) static power and 2) dynamic power. The static power is owing to a leakage current and the dynamic power is due to charging and discharging of a load capacitance [17]. For improving the scan shifting frequency, the dynamic power has more severe effect than the static power from the point of view of switching from 0 to 1 or vice versa on the circuit components [18].

A weighted transition metric (WTM) [18] is one of the preferred methods for estimating the scan shifting power. The WTM can consider both the number of transition and their relative positions into a scan chain. The shift-in power in the *i*th pattern can be estimated with the following equation:

$$WTM_i = \sum_{j=1}^{N-1} \left(S_{i,j} \oplus S_{i,j+1} \right) \times j \qquad (1)$$

where N is the number of the scan cells into the scan chain and $S_{i,j}$ represents the logic state of the jth scan cell in the ith test pattern. If the shift-out power may be estimated, the last term is replaced to $(N - j)$. In this paper, all scan shift power will be presented by (1).

III. Proposed Scan Shift Power Reduction Method

In order to deal with the scan shift power, we propose a new scan shift power reduction method using the SR-aware X-filling and the scan stitching method, and this procedure is illustrated in Fig. 1. First, the test patterns are extracted from the ATPG considering a post-ATPG X-filling. Then, the SR-aware X-filling is performed based on the results of the transition probability (TP). Finally, all scan chains are stitched by using minimum WHD searching. To explain more detail, we sequentially demonstrate these three steps and illustrate its examples.

A. Test Pattern Extraction

Note that, we use the post-ATPG X-filling, which consists of a test relaxation and the X-filling, and its effectiveness depends on the characteristic of the X-bits in the test cubes [19]. The test relaxation is to maintain a test coverage and test pattern count. Hence, it should obtain the test patterns including a number of X-bits although it uses a dynamic compaction during the ATPG. Fortunately, it has been observed that the test patterns are composed of a number of X-bits as shown in Fig. 2. Care bit density of the test patterns is fairly high in the earlier patterns, but the later test patterns (over 85%) are composed of a number of X-bits. Consequently, the test patterns can be extracted including many X-bits in spite of using the dynamic compaction. Due to this result, the later test patterns can be controlled by our proposed SR-aware X-filling.

To improve the efficiency of the test relaxation, we use a random fill in the earlier test patterns although this filling method introduces many switching activities during the scan shift mode. It is a negligible burden compared to the expected effects in the later test patterns because we speed up the shifting frequency when inserting the later test patterns which composed over 85% X-bits. Hence, automatic test equipment (ATE) maintains conventional frequency in the area of the earlier test patterns. But if the test power reduction is enabled in the later test patterns, the total test time is significantly faster than the conventional low power test methods.

B. SR-aware X-Filling

As previous mentioned, the proposed ATPG flow generates the test patterns with many X-bits in the later test patterns. The

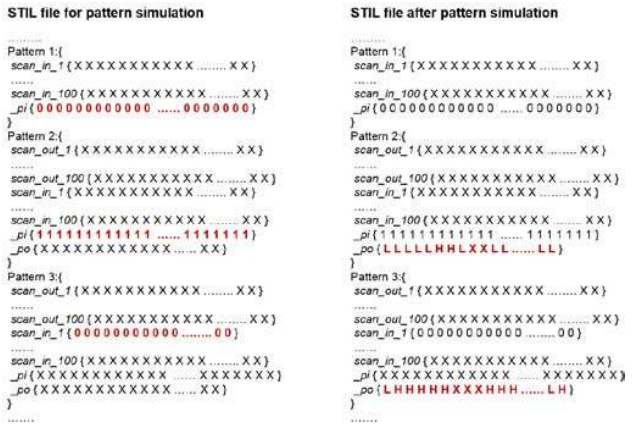


Fig. 3. STIL files for the pattern simulation and the simulation result.

objective of the proposed X-filling is for improving the effectiveness of the proposed low power scan stitching method. In addition, it intends to operate on both single chain and multiple chains. In order to meet above conditions, two additional works should be performed: 1) pattern simulation and 2) TP estimation. The pattern simulation and the TP estimation is to improve the similarity on the cells' values in the both scan-in and scan out. This is because it is trying to assign the X-bits to same bits and get the same responses for the proposed scan stitching method; these procedure is necessary for the Step 3.

First of all, a new standard test interface language (STIL) file is required to simulate the test patterns in order to get the test responses on a simulation pattern. The simulation pattern is that the X-bits of each scan chain value are filled with all 0s or 1s. Let us assume that a design has 100 scan chains, the STIL file for the simulation and the simulation result are presented in Fig. 3, where s*can_in_i* is a *i*th input test data, s*can_out_i* is a *i*th output test responses, and *_pi* and *_po* are a primary input (PI) and a primary output (PO). In *Pattern 1* for the pattern simulation, the *_pi* data are filled with all 0s. On the contrary, the *_pi* data are assigned to all 1s in the next pattern. From the next pattern, this procedure is iterated until final *scan_in_100* data are filled with all 0s and 1s in the same way. Here, the rest test patterns are filled with all X bits. The pattern counts in the STIL file for the pattern simulation, C_{sim_pat}, can be estimated with the following equation:

$$C_{sim\_pat} = N_{SC} \times 2 + 2 \qquad (2)$$

where N_{SC} is the number of the scan chains and the last term which is added to 2 is due to PI such as pattern 1 and 2. Once the initial STIL file is produced, the pattern simulation is performed by the ATPG tool such as TetraMAX which is the test generation tool of Synopsys. The results of this simulation are illustrated in bold in the right side of the Fig. 3, where *L* and *H* indicate a low (0) and a high (1) response.

Next, the TP estimation is conducted for deciding whether the X-bits of the particular chain should be filled with 0 or 1. Let us assume that the number of the scan cells is *N*, then the TP in each pattern, TP_{tot}, can be estimated with the following equation:

$$TP_{tot} = \sum_{i=1}^{N-1} TP_{in\_out}^{i,i+1} = \sum_{i=1}^{N-1} \left(TP_{in}^{i,i+1} + TP_{out}^{i,i+1} \right) \qquad (3)$$

where each TP_{in}^{i} and TP_{out}^{i} indicates input and output TP between *i*th and *i*+1th cell values, and $TP_{in\_out}^{i,i+1}$ is a summation of them. In addition, each $TP^{i,i+1}$ can be written as follows:

$$TP^{i,i+1} = P\left(x^{i}=0\right) \times P\left(x^{i+1}=1\right) + P\left(x^{i}=1\right) \times P\left(x^{i+1}=0\right) \qquad (4)$$

where the two terms are whether a switching activity is produced between the *i*th and the *i*+1th cell. If x^{i} or x^{i+1} is assigned to X, $TP^{i,i+1}$ is 0.5.

Note that the proposed X-filling method is SR aware, so the TP estimation is conducted after a simple SR. The proposed scan stitching is performed to collect the same in and out values for reducing switching activities. Let us consider the following example where $N = 24$ and $N_{SC} = 4$, shown in Fig. 4. It shows how the X-bits of the Chain 1 will be determined. In Case 1, the pattern simulation is performed after the input data of Chain 1 are fully filled with 0s and the result is shown in Fig. 4(a). When

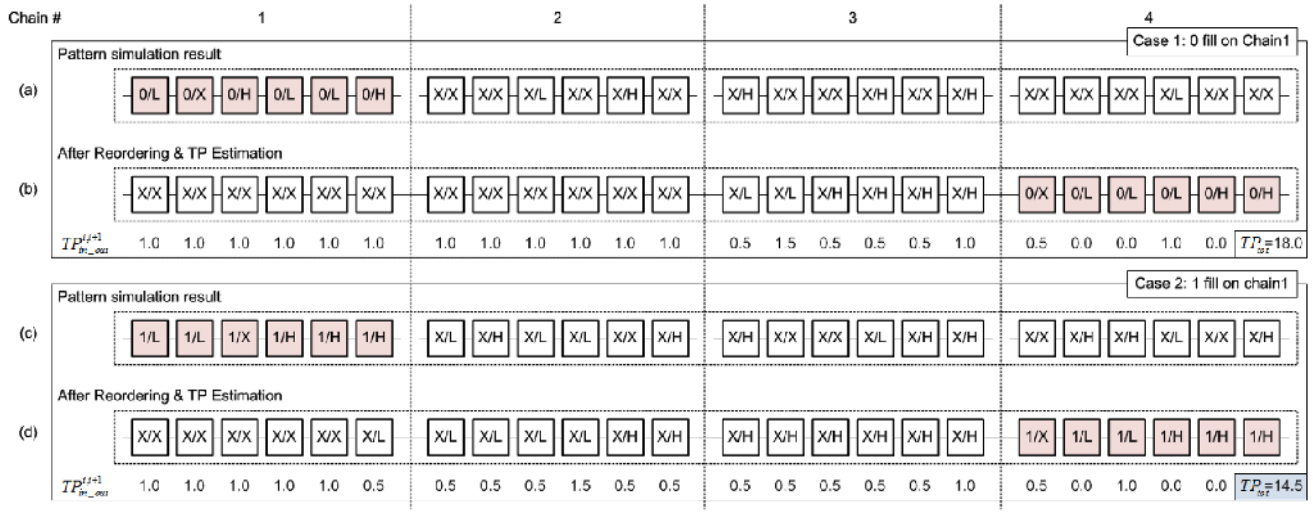
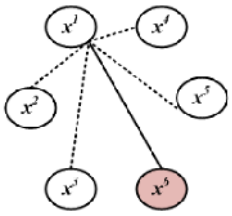


Fig. 4. Simple example for the SR and the TP estimation.



Scan cells	x^1	x^2	x^3	x^4	x^5	x^6
1st pattern	1/L	1/L	1/H	1/H	1/H	1/L
2nd pattern	1/L	1/H	1/H	1/H	1/H	0/L
3rd pattern	1/H	1/H	1/L	1/H	1/H	1/H
$D(x^i, x^j)$	-	5	15	10	10	1

Fig. 5. Simple example for the proposed scan stitching method.

TABLE I. INFORMATION OF THE BENCHMARK CIRCUITS

Circuit	# of FFs	# of PIs	# of POs	Gate Counts
s13207	669	31	121	7,951
s15850	597	14	87	9,772
s38417	1,636	28	106	22,179
s38584	1,452	12	278	19,253
b17	1,415	37	97	32,326
b18	3,320	37	23	114,621
b19	6,642	21	30	231,320

the pattern simulation is done, some unspecified bits in the responses are replaced to the specified bits due to insertion of 0s to the inputs of Chain 1. Then, the simple reordering and the TP estimation are performed, and the final TP_{tot} is estimated to 18.0, as shown in Fig. 4(b). Likewise, in Case 2, the pattern simulation is operated after the input data of Chain 1 are assigned to 1s and this example is shown in Fig. 4(c). Here, the final TP_{tot} is estimated to 14.5, as shown in Fig. 4(d), which is smaller than that of Case 1. Consequently, the X-bits of Chain 1 is filled with 1s. After the X-bits of all scan chains are decided in the same way, the scan stitching will be performed.

C. Low Power Scan Stitching

The final step requires fully filled test patterns for stitching the all scan chains, which is also called the scan reordering. For reducing the test power, the minimum WHD searching is performed; hence distance between ith and jth cell, $D(x^i, x^j)$ can be estimated with the following equation:

$$D\left(x^i, x^j\right) = D_{in}\left(x^i, x^j\right) + D_{out}\left(x^i, x^j\right) = \sum_{n=1}^{N} W_{in}^{i}\left(x_{in}^{n,i} \oplus x_{in}^{n,j}\right) + \sum_{n=1}^{N} W_{out}^{i}\left(x_{out}^{n,i} \oplus x_{out}^{n,j}\right) \quad (5)$$

where $D_{in}(x^i, x^j)$ and $D_{out}(x^i, x^j)$ is the distance according to the input test data and the output test response, respectively. W_{in}^{i} and W_{out}^{j} is the weight of ith and jth element which is written by i+1 and L-(i+1), respectively. In addition, L is the length of a scan chain, N is the number of the test pattern, and $x_{in}^{n,i}$ and $x_{in}^{n,j}$ is a bit of the ith and jth input test data in a nth test pattern. On the contrary, $x_{out}^{n,i}$ and $x_{out}^{n,i}$ are about the output test response. By using the minimum WHD searching, the switching activities can be reduced for the low power scan test.

Let us assume that a design has 6 scan cells and the number of test patterns is 3; the example is shown in Fig. 5. Here, the first scan cell has already been selected. So, this example is a procedure, which is trying to find the second cell using the minimum WHD searching. In order to get the minimum WHD for x^1, all elements are estimated using (5) and their results are illustrated in the last columns of the table in the Fig. 5. As a result, the 6th scan cell is selected as the next scan cell. In this example, the shadow blocks indicate the selected minimum scan cell and the solid line is stitched line, but the dotted lines are invalid lines. This work is iterated until all scan chains are stitched by the minimum WHD searching.

IV. EXPERIMENTAL RESULTS

To examine the improved effects of the proposed method, experiments are performed on the four large ISCAS'89 and three large ITC'99 benchmark circuits. The information of these

TABLE II. COMPARISON OF THE SCAN SHIFT POWER WITH THE ADJACENT FILLING METHOD

Circuit	# of flip flops	# of scan chains	Method	Earlier patterns		Later patterns		Total patterns	
				# of PAT	WTM avg.	# of PAT	WTM avg.	# of PAT	WTM avg.
s13207	669	50	Adjacent fill	10	3,223	102	1,625	112	1,768
			LP scan stitch		2,781		1,154		1,300
			SR-aware fill	10	3,391	112	1,995	122	2,109
			LP scan stitch		2,629		**365**		**551**
s15850	597	50	Adjacent fill	10	2,626	90	1,404	100	1,526
			LP scan stitch		2,180		795		934
			SR-aware fill	10	3,116	94	1,489	104	1,605
			LP scan stitch		2,190		**407**		**568**
s38417	1636	50	Adjacent fill	10	23,257	99	13,314	109	14,226
			LP scan stitch		19,434		7,997		9,046
			SR-aware fill	10	24,952	111	15,330	121	16,126
			LP scan stitch		18,478		**4,675**		**5,815**
s38584	1452	50	Adjacent fill	10	18,478	113	8,158	123	9,102
			LP scan stitch		16,528		4,849		5,806
			SR-aware fill	10	19,768	121	7,944	131	8,846
			LP scan stitch		17,328		**2,730**		**3,844**

TABLE III. COMPARISON OF THE SCAN SHIFT POWER WITH A VARIETY OF THE SCAN CHAIN SIZE

Circuit	# of FFs	# of scan chains	Method	Earlier patterns		Later patterns		Total patterns	
				# of PAT	WTM avg.	# of PAT	WTM avg.	# of PAT	WTM avg.
b18	3320	50	Adjacent fill	100	43,496	919	13,660	1,019	16,588
			SR-aware fill	100	43,059	1,183	18,345	1,283	20,271
			LP scan stitch	100	**39,809**	1,183	**6,585**	1,283	**9,175**
		100	Adjacent fill	100	21,142	923	6,735	1,023	8,144
			SR-aware fill	100	20,945	1,183	9,938	1,283	10,796
			LP scan stitch	100	**21,712**	1,183	**3,823**	1,283	**5,217**
b19	6642	50	Adjacent fill	150	153,478	905	55,819	1,055	69,705
			SR-aware fill	150	152,065	1,247	92,530	1,397	98,922
			LP scan stitch	150	**152,889**	1,247	**19,490**	1,397	**33,814**
		100	Adjacent fill	150	74,926	905	39,492	1,055	43,680
			SR-aware fill	150	74,926	1,119	39,492	1,269	43,680
			LP scan stitch	150	**77,801**	1,119	**12,045**	1,269	**19,815**

TABLE IV. COMPARISON OF THE SCAN SHIFT POWER WITH A VARIETY OF EXISTING SCAN CELL REORDERING METHODS

Circuit	Method	APR	ROBPR [6]	PRORO [6]	Proposed method
s13207	Total WTM	8,490,452	3,665,027	3,895,618	**2,867,436**
	Normalized	1.00	0.43	0.45	**0.34**
s15850	Total WTM	7,013,465	2,994,375	3,034,897	**3,317,747**
	Normalized	1.00	0.43	0.43	**0.47**
s38417	Total WTM	82,459,089	39,396,985	40,505,086	**34,234,908**
	Normalized	1.00	0.48	0.49	**0.41**
s38584	Total WTM	60,049,467	37,493,542	37,527,256	**25,360,926**
	Normalized	1.00	0.62	0.62	**0.42**
b17	Total WTM	295,180,622	63,096,447	64,846,104	**60,108,710**
	Normalized	1.0	0.21	0.22	**0.20**
Avg. normalized		1.00	0.43	0.44	**0.37**

circuits are shown in Table I. The initial test patterns are generated from TetraMAX with the dynamic compaction turned on, the random fill turned on in the earlier patterns, and the random fill turned off in the later patterns. The scan shift power is estimated by (1).

Table II compares the scan shift power with the adjacent fill which is known as simple and efficient to reduce the shift power. The first row in each circuit shows comparable result generated from the ATPG with the adjacent fill and the next row indicates the result of the proposed low power stitching method after applying the adjacent fill. The third and fourth row are the results which performed in our proposed methods. In the third and fourth row, the earlier patterns are generated from the ATPG with random fill. However the later patterns are generated from the ATPG with no filling method and then all X-bits are fully applied to the proposed SR-aware X-filling. Our filling method increases the number of test pattern (about 10%) for reaching the same coverage as the result of applying the adjacent fill. However, the proposed method covers the lower shifting power (above -34% up to -64%) than the results of the adjacent fill after applying the proposed scan stitching method.

It is necessary to verify the facts that the conventional test frequency can be maintained in the range of the earlier pattern. Moreover, it should be applied to the circuits if the size of the scan chain is variable. To examine these situations, the additional experiments in the largest ITC'99 circuits are performed and these results are shown in Table III. The experimental results of the proposed method are illustrated in bold. In the earlier patterns, the shifting power after the low power scan stitching is similar to the results of the adjacent fill. Hence, this result shows that the shifting frequency can maintain the conventional frequency. In addition, the scan shift power is always reduced regardless of the size of the scan chains.

Finally, we compare our proposed method with the existing scan chain reordering methods and these results are shown in Table IV. The third column is produced by [6] using APR, which is a commercial back-end tool of Cadence. Reordering considering both pattern and response correlation (ROBPR) method and power and routing-overhead reordering (PRORO) method consider a routing overhead a little, but the power consumption is quite reduced compared to the Cadence method. This is because the priority of APR is the routing overhead during the scan cell reordering. On the contrary, our proposed

method concentrates the scan shift power reduction. All experiments in Table IV are performed in a single chain environment for comparison with the existing methods. In addition, these results show that the proposed method covers outstanding performance from a low power scan shifting point of view.

V. Conclusion

In this paper, we present a new scan shift power reduction method based on the SR-aware X-filling and the low power scan stitching. The proposed method reduces the scan shifting power without a heavy burden. The experimental results show that the scan shifting power is more effective than the results of the existing works in all cases such as the number of the scan chains and many circuits. Moreover, the proposed method can be always used to improve the test frequency by reducing the scan shifting power in the later test patterns regardless of the circuit type. To conclude, the proposed scan shift power reduction method is suitable for any circuit in order to reduce the scan shift power and this result leads to save the test time during the scan-based test.

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