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Schottky-Barrier Profiling Techniques in Semiconductors - Gate Current and Parasitic Resistance Effects

David C. Look
Wright State University - Main Campus, david.look@wright.edu

Schottky-barrier profiling techniques in semiconductors: Gate current and parasitic resistance effects

D. C. Look
University Research Center, Wright State University, Dayton, Ohio 45435

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The theory for obtaining mobility and carrier concentration profiles by the Hall-effect, magnetoresistance, and capacitance-conductance methods is developed in the relaxation-time approximation. This theory is then applied to semiconductors in which a Schottky barrier is used to control a depletion region. Particular emphasis is given to field-effect transistor structures which are ideally suited for geometric magnetoresistance measurements. A unique feature of the present model is the correction for finite gate (Schottky-barrier) current, which can be very important under forward-gate-bias conditions. The ability to use forward-bias makes the near-surface region more accessible. Also, parasitic resistance effects are treated. We apply these results to GaAs conducting layers formed by direct implantation of $4\times10^{12}/cm^2$, 100-keV Si ions into Cr-doped GaAs.

I. INTRODUCTION

Thin-layer structures are usually characterized by their average mobilities and carrier concentrations, as obtained from surface Hall-effect and conductivity measurements. However, it is often necessary to know the detailed profiles of these quantities in order to predict device properties. For example, the pinch-off behavior of a field-effect transistor (FET) depends on the steepness of the carrier profile in the substrate-active-layer region. One way to get both carrier concentration and mobility profiles is by successively removing very thin layers, and then performing conductivity and Hall-effect measurements at each step.[1] This method, however, has several disadvantages: (1) it is totally destructive, and the measurements cannot be repeated; (2) it is time consuming, and not easily automated; and (3) the layer removal process (usually a chemical etch) is often not homogeneous across the surface of the sample, and thus measurements in the high-resistivity tail of the profile are difficult if not impossible. All of the above difficulties are overcome by the Schottky-barrier techniques, in which actual layer removal is replaced by depletion depth adjustment.[2-4] Such adjustment is accomplished by reverse-biasing the Schottky barrier with respect to a nearly Ohmic contact. For example, in *n*-type GaAs, it is convenient to evaporate a gold Schottky barrier over the surface of a Hall-bar or van der Pauw pattern (avoiding the Ohmic contacts, of course) and reverse-bias the Au layer. The maximum depletion depth is limited by breakdown at high reverse-bias voltages, although this problem is not severe in 10^{17}-cm^{-3} GaAs, typical material for FETs. The *minimum* depth has usually been taken as the zero-bias depletion depth, about 0.1 μm in the aforementioned material. (Note that the depletion from *surface* states in GaAs has about the same magnitude as that imposed by a Schottky barrier, so that the etch-step method is also limited in profiling close to the surface.) However, by *forward*-biasing the Schottky barrier, it is possible to get closer to the surface, in fact, to about 0.05 μm in 10^{17}-cm^{-3} GaAs. The region between 0.05 and 0.10 μm is quite important in direct-implant GaAs FETs, since the concentration and implant-damage profile peaks typically occur here. Unfortunately, in forward bias, gate current begins to flow and can cause severe errors in mobility calculations.

It is the purpose of this paper to develop a theoretical basis for profiling by three different techniques: (1) Hall effect, (2) geometrical magnetoresistance, and (3) capacitance-conductance. The relationships between the various measured mobilities will be established in the relaxation-time approximation. Many of the results reported in this first section will not be new, but have the advantage of being presented in a unified framework. Then, a dc effective-circuit model will be developed to show how gate (Schottky-barrier) current, and parasitic resistance, can be included in the analysis. Particular emphasis will be placed on the FET structure. Finally, the results will be applied to a FET-type GaAs layer formed by direct implantation of $4\times10^{12}/cm^2$, 100-keV Si ions into a Cr-doped, semi-insulating GaAs substrate.

II. BULK TRANSPORT THEORY

The current density in an isotropic, *n*-type semiconductor, with spherical equal-energy surfaces, is given by[4]

$$J_x = \sigma_{xx}E_x + \sigma_{xy}E_y, \tag{1}$$

$$J_y = \sigma_{yx}E_x + \sigma_{yy}E_y, \tag{2}$$

where

$$\sigma_{xx} = \sigma_{yy} = \frac{ne^2}{m_n^*}\left\langle\frac{\tau}{1+\omega^2\tau^2}\right\rangle, \tag{3}$$

$$\sigma_{xy} = -\sigma_{yx} = -\frac{ne^2}{m_n^*}\left\langle\frac{\omega\tau^2}{1+\omega^2\tau^2}\right\rangle. \tag{4}$$

Here, the σ_{ij} are components of the conductivity tensor, E_i denotes the electric-field component in the ith direction, n is the electron concentration, e is the *magnitude* of the electronic charge, m_n^* is the electron effective mass, τ is the mean time between collisions, and $\omega = eB/m_n^*$, where B is the strength of a magnetic field along the z axis. The brackets denote an average over energy.

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A. Hall effect, physical magnetoresistance

We first consider the geometry, shown in Fig. 1(a), for Hall-effect and physical magnetoresistance measurements. The boundary condition is $J_y = 0$, so that, from Eq. (2), $E_y = -E_x\sigma_{yx}/\sigma_{yy}$. The Hall coefficient is defined by

$$R \equiv \frac{E_y}{J_x B} = -\frac{1}{B}\frac{\sigma_{yx}}{\sigma_{xx}\sigma_{yy} - \sigma_{xy}\sigma_{yx}} \equiv -\frac{r}{ne}, \tag{5}$$

where the well-known Hall factor r is given by

$$r = \frac{\left\langle \frac{\tau^2}{1+\omega^2\tau^2} \right\rangle}{\left\langle \frac{\tau}{1+\omega^2\tau^2} \right\rangle^2 + \omega^2 \left\langle \frac{\tau^2}{1+\omega^2\tau^2} \right\rangle^2}. \tag{6}$$

For $\omega^2\tau^2 \ll 1$, we simply have $r = \langle\tau^2\rangle/\langle\tau\rangle^2$. The Hall mobility is defined by

$$\mu_H \equiv |R\sigma| = (r/ne)ne\,\mu_{con} = r\,\mu_{con} \tag{7}$$

where μ_{con}, the conductivity mobility, will be defined later.

In this same approximation, by expanding the denominators in Eqs. (3) and (4) to order $\omega^2\tau^2$, we get

$$\begin{aligned} J_x &= \left(\sigma_{xx} - \sigma_{xy}\frac{\sigma_{yx}}{\sigma_{yy}}\right)E_x, \\ &\simeq \frac{ne^2E_x}{m_n^*}\left[\langle\tau\rangle - \omega^2\left(\langle\tau^3\rangle - \frac{\langle\tau^2\rangle^2}{\langle\tau\rangle}\right)\right] \\ &= \frac{ne^2\langle\tau\rangle E_x}{m_n^*}\left[1 - \frac{e^2B^2}{m_n^{*2}}\frac{\langle\tau^2\rangle^2}{\langle\tau\rangle^2}\left(\frac{\langle\tau^3\rangle\langle\tau\rangle}{\langle\tau\rangle^2} - 1\right)\right] \\ &= \frac{ne^2\langle\tau\rangle E_x}{m_n^*}\left(1 - \frac{e^2\langle\tau\rangle^2}{m_n^{*2}}r^2B^2\xi\right) \\ &= ne\,\mu_{con}(1 - r^2\xi\,\mu_{con}^2B^2)E_x \\ &= ne\,\mu_{con}(1 - \mu_{PMR}^2B^2)E_x, \end{aligned} \tag{8}$$

where we have defined $\mu_{con} \equiv e\langle\tau\rangle/m_n^*$, $\mu_{PMR} = r\xi^{1/2}\mu_{con}$, and

$$\xi = (\langle\tau^3\rangle\langle\tau\rangle/\langle\tau^2\rangle^2) - 1. \tag{9}$$

Thus, we can determine μ_{PMR} from the relationship $J_x(B)/J_x(0) = 1 - \mu_{PMR}^2B^2$. The parameter ξ is usually called the magnetoresistance coefficient.

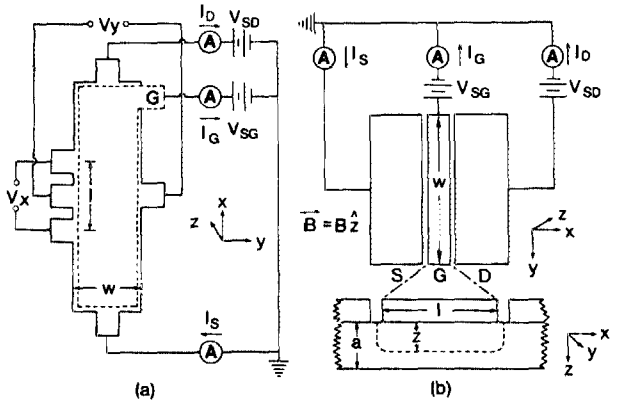

FIG. 1. (a) Hall-bar structure used in this study, drawn to scale, with $l \simeq w \simeq 30\ \mu$m. The dotted lines denote the Schottky-barrier gate. Current directions refer to electron flow. (b) Typical FET structure used in this study, not drawn to scale. For the "fat" FET, $l \simeq 50\ \mu$m, $w \simeq 400\ \mu$m, and $a \simeq 0.1\ \mu$m. The bottom part of (b) is a cross-sectional view of the region under the gate.

B. Geometrical magnetoresistance

We next consider the geometry shown in Fig. 1(b), in which it is apparent that the Hall field E_y is effectively shorted out, i.e., $E_y = 0$. Then, to first order in $\omega^2\tau^2$, Eq. (1) becomes

$$\begin{aligned} J_x &= \sigma_{xx}E_x \\ &= \frac{ne^2}{m_n^*}(\langle\tau\rangle - \omega^2\langle\tau^3\rangle)E_x \\ &= \frac{ne^2\langle\tau\rangle}{m_n^*}\left(1 - \frac{\langle\tau^3\rangle}{\langle\tau\rangle^3}\frac{e^2\langle\tau\rangle^2}{m_n^{*2}}B^2\right)E_x \\ &= ne\,\mu_{con}[1 - r^2(\xi+1)\mu_{con}^2B^2]E_x \\ &= ne\,\mu_{con}(1 - \mu_{GMR}^2B^2)E_x, \end{aligned} \tag{10}$$

where $\mu_{GMR} = r(\xi+1)^{1/2}\mu_{con}$. For the GaAs material considered in this study, τ is almost independent of energy through much of the layer because of the nearly degenerate electron concentration. Then, $\mu_{GMR} \simeq \mu_H \simeq \mu_{con}$, and $\mu_{PMR} \simeq 0$. However, the "tail" of the electron profile is no longer degenerate so that these approximations do not hold in this region.

III. PROFILING THEORY

We consider the geometries shown in Fig. 1. For the FET-like structure, Fig. 1(b), electron current flows from the source to the drain, which is positively biased at V_{SD}, but the gate may also draw current, especially when V_{SG} denotes a relatively high, positive bias (say, 0.5–0.6 V). In Fig. 1(b), the region under the Schottky-barrier gate is depicted in an expanded, cross-sectional view. A certain region under the gate, of depth z, is depleted of electrons, due to the Schottky-barrier surface potential, $V_{SG} + V_{bi}$, where V_{bi}, the "built-in" potential, is about -0.75 V, in GaAs.[5] For example, when $n \simeq 10^{17}$ cm^{-3} in GaAs, $z \simeq 0.1\ \mu$m for $V_{SG} = 0$. In order that z be uniform along the length of the gate, we require that $V_{SD} \ll 2|V_{SG} + V_{bi}|$. If we decrease V_{SG} by ΔV_{SG}, then z will increase by Δz. We assume that the conductive layer ends abruptly at $z = a$. The total currents will be given by integrals over thin sheets of current, from z to a, with each sheet assumed to have uniform electrical properties. Thus, from Eqs. (1) and (2),

$$I_x(V_{SG}) = w\left(E_x(V_{SG})\int_z^a \sigma_{xx}(s)ds + E_y(V_{SG})\int_z^a \sigma_{xy}(s)ds\right), \tag{11}$$

$$I_y(V_{SG}) = w\left(E_x(V_{SG})\int_z^a \sigma_{yx}(s)ds + E_y(V_{SG})\int_z^a \sigma_{yy}(s)ds\right), \tag{12}$$

where each sheet has width w and depth ds, and where I_x is the total current actually flowing under the depletion region. (Note that $I_x \neq I_S \neq I_D$, unless $I_G = 0$. This topic will be discussed later.) The electric fields are assumed uniform, i.e., $E_x = V_x/l$, and $E_y = V_y/w$, where w and l are defined in Figs. 1(a) and 1(b), for the Hall-bar and FET structures, respectively.

In some experiments, V_{SD} is held constant and, in other experiments, I_S or I_D. Thus, we shall present the results in a way which will include both the constant-current and constant-voltage cases. Also, we will defer the treatment of parasitic resistances until the next section.

It is convenient to solve Eqs. (11) and (12) and set up a

general profiling model before imposing any boundary condition. By using the relationship $\sigma_{xy} = -\sigma_{yx}$, we get

$$\int_z^a \sigma_{xx}(s)ds = \frac{I_x/wE_x + I_yE_y/wE_x^2}{1+E_y^2/E_x^2} \equiv \alpha, \tag{13}$$

$$\int_z^a \sigma_{xy}(s)ds = \frac{I_xE_y/wE_x^2 - I_y/wE_x}{1+E_y^2/E_x^2} \equiv \beta. \tag{14}$$

Then,

$$\begin{aligned}\Delta\alpha &\equiv \alpha(V_{SG}+\Delta V_{SG}) - \alpha(V_{SG}) \\ &= \int_{z+\Delta z}^a \sigma_{xx}(s)ds - \int_z^a \sigma_{xx}(s)ds \\ &= \int_{z+\Delta z}^z \sigma_{xx}(s)ds = -\Delta z\sigma_{xx}(z) \\ &= -\Delta z[ne\mu_{\rm con} - ne\mu_{\rm con}^3 r^2(\xi+1)B^2]. \end{aligned} \tag{15}$$

$$\begin{aligned}\Delta\beta &\equiv \beta(V_{SG}+\Delta V_{SG}) - \beta(V_{SG}) = -\Delta z\sigma_{xy}(z) \\ &= -\Delta z[-ne\mu_{\rm con}^2 rB], \end{aligned} \tag{16}$$

where Eqs. (3) and (4) have been expanded to order $\omega^2\tau^2$, and $\mu_{\rm con}$, r, and ξ have been defined earlier. Equations (15) and (16) then yield

$$\sigma(z) \equiv ne\mu_{\rm con} = -\Delta\alpha_0/\Delta z, \tag{17}$$

$$\mu_{\rm H} \equiv r\mu_{\rm con} = -\frac{1}{B}\frac{\Delta\beta}{\Delta\alpha_0}, \tag{18}$$

$$n_{\rm H}(z) \equiv n/r = \frac{B}{e}\frac{(\Delta\alpha_0)^2}{(\Delta z)(\Delta\beta)}, \tag{19}$$

$$\mu_{\rm GMR}(z) \equiv r(\xi+1)^{1/2}\mu_{\rm con} = \frac{1}{B}\left(1-\frac{\Delta\alpha}{\Delta\alpha_0}\right)^{1/2}, \tag{20}$$

where the subscript zero denotes a measurement at $B=0$.

A. GMR profiling

Because of the high aspect ratio w/l the Hall field E_y is effectively shorted by the source and drain contacts in the FET structure [Fig. 1(b)]. Then

$$\alpha = I_x/wE_x = lI_x/wV_x = (a-z)/\rho_{\rm av}, \tag{21}$$

so that

$$\begin{aligned}\mu_{\rm GMR}(z) &= \frac{1}{B}\left(1-\frac{\Delta(I_x/V_x)}{\Delta(I_{x0}/V_{x0})}\right)^{1/2} \\ &= \frac{1}{B}\left(1-\frac{\Delta(1/\rho_{\rm av})}{\Delta(1/\rho_{0\rm av})}\right)^{1/2}, \end{aligned} \tag{22}$$

where $\rho_{\rm av}$ is the *average* resistivity of the remaining (undepleted) layer. If V_x is held constant, then we can also write

$$\mu_{\rm GMR}(z) = \frac{1}{B}\left(1-\frac{g_m}{g_{m0}}\right)^{1/2}, \tag{23}$$

where $g_m \equiv \Delta I_x/\Delta V_{SG}$, the transconductance. Equation (23) is the form used by Jay and Wallis.[6]

B. Hall-effect profiling

For the Hall-effect structure, Fig. 1(a), we can impose the condition $I_y = 0$. Then

$$\alpha = \frac{I_x/wE_x}{1+E_y^2/E_x^2} = \frac{lI_x/wV_x}{1+l^2V_y^2/w^2V_x^2} = \frac{(a-z)/\rho_{\rm av}}{1+\mu_{H\rm av}^2B^2}, \tag{24}$$

$$\begin{aligned}\beta &= \frac{I_xE_y/wE_x^2}{1+E_y^2/E_x^2} = \frac{l^2I_xV_y/x^2V_x^2}{1+l^2V_y^2/w^2V_x^2} \\ &= \frac{(a-z)\mu_{\rm Hav}B/\rho_{\rm av}}{1+\mu_{\rm Hav}^2B^2}, \end{aligned} \tag{25}$$

and

$$\begin{aligned}\sigma(z) &= -\frac{l}{w\Delta z}\Delta(I_{x0}/V_{x0}) = -\frac{(a-z)}{\Delta z}\Delta(1/\rho_{0\,\rm av}), \\ \mu_{\rm H}(z) &= -\frac{1}{B}\frac{\Delta[l^2I_xV_y/w^2V_x^2(1+l^2V_y^2/w^2V_x^2)]}{\Delta(lI_{x0}/wV_{x0})} \\ &\simeq -\frac{\Delta[\mu_{\rm Hav}/\rho_{\rm av}(1+\mu_{\rm Hav}^2B^2)]}{\Delta(1/\rho_{0\rm av})} \simeq -\frac{\Delta(\mu_{\rm Hav}/\rho_{\rm av})}{\Delta(1/\rho_{0\rm av})}, \end{aligned} \tag{26}$$

$$\begin{aligned}n_{\rm H}(z) &= \frac{B}{e\Delta z}\frac{[\Delta(lI_{x0}/wV_{x0})]^2}{\Delta[l^2I_xV_y/w^2V_x^2(1+l^2V_y^2/w^2V_x^2)]} \\ &= \frac{(a-z)}{e\Delta z}\frac{[\Delta(1/\rho_{0\rm av})]^2}{\Delta[\mu_{\rm Hav}/\rho_{\rm av}(1+\mu_{\rm Hav}^2B^2)]^2} \end{aligned} \tag{27}$$

$$\simeq \frac{(a-z)}{e\Delta z}\frac{[\Delta(1/\rho_{0\rm av})]^2}{\Delta(\mu_{\rm Hav}/\rho_{\rm av})}. \tag{28}$$

The final approximate forms of Eqs. (27) and (28) should be good enough for most purposes, since the whole analysis breaks down anyway unless $\mu^2B^2 \ll 1$.

C. Capacitance-conductance profiling

The Schottky-barrier gate of Fig. 1(b) will have a capacitance C given by

$$C = \varepsilon A/z, \tag{29}$$

where ε is the low-frequency dielectric constant, and $A \simeq wl$ is the area of the capacitor. It may be shown, in the abrupt-junction approximation, that[3]

$$n(z) = \frac{1}{\varepsilon eA^2}\frac{C^3}{(dC/dV_{SG})}. \tag{30}$$

By combining Eqs. (26) and (30), we get

$$\mu_{\rm CC}(z) = \mu_{con}(z) \equiv \sigma(z)/en(z) = -\frac{\varepsilon l^3w\Delta(I_{x0}/V_{x0})}{C^3\Delta z}\frac{dC}{dV_{SG}}. \tag{31}$$

From Eq. (29) we get $\Delta z = -(\varepsilon A/C^2)(dC/dV_{SG})\Delta V_{SG}$ so that, if V_{x0} is constant with change in V_{SG},

$$\mu_{\rm CC}(z) = \frac{l^2}{CV_{x0}}\frac{\Delta I_{x0}}{\Delta V_{SG}} = \frac{l^2}{CV_{x0}}g_m, \tag{32}$$

where g_m is the transconductance, defined earlier. Equation (32) was first derived by Hsu and Scott.[7] Either this equation or the previous one may be used to determine $\mu_{\rm CC}(z)$. Note that the capacitance-conductance method gives the conductivity mobility directly. Corrections to ΔI_{x0} due to finite gate current and parasitic resistances will be given in the next section.

D. Gate-current and parasitic resistance effects

The quantities I_x, V_x, and V_y referred to in the previous section denote the current and voltage drop in the conductive layer (channel) under the depletion region. The quantities actually measured, however, are somewhat different.

For the FET structure, Fig. 1(b), we can measure only V_{SG}, V_{SD}, I_S, I_D, and I_G, while for the Hall-effect structure, we can additionally measure V_x and V_y because of the side arms, which carry no current. By use of a detailed effective-circuit analysis, published elsewhere,[8] it can be shown that the *average* channel current is approximately given by

$$I_{x\,\mathrm{avg}} \equiv I_{SDG} = \frac{I_S + I_D}{2} - \frac{I_G}{2} f(\alpha),\ \alpha = \frac{eV_{SD}}{2kT}, \tag{33}$$

where $f(\alpha) = \coth\alpha - \alpha^{-1}$, and the total channel voltage can be written

$$V_x = V_{SD} - I_{SD} R_P, \tag{34}$$

where $I_{SD} = (I_S + I_D)/2$, and R_P is the parasitic resistance, including contact, access, and ammeter resistances. [The "α" in Eq. (33) should not be confused with the "α" in Eq. (13).] It is assumed that the structure is symmetric, so that the parasitic contribution on the source side is identical to that on the drain side. Also, Eq. (33) is derived under the constant-electric-field approximation, already made for the profiling theory. Such an approximation is justified for purposes of this calculation if the term involving I_G in Eq. (33) is only corrective, i.e., if $I_G f(\alpha)/2 \ll I_{SD}$. The quantity $f(\alpha)$ is plotted in Fig. 2. As can be seen, if $V_{SD} \lesssim 50$ mV, then $f(\alpha)/2 \lesssim 0.15$, and $I_G f(\alpha)/2 \ll I_{SD}$, even if $I_G \simeq I_{SD}$. Usually, the GMR signal-to-noise ratio is quite good for $V_{SD} \simeq 10$–50 mV.

If it is also true that $\Delta(I_G f(\alpha)/2) \ll \Delta I_{SD}$, then we can show that, for the GMR case, with V_{SD} constant,

$$\begin{aligned}\frac{\Delta(I_x/V_x)}{\Delta(I_x/V_x)_0} &= \frac{\Delta I_{SDG}(B)}{\Delta I_{SDG}(0)} \frac{R_T^2(B)}{R_T^2(0)} \frac{R_C^2(0)}{R_C^2(B)} \\ &= \frac{\Delta I_{SDG}(B)}{\Delta I_{SDG}(0)} \frac{R_T^2(B)}{R_T^2(0)} \frac{1}{1+\mu_{\mathrm{avg}}^2 B^2} \\ &= \frac{\Delta I_{SDG}(B)}{\Delta I_{SDG}(0)} F(B),\end{aligned} \tag{35}$$

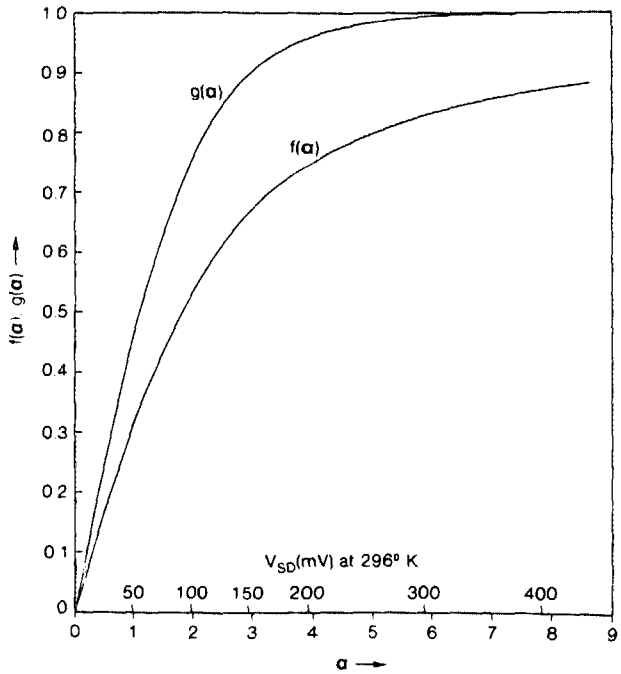

FIG. 2. Quantities $f(\alpha) = (\coth\alpha - \alpha^{-1})$ and $g(\alpha) = (\coth\alpha - \sinh^{-1}\alpha)$ vs α, and vs $V_{SD} \equiv 2kT\alpha$.

where $R_T = R_C + R_P \simeq V_{SD}/I_{SD}$, and μ_{avg} is an average channel mobility as defined in Ref. 8. Here R_C, R_P, and R_T are the channel, parasitic, and total resistances, respectively. For $R_P \ll R_C$, $F(B) \simeq 1$, but if not, an iterative procedure can be used to determine $F(B)$ at each gate voltage (see Ref. 8). We will show later, by a direct method, that $F(B)$ is close to unity for samples such as the ones discussed in this report, although a rapidly varying μ_{GMR} might require further consideration of this term. Thus, in most cases, we can write Eq. (22) as

$$\mu_{\mathrm{GMR}}(z) = \frac{1}{B}\left(1 - \frac{\Delta I_{SDG}(B)}{\Delta I_{SDG}(0)}\right)^{1/2}, \tag{36}$$

where I_{SDG} is defined in Eq. (33). Note that a typical V_{SD}, in practice, is about 30 mV, which leads to $\alpha \simeq 0.6$, $f(\alpha) \simeq 0.2$. Thus, $I_G f(\alpha)/2 \simeq 0.1\, I_G$.

For the capacitance-conductance (CC) profiling method, the considerations are basically the same as those given above for the GMR method. Equation (31) involves $\Delta(I_{x0}/V_{x0})$, and if $I_G f(\alpha)/2 \ll I_{SD}$ and $\Delta[I_G f(\alpha)/2] \ll \Delta I_{SD}$, then

$$\Delta(I_{x0}/V_{x0}) \simeq \frac{\Delta I_{SDG}}{V_{SD}} \frac{R_{T0}^2}{R_{C0}^2}, \tag{37}$$

where $R_T = R_C + R_P$ and $I_{SDG} = (I_S + I_D)/2 - I_G f(\alpha)/2$. Then,

$$\mu_{\mathrm{CC}}(z) = -\frac{\varepsilon l^3 w}{C^3 \Delta z} \frac{dC}{dV_{SG}} \frac{\Delta I_{SDG}}{V_{SD}} \frac{R_{T0}^2}{R_{C0}^2}. \tag{38}$$

This form of the parasitic-resistance correction was derived by Pucel and Krumm.[9] However, an important limitation in the accuracy of the CC mobility is its dependence upon capacitance measurements, which suffer if the series resistance is too high[10] or if the impurity profile is too abrupt.[11] Also, the effects of gate current upon C-V measurements have not been treated, although the charge-storage capacitance should be small for a Schottky-barrier device.[12] The GMR mobility suffers from no such limitations although, of course, the depth z is determined from capacitance measurements in both cases.

For the Hall-bar geometry, the situation is somewhat different. First of all, parasitic resistances are not important because two side arms, close to the middle of the sample, are used to measure the parallel voltage drop. Secondly, the perpendicular (Hall) voltage is also measured at the middle of the sample, so that it is the current near the middle, not the average current, that is important. As before, if the electric field in the channel is constant, then by using the techniques of Ref. 8 it can be shown[13] that the current at midchannel is

$$I_{x\,\mathrm{mid}} = I_{SD} - \frac{I_G}{2} g(\alpha),\ \alpha = \frac{eV_{SD}}{2kT}, \tag{39}$$

where $I_{SD} = (I_S + I_D)/2$, and $g(\alpha) = \coth\alpha - \sinh^{-1}\alpha$. Thus, for the Hall-effect formulas, Eqs. (26)–(28), we directly measure V_x and V_y, and determine I_x from Eq. (37). The quantity $g(\alpha)$ is plotted in Fig. 2.

Unfortunately, the Hall-bar geometry with its long narrow gate, can lead to relatively high ratios of I_G/I_{SD} and $\Delta I_G/\Delta I_{SD}$ at low source-drain voltages and high forward-bias gate voltages, say $V_{SD} \simeq 30$ mV and $V_{SG} \gtrsim 0.5$ V. This

problem can be circumvented by going to higher V_{SD}, but then the restriction $V_{SD} \ll 2|V_{SG} - 0.75\ \text{V}|$ may be violated, so that the depletion layer is not of uniform thickness. Basically, as with the GMR case, we should worry about the approximation of constant electric field when the corrective terms are large, i.e., when $I_G g(\alpha)/2 \simeq I_{SD}$ or when $\Delta(I_G g(\alpha)/2) \simeq \Delta I_{SD}$. Note that $g(\alpha) > f(\alpha)$ for all α so that the Hall-effect case involves larger gate-current corrections than the GMR case.

IV. RESULTS AND DISCUSSION

A FET-type active layer ($n \simeq 10^{17}\ \text{cm}^{-3}$) was formed in a Cr-doped, semi-insulating GaAs wafer by direct implantation of $4 \times 10^{12}/\text{cm}^2$, 100-keV Si ions, with subsequent capping and annealing for activation. A test pattern, containing a gated Hall bar, as well as several FET geometries, was fabricated onto this wafer. A separate "fat" FET, isolated from the other devices, was used for simultaneous C-V measurements, so that n and z were always determined along with the mobilities. The entire experiment was performed automatically with a PDP-11-03 computer.

The currents I_S and I_D were measured by switching a Keithley 619 ammeter between source and drain circuits. The gate current I_G was determined either from the relationship $I_G = I_S - I_D$, or from a separate ammeter in the gate circuit. The highest source-gate voltage employed was about 0.6 V, which limited the acceptable source-drain voltages to $V_{SD} \ll 2|V_{SG} - 0.75\ \text{V}| \simeq 300\ \text{mV}$, in order to keep z relatively constant over the channel length.

A. Gate-current corrections

We consider the GMR-mobility data, shown in Fig. 3. A fat FET, with a 50×400-μm gate, was used for these measurements. The voltages were $V_{SD} = 30$ mV, $V_{SG} \simeq -1.2$–0.53 V. At $V_{SG} = 0.53$ V, the currents were $I_{SD} \simeq 79\ \mu\text{A}$ and $I_G \simeq 46\ \mu\text{A}$, so that I_G was an appreciable fraction of I_{SD}. Since $\alpha \simeq 0.6$, and $f(\alpha) \simeq 0.2$, the quantity $I_G f(\alpha)/2$ was less than $5\ \mu\text{A}$, only a 6% correction to I_{SD}. However, $\Delta(I_G f(\alpha)/2)$ was comparable to ΔI_{SD}, due to the large values of $\Delta I_G/\Delta V_{SG}$ at these gate biases. (At $V_{SG} = 0.42$ V, I_G was down by an order of magnitude.) Note that the depletion depth at $V_{SG} = +0.53$ V is 0.087 μm, while the depletion depth at $V_{SG} = 0$ is about 0.16 μm. Thus, the use of forward bias has made possible the obtaining of information much closer to the surface, including the important implantation-peak region (about 0.08 μm) in this case. The curve designated μ-*SDG* in Fig. 3 is corrected according to Eq. (36), while the curve designated μ-S uses only the source current, with no correction for gate current. As can be seen, the correction to the mobility profile is considerable. Smaller FETs, on the same chip, give basically similar (within 10–15%) *corrected* mobility profiles, although the uncorrected profiles are much different. These results, as well as other data presented in Ref. 8, confirm the general correctness of the gate-current corrections, as given by Eq. (36). Note that certain regions of the C-V data in Fig. 3 may not be accurate due to abrupt-profile effects.[11] However, series-resistance effects[10] should not be important since $\omega RC < 0.1$ everywhere.

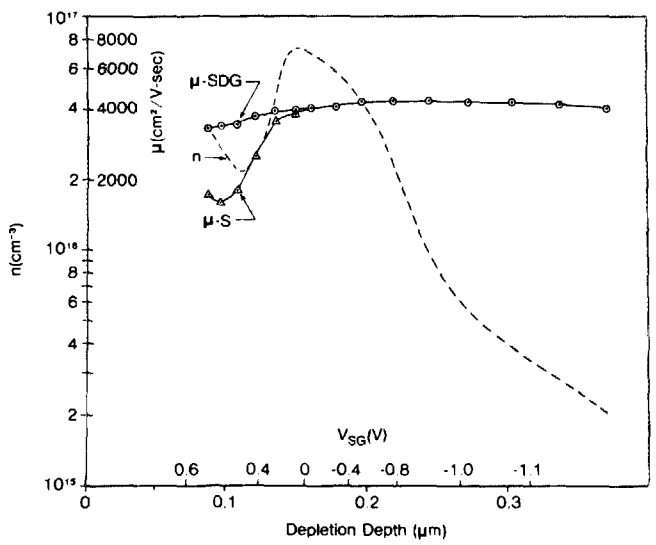

FIG. 3. Mobility (GMR) and carrier-concentration (C-V) profiles of an active layer formed by a 4×10^{12}-cm^{-2}, 100-keV Si implantation in GaAs. The μ-SDG curve is corrected for gate current, while the μ-S and n curves are not.

B. Parasitic-resistance corrections

In this section we will show by a direct method that the parasitic-resistance effects are quite small for the GMR method, and quite large for the CC method, at least for our material and test structures. To carry out this procedure, it is necessary to be able to separate R_T into its components R_C and R_P. Such a separation is difficult for the fat FET so it is necessary to employ two other structures on the test pattern, namely a 4×100-μm FET and a 10×100-μm FET, which have identical contact geometries and identical source-gate and gate-drain spacings. Thus, R_P should be the same for these two devices. By writing $R_T = R_P + R_C = R_P + lr_C$, where r_C is the channel resistance per unit length and l is the gate length, it is easy to show that $R_P = (5R_{T4} - 2R_{T10})/3$ where, for example, R_{T4} is the total resistance of the 4-μm device.

Plots of R_P and R_C vs gate bias for the 10-μm device are shown in Fig. 4, for $B = 0$. Here R_T is calculated from V_{SD} and I_{SD} ($R_T = V_{SD}/I_{SD}$) for each device, R_P is found from the relationship derived above, and $R_C = R_T - R_P$. It is seen that R_P is nearly constant ($135 \pm 15\ \Omega$) over a large range of gate bias, while R_C changes by a factor 5 over the same range. For $V_{SG} < -1.3$ V it is difficult to get an accurate value of R_P, since $R_P \ll R_C$ in this region. The observed behavior of R_P and R_C is exactly what we expect from our simple model and gives confidence that our separation procedure is credible.

With the knowledge of R_T/R_C vs V_{SG}, we can correct the CC profile, as shown in Eq. (38). These corrections can be very large for our 10-μm MESFET structure, ranging from 1.0, for $V_{SG} < -1.4$ V, to 2.3 at $V_{SG} = 0$ V. The corrected and uncorrected μ_{CC} profiles are shown in Fig. 5. Forward-bias results are not shown because the n-curve dip in this region (cf. Fig. 3) may be artificial. The capacitance per unit area of the 10-μm device was virtually the same as that for the fat FET. It is clearly seen that unless the test structure has $R_P/R_T \ll 1$, the CC method is quite inaccurate, except

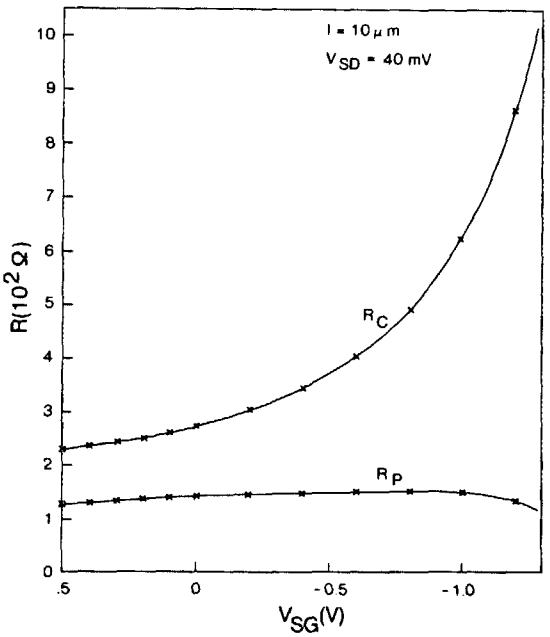

FIG. 4. Channel and parasitic resistances as a function of gate voltage for a 10×100-μm MESFET on the same wafer as the fat FET shown in Fig. 3. The source-drain voltage is 40 mV.

near pinch-off, and even then series resistance can cause the results to be questionable.

We now turn to the GMR case. Here, only the magnetic-field dependence of the ratio R_T/R_C is important, as seen from Eq. (35). This dependence was checked at 10 kG, the same field as that used for the μ_{GMR} measurements, and it was found that $F(B)$ ranged from 1.008 to 0.982, as V_{SG} ranged from 0.5 to -1.4 V. The corrections to μ_{GMR} are less than 4.7% over the entire profile, as shown in Fig. 5. It is interesting that Jay and Wallis[6] also report parasitic-resistance effects of less than 5%. Thus, parasitic-resistance effects do not seem to be very important in the GMR method, either for the sample studied here or for a wide variety of other samples that we and others[6] have tested. However, this situation may not hold for a sample which has a very strong mobility variation.

The Hall-mobility profile, also shown in Fig. 5, was measured on a device similar to that shown in Fig. 1(a). Unfortunately, at low V_{SD}, signal-to-noise was poor and the corrections were very large. For example, even for a V_{SD} of

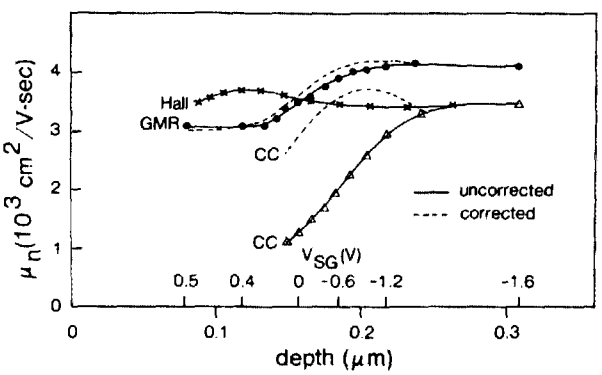

FIG. 5. Hall, GMR, and capacitance-conductance (CC) mobilities as a function of gate voltage. The GMR and CC data are from the same 10×100-μm MESFET as that shown in Fig.4. The dotted lines denote data corrected for parasitic resistance effects.

100 mV, I_G was larger than I_{SD}, and $\Delta(I_G g(\alpha)/2)$ was *much* larger than ΔI_{SD}, at $V_{SG} = 0.53$ V. The data shown are for $V_{SG} = 300$ mV, which gives $\Delta(I_G\, g(\alpha)/2) \simeq \Delta I_{SD}$ at about $V_{SG} \simeq 0.55$ V. The Hall-bar geometry, shown to scale in Fig. 1(a) ($l \simeq w \simeq 30\,\mu$m), is not ideal because of the width of the side arms ($10\,\mu$m). Another geometry is now being designed, and will be tested soon.

It is interesting to compare the corrected Hall, GMR, and CC mobility profiles, shown in Fig. 5. All three methods give a rather flat profile at depths greater than 0.2 μm. The difference in absolute magnitudes should perhaps not be considered significant, given the nonideal designs involved. In fact, the corrected CC profile is quite similar to the GMR profile over its entire range, except for being lower by 15–20%. The downward turn of the GMR and CC mobilities at depths less than 0.15 μm is not unexpected since the implanted-ion concentration and damage are peaking in this range. Again, the Hall mobility data in this region are almost certainly inaccurate because of the high V_{SD} which was necessary to get a reasonable signal-to-noise ratio at forward bias. However, it should be noted that the only totally unreasonable mobility values shown in Fig. 5 are those from the *uncorrected* CC technique, in the zero-bias region. Therefore, those using this technique should make sure that either the parasitic resistance of their test structure is negligible, or it is easily measurable. Otherwise, the results could be quite misleading.

In summary, we have developed a theoretical framework for determining mobility profiles by the Hall-effect, geometric-magnetoresistance, and capacitance-conductance techniques. Our treatment includes finite gate-current effects, which allow the extraction of data much closer to the surface than was possible before, and parasitic-resistance effects. From a practical point of view, the GMR technique seems to have advantages over the other two, because the Hall method is harder to implement, and the CC method is fraught with inaccuracies, some inherent, and some perhaps due to our particular design structure.

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