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Seamless On-Wafer Integration of Si(100) MOSFETs and GaN HEMTs

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***Abstract*—The first on-wafer integration of Si(100) MOSFETs and AlGaN/GaN high electron mobility transistors (HEMTs) is demonstrated. To enable a fully Si-compatible process, we fabricated a novel Si(100)–GaN–Si(100) virtual substrate through a wafer bonding and etch-back technique. The high thermal stability of nitride semiconductors allowed the fabrication of Si MOSFETs on this substrate without degrading the performance of the GaN epilayers. After the Si devices were fabricated, the nitride epilayer is exposed, and the nitride transistors are processed. By using this technology, GaN and Si devices separated by less than 5 μm from each other have been fabricated, which is suitable for building future heterogeneous integrated circuits.**

***Index Terms*—GaN, heterogeneous integration, high electron mobility transistor (HEMT), metal–oxide–semiconductor field-effect transistor (MOSFET), Si(100), virtual substrate.**

I. Introduction

THE integration of III–V compound semiconductors and silicon (100) CMOS technologies has been a long pursued goal. A robust heterogeneous integration technology would make the outstanding analog and mixed-signal performance of compound semiconductor electronics available to design these key functions on VLSI chips that are difficult to implement in Si technology.

GaN-based devices are one of the best candidates for integration with Si. While Si electronics has shown unsurpassed levels of scaling and circuit complexity, GaN devices offer excellent high-frequency/power performance as well as outstanding optoelectronic properties [1], [2]. The ability to combine these two material systems in the same chip and in very close proximity would allow unprecedented flexibility for advanced applications.

Previously, several authors have reported heterogeneous integration of Si and GaAs devices (i.e., field-effect transistors and light-emitting diodes) by the low-temperature selective epitaxial growth of GaAs on a *miscut* Si(100) substrate [3]–[5]. With similar technology, several groups have reported the growth of GaN structures on *miscut* Si(100) or Si(110) substrates by molecular beam epitaxy [6], [7] and metalorganic vapor phase epitaxy [8], [9]. However, this approach is challenging because of the difficulty of growing high-quality Wurtzite GaN on these substrates [9]. Moreover, the use of miscut substrates increases the density of surface states in the Si material, degrading the performance of Si electronics designed therein.

A different approach to achieve the heterogeneous integration of GaN and Si involves transferring an already grown GaN epilayer onto a Si(100) substrate through the removal of the original substrate and subsequent bonding to the Si(100) wafer. Laser lift-off and Au/In/Au bonding layer were used in [10]. Wafer bonding of GaN with Si substrates using $PdIn_3$ and AuGe as an interlayer has also been reported in [11] and [12]; however, none of these hybrid wafers satisfies the thermal budget of Si processing ($\sim$1000 °C) since the melting points of $PdIn_3$ and AuGe are $\sim$660 °C and $\sim$360 °C, respectively. Recently, our group demonstrated the robust wafer bonding of GaN and Si(100) wafers through the use of a SiO_2 interlayer [13]. The thermal stability of this bonding was successfully tested up to 1000 °C, a sufficient thermal budget for Si and GaN processing.

In this letter, we demonstrate the first integration of Si(100) MOSFETs and GaN high electron mobility transistors (HEMTs) on the same wafer in very close proximity. The key enabling technology is the fabrication of a Si(100)–GaN–Si(100) virtual substrate through a wafer bonding and etch-back process. On this substrate, standard Si MOSFETs were first fabricated. Then, the top Si layer was locally removed, exposing the AlGaN surface, and GaN HEMT devices were processed in those regions. It should be highlighted that in our technology, the Si devices are fabricated on Si(100) wafers without any miscut and following a conventional Si process flow. Due to the very high thermal stability of GaN [14], this process did not adversely affect the electrical properties of the embedded GaN layer.

II. Device Fabrication

Fig. 1 summarizes the main steps of the fabrication of Si(100)–GaN–Si(100) virtual substrates. The Si(100)–GaN–Si(100) virtual substrate fabrication begins with the epitaxial growth of an AlGaN/GaN transistor structure on a Si(111) substrate by metal–organic chemical vapor deposition at Nitronex Corporation. In these samples, the AlGaN barrier had a total thickness of 175 Å and an Al composition of 26%. Our technology then removes the original Si(111) substrate and applies wafer bonding twice to have Si(100) substrates on both the

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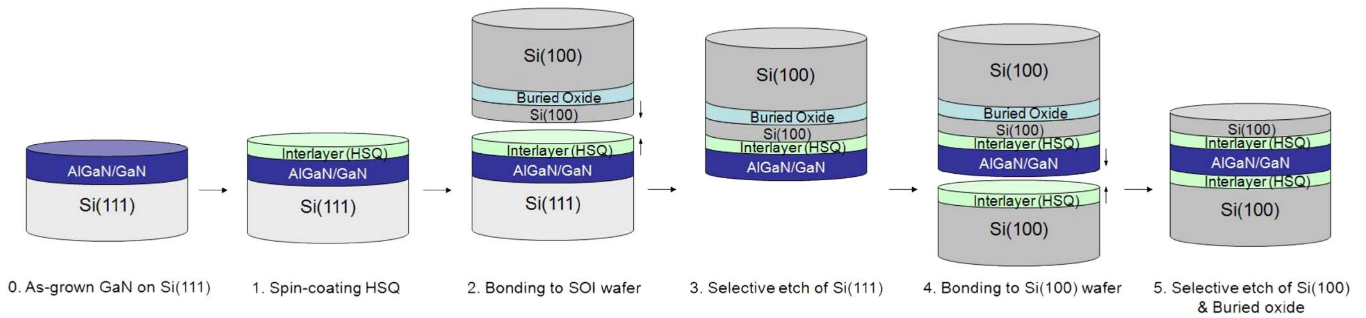

Fig. 1. Schematic illustration of the main processing steps in the fabrication of Si(100)–GaN–Si(100) virtual substrates through the layer transfer technology described in [13]. The thin top Si(100) layer is obtained from the active Si layer of a silicon-on-insulator wafer. The doping of this layer sets the nMOS or pMOS character of the fabricated devices. The Si(111) substrate removal in step 3 is performed in a deep reactive ion etch system using an SF_6-based plasma. The fabrication process of the Si–GaN–Si virtual substrates can be simplified by leaving the Si(111) substrate and skipping steps 3 and 4.

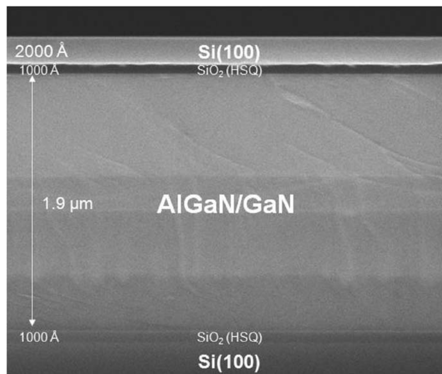

Fig. 2. Cross-sectional SEM image of the Si–GaN–Si virtual substrate.

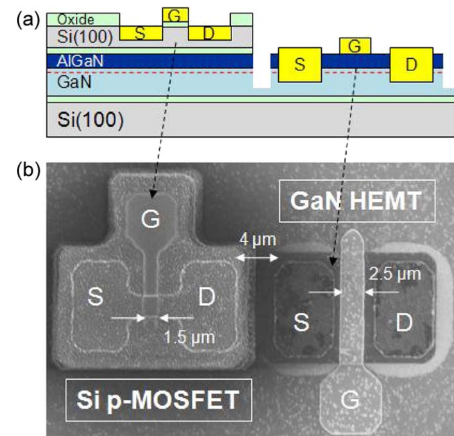

Fig. 3. (a) Cross-sectional schematic of fabricated Si p-MOSFETs and GaN HEMTs. (b) Plan-view SEM image of the fabricated transistors.

top and bottom sides of the AlGaN/GaN layer. The top Si(100) layer has a thickness of 200 nm and a donor doping concentration of 10^{15} cm^{-3}. Our wafer bonding technology has been described in [13], and it is based on spin-coating the GaN wafer with hydrogen silsesquioxane (HSQ), followed by thermal compression with the Si wafer at 400 °C for 1 h. HSQ is a flowable oxide with excellent thermal stability, which withstands the high thermal budget required during the processing of both Si and GaN devices (i.e., > 1000 °C). Following this technology, hybrid wafers with 1-in diameter have been obtained.

Once the virtual substrate has been fabricated (Fig. 2), device processing starts with the fabrication of Si p-MOSFETs. Device isolation was achieved by a field oxide, and a 10-nm gate oxide was formed by plasma-enhanced chemical vapor deposition (PECVD). Undoped polycrystalline Si was subsequently deposited and anisotropically etched in a Cl_2 plasma to form the gate contact. The source, drain, and gate implantation was achieved at the same time with a species of BF_2, a dose of 4×10^{15} cm^{-2}, and an implantation energy of 10 keV.

To fabricate GaN HEMTs, the AlGaN/GaN layer embedded in the virtual substrate was exposed by etching the top Si(100) and HSQ layers using SF_6 plasma followed by buffered oxide etchant in those regions where GaN devices are to be located. The etch selectivity between Si/SiO_2 and AlGaN is excellent, and a smooth AlGaN surface was obtained after the etch. Once the AlGaN/GaN layer is exposed, the fabrication of GaN HEMTs is identical to a standard GaN HEMT process. A Ti/Al/Ni/Au multilayer was first deposited for the ohmic contacts. Ohmic metal alloying in the GaN HEMTs and dopant activation in the Si p-MOSFETs were simultaneously accomplished by rapid thermal annealing at 870 °C for 30 s in N_2 atmosphere. A Cl_2/BCl_3 plasma was used for the mesa isolation of the HEMT devices, and then, a 2–3-μm-long gate was formed by photolithography and Ni/Au/Ni metallization. Fig. 3 shows a scanning electron micrograph (SEM) image of the integrated Si p-MOSFETs and GaN HEMT devices after this step. The separation between these two devices is just 4 μm. Finally, 500 nm of SiO_2 passivation layer was deposited by PECVD, contact vias were opened in the dielectric, and the contact pads and interconnections were metalized with Ti/Al.

III. Results and Discussion

The drain current versus drain voltage characteristics, as well as the transfer characteristics, of a typical Si p-MOSFET and GaN HEMT fabricated using the technology described earlier are shown in Fig. 4. Both devices have good modulation of the drain current by the gate contact as well as low off-currents. However, the long gate lengths of these devices limited their maximum output current. The use of a shorter gate length and higher doping levels in the Si active layer is expected to improve the performance of the MOSFETs, and it is part of our on-going work.

The effect of the entire fabrication process to the transport properties of the AlGaN/GaN epilayer was evaluated by

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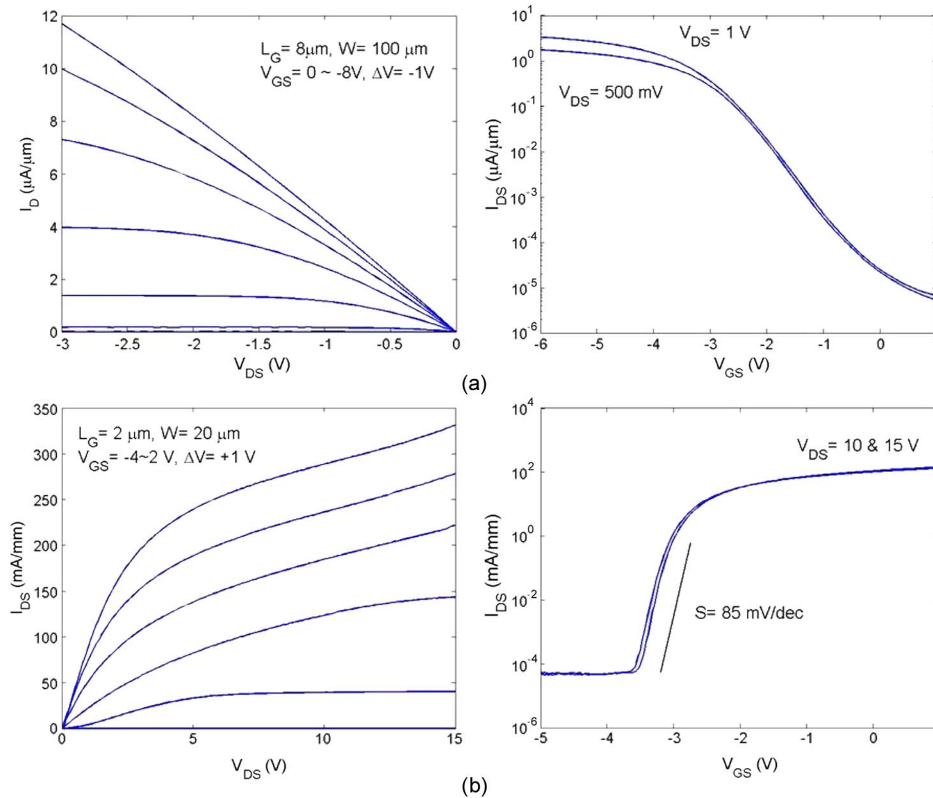

Fig. 4. (a) DC current–voltage characteristics (left) and transfer curve (right) of a long-channel Si p-MOSFET ($L_G = 8\ \mu$m). (b) DC current–voltage characteristics (left) and transfer curve (right) of a GaN HEMT ($L_G = 2\ \mu$m).

transfer length measurements and compared to conventional devices. The contact resistance (R_c) did not change ($0.3 - 0.4\ \Omega \cdot$ mm); however, the sheet resistance ($R_{\rm sh}$) was reduced by 24%, from 476 to 364 Ω/sq. This improvement in $R_{\rm sh}$ is due to the layer transfer process, and it was also reported in [13].

IV. Conclusion

We have demonstrated the first on-wafer integration of GaN-based devices and Si(100) electronics through a fully Si-compatible process. This integration allows device-level integration of compound semiconductors (transistors, LEDs, lasers, etc.) and Si-based transistors on the same wafer to enable revolutionary advances in circuits and systems. Some of the applications envisioned for this integration include high-power integrated wireless transmitters, power gating and power conversion circuits, and in-chip optical interconnections where the optoelectronic devices are made of nitride semiconductors and the digital circuit is based on Si devices.

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