SELECTIVE ELECTROLESS NICKEL PLATING ON OXYGEN-PLASMA-ACTIVATED GOLD SEED-LAYERS FOR THE FABRICATION OF LOW CONTACT RESISTANCE VIAS AND MICROSTRUCTURES

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ABSTRACT

This paper presents a novel technique to selectively deposit nickel by electroless plating on gold seed layers using an oxygen-plasma-activation step. No prior wet surface pre-treatments or metal oxide etches are required. This enables the manufacturing of low-resistance vias for heterogeneous three-dimensional (3D) integration of MEMS but it is also a suitable technique for the fabrication of arbitrary shaped nickel-microstructures using chemically stable and cost-effective electroless nickel plating baths.

INTRODUCTION

Common fabrication methods for large-scale metal vias are the electrodeposition of copper or gold. Especially the electroplating of copper is very well established due to its processability of high aspect ratio features at close to room temperature conditions [1]. An alternative approach is the use of electroless plating technologies, which do not require an interconnected seed-layer as plating electrode and therefore benefits from a less complex process and less elaborate requirements on the plating-equipment in comparison to electroplating. However, electroless plating processes for microstructures are not well established yet due to chemical instabilities and hazardous ingredients typically found in copper- and gold-plating solutions. Electroless nickel plating is a well-established low-cost and non-hazardous process and plated nickel is used for macroscopic surface coatings for wear and corrosion protection [2], as a diffusion barrier for solder [3] and in MEMS as a structural- and actuator-material [4, 5, 6].

The electroless deposition of nickel with hydrophosphite-based plating solutions can be spontaneously induced on seed-layer metals of group VIII (Fe, Co, Ni, Rh, Pd, Pt) [2]. The general drawback of these native seed-layer metals is their native oxide and/or bad processabilty and availability. The native oxide layer on top of a seed-layer metallization induces several problems such as the prevention of a well controlled start of the autocatalytic plating process, poor electrical performance due to high interface resistances as well as bad adhesion of the plated layer to the seed-layer. Electroless nickel plating on other, inactive seed-layers such as silicon [6, 7], aluminum [8] and dielectrics [9] require special activation processes. These pre-treatments consist typically of numerous wet process steps with activator solutions, which contain acids and catalyzation agents such as palladium and tin chlorides. However, these solutions typically activate all exposed surfaces and thus additional lithographic process steps are necessary for the selective deposition of nickel [6, 7].

Gold as an inert and highly conductive metal does not form a native oxide layer and thus is very attractive to overcome the stated problems, which are caused by common seed-layer materials. However, gold is not a native seed-layer for hydrophosphite-based electroless nickel plating solutions and therefore requires a pre-treatment in order to induce the autocatalytic plating process. In this paper we present a novel and entirely dry surface activation method for selective electroless plating of nickel on gold seed-layers, which does not contain any laborious wet and/or acidic process steps.

DESIGN AND FABRICATION

The investigations within this work have been focused on vertical interconnections (vias). Heterogeneous 3D integration concepts for MEMS and ICs use vias as electrical and physical connections between layers on different levels, as depicted in Fig. 1 [10].

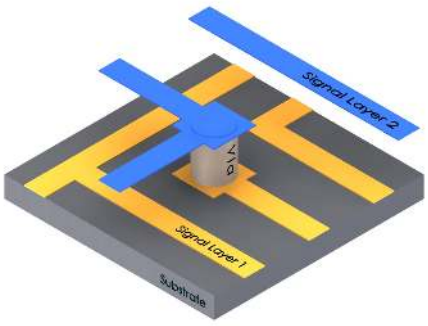


Figure 1: Schematic of a via vertically interconnecting a signal layer with another (released) layer.

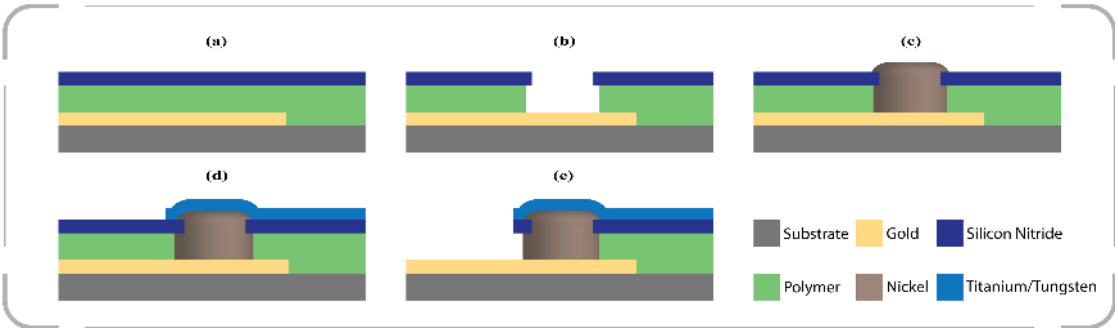


Figure 2: Cross section of the fabrication scheme for selective plating of nickel vias.

The vias must provide both good ohmic contacts and structural integrity in order to provide a stable platform for the MEMS structures. The design of the test structures therefore consist of two major elements in order to characterize selectively deposited micro-scaled vias with dimensions from 0.5 to 5 µm. First is the electrical characterization with the help of Kelvin test structures (Fig. 3) for the evaluation of the resistance of the via and the interface resistance to the seed layer and the top-metallization. Second is the characterization of the plating process with the help of arrays consisting of vias of different dimensions, shapes and pitches (squares and circles with edge-lengths/diameters from 0.5 to 5 µm) (Fig. 2). These structures provide information about the electroless nickel plating process and its physical limitations, such as minimum feature size, plating uniformity and characteristics.

The fabrication process of the vias is depicted in Fig. 2 and is based on standard 500 µm thick single-side polished 100 mm-substrates with a 2.5 µm thick silicon oxide layer (not shown in Fig. 2), which acts as an electrical insulation of the seed layer to the substrate. The gold seed-layer and its adhesion promotion layer (TiW, not shown in Fig. 2) is deposited and structured with the help of a lift-off process. A thermosetting polymer (mr-I 9150 XP, [10]) is subsequently spun-on and hard-cured. A silicon nitride layer, which is deposited by a PECVD process acts as a hardmask for the etch of the via mold (Fig. 2 a). The silicon nitride layer is structured by stepper lithography and a standard dry etch. The etch of the polymer was performed in an oxygen plasma (AMAT P5000 MK2) with optimized parameters for an anisotropic etch process, which generates straight sidewalls in the via mold. Subsequently to the via mold formation the surface-activation of the seed-layer takes part in a mild oxygen plasma (Fig. 2 b). The plating process was conducted with a stirrer-hotplate which kept the temperature of the hydrophosphite-based electroless Ni plating solution (Durni Coat, DNC571, AIMT Holding GmbH) to 92°C (Fig. 2 c). The top-metallization layer was deposited by sputtering with a prior sputter etch without breaking the vacuum in order to remove the native oxide from the top-surface of the nickel via. A final photolithography and a dry etch forms the structures of the top-metallization (Fig. 2 d). In order to be able to electrically probe both the seed layer and the top-metallization the polymer was selectively removed by a second anisotropic plasma etch (Fig. 2 e).

EXPERIMENTAL RESULTS

In oder to acquire comparative results the entire characterization of the vias has been conducted both on gold and nickel seed-layers with an identical fabrication process.

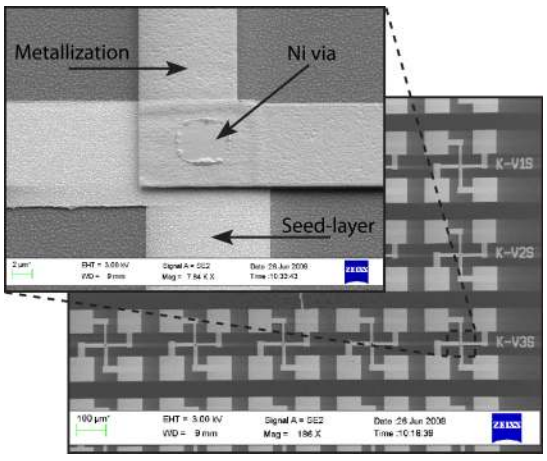


Figure 3: SEM images of the Kelvin test structures. The close-up shows the gold seed-layer, the square-shaped nickel via and the TiW-metallization on top of the polymer.

The substrates with gold seed-layers at the bottom of the via molds are immersed into the electroless nickel plating solution after prior activation in oxygen plasma. The activation step does not attack the polymer of the mold due to the very low RF-power of the plasma. The activation has been successfully established both with a TePla Model

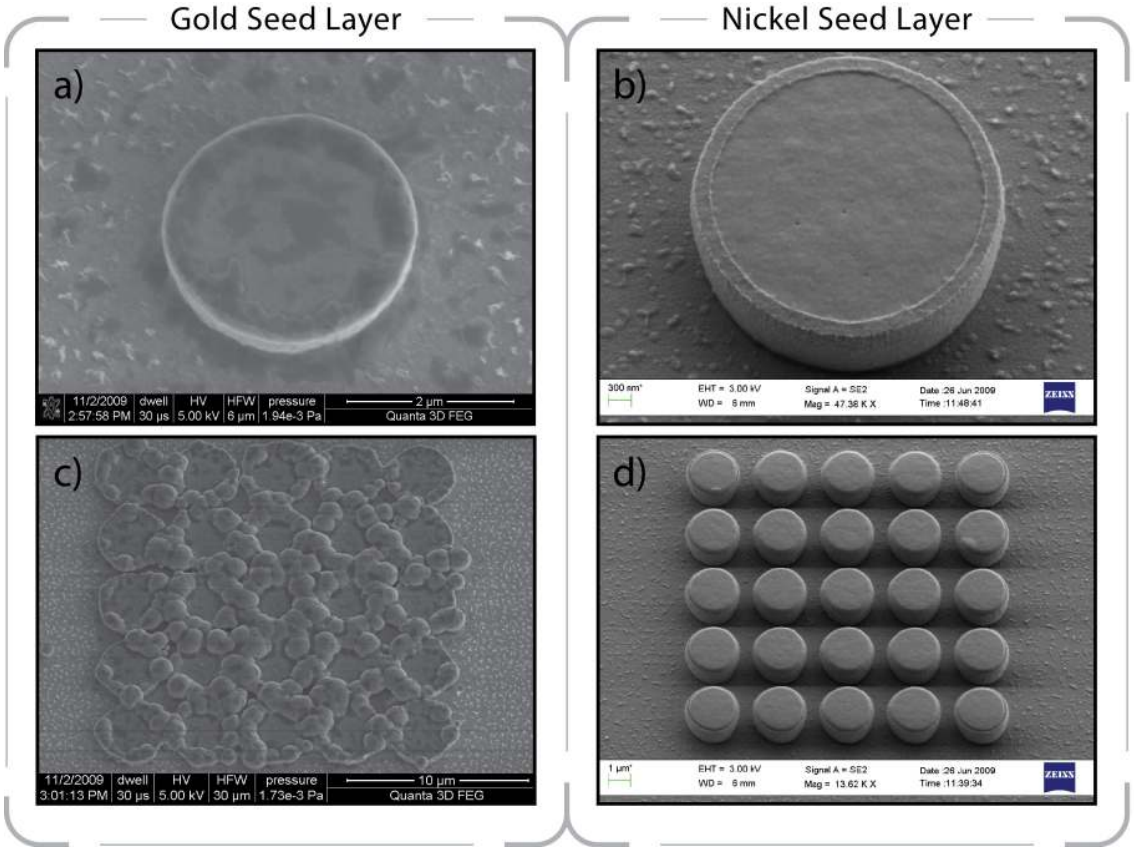
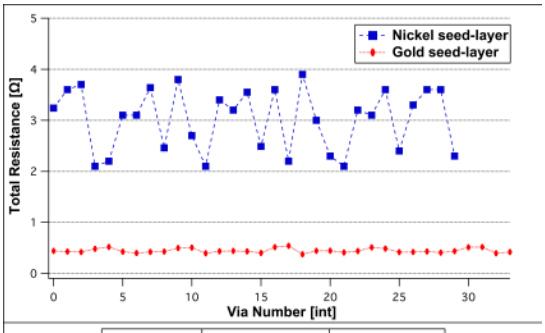


*Figure 4: a) single nickel via on gold seed-layer (*3 µm *diameter), b) single nickel via on nickel seed-layer (*1 µm *diameter), c) 5x5 array test structure (*3 µm *diameter,* 3 µm *pitch) on gold seed-layer, d) 5x5 array test structure (*3 µm *diameter,* 3 µm *pitch) nickel gold seed-layer*

300 Oxygen Plasma Reactor in barrel configuration (RF power 150 W, O_2 flow 140 mL/min, 6 min)) and a Surface Technology Systems (STS) Multiplex ICP (RF power 150 W, platen power 25 W, O_2 flow 50 mL/min, pressure 90 mTorr, time 6 min). The plasma treatment was found to be sufficient to induce the plating process on gold seed-layers, the theoretic chemical/physical background remains to be investigated. The surface remains activated for the plating process for about 45 min. The yield of the plating process decreases with the feature size of the plated structures. The threshold for a sufficiently high yield of nickel structures on plasma activated gold seed layers is a minimum feature size of 3 µm, whereas it is less than 1 µm for nickel seed layers, as shown in Fig. 3 b and d.

The electrical characterization of the vias was conducted with a 4-point probe station and a digital multimeter and was focused on square-shaped 3 µm-wide vias with a height of 1.5 µm. The 4-point measurement cancels out the metal-line-resistance so that the measured total resistance can be considered as the resistance of the plated nickel structure and its two interface resistances between the via and the seed-layer and between the via and



Seed-Layer	Resistance [Ω]	pre-treatment
Nickel	3.02 ± 1.81 (3σ)	dry/wet*
Gold	0.45 ± 0.13 (3σ)	dry

Figure 5: Comparative Kelvin-measurement of the total resistance of electroless nickel vias (square, 3 µm *width,* 1.5 µm *height) on two different seed layers. Electroless nickel plated structures on gold seed-layers show a significantly lower resistance and variance compared to nickel seed-layers.*
**) different pre-treatments have been investigated, displayed are the resistances with the best result*

the top-metallization. The total resistance of the vias on gold seed-layers showed very low values,

which are about seven times lower as compared to similar fabricated vias on nickel seed-layers. Also the variance of the measured total resistances was 50 % lower for vias on gold seed-layers (Fig. 5). The difference between the measured total resistance and the calculated resistance of the via itself (app. 0.1 Ω) can be assumed to be the two contact resistances with a clear predomination of the contact resistance to the seed layer. It was not possible to achieve comparable low resistances for nickel seed-layers, even with prior wet acidic pre-treatments with diluted HCl solutions (1:10 and 1:100 HCl:DI Water) in order to remove the native oxide of the nickel.

The morphology of the plated structures has been evaluated with the help of scanning electron microscopy (SEM) as shown in Fig. 4. The morphology of plated nickel structures varies, depending to the used seed-layer material. Vias, which were grown on gold seed-layers, as depicted in Fig. 4 a, have a rougher surface topology than vias, which were grown on nickel seed-layers, as shown in Fig. 4 b. The plating rate was in general higher and less controlled close to the edge of the structures, that were plated on gold seed-layers. This effect has no impact on the electrical functionality of the via but causes problems for small via pitches, where vias can be short-circuited, as shown in Fig. 4 c). The shape of the fabricated vias, whether square or circular, had in general no impact on the electrical performance and the material morphology. A comparative summary with qualitative characteristics of the characterization is given in Tab. 1.

Criteria	Nickel	Gold
contact resistance	-	+
total resistance variance	-	+
process controllability	+	+
via morphology	+	-
small feature sizes	+	-
small via pitches	+	-

Table 1: Qualitative summary of characteristics of electroless plated nickel vias on gold and nickel seed-layers.

DISCUSSION AND CONCLUSIONS

We demonstrate a novel and entirely dry pre-treatment method to selectively create low-resistance nickel vias on gold seed-layers with a commercial available hydrophosphite-based electroless nickel plating solution. The activation with a low-power oxygen-plasma was found to be sufficient to initiate the electroless plating on gold seed-layers as well as improving the yield on nickel seed-layers. The contact resistance of the plated structures on gold seed-layers were investigated and showed superior electrical characteristics in comparison to conventional nickel seed layers. The absence of a native oxide on gold seed-layers enables unlike other materials low interface resistances and therefore the realization of low-resistance electrical interconnects.

ACKNOWLEDGEMENTS

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