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Selective Glitch Reduction Technique for Minimizing Peak Dynamic IR Drop

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Abstract This paper proposes a glitch compensation technique which involves reducing glitch power in selected combinational cells to reduce peak current which contributes to dynamic voltage or IR drop. The proposed methodology can be seamlessly integrated to existing physical design flows. A glitch is an undesired transition that occurs before intended value in digital circuits. A glitch occurs in CMOS circuits when differential delay at the inputs of a gate is greater than inertial delay, which results into increased gate switching and hence notable amount of power consumption. When such large number of logic gates switch close to the same time they will contribute to power integrity challenge called peak dynamic IR drop. The glitch power is becoming more prominent in lower technology nodes. Introduction of buffers at the input of the Logic gate may reduce glitches, but it results into large area overhead and dynamic power. In the proposed methodology we are using transmission gate as a compensation circuit to reduce extra leakage and dynamic power. A flow is proposed for charactering the pass transistor logic to cater different delay values. The proposed methodology has been validated on a place and routed Multiply Accumulate (MAC) layout implemented using Synopsys SAED 90nm Generic library. Experimental results show 12% to 50% reduction in top 10 peak transient IR drop numbers with just 12% glitch power reduction in selected combinational cell instances. When compared to traditional on-chip decoupling capacitor (Decap) cells insertion method the proposed technique could reduce the peak IR drop numbers by the same amount with just 5% increase in total core capacitance.

Keywords Dynamic Power, Glitch Power, Switching Activity, IR Drop, Decoupling Capacitance

1. Introduction

The power spent in Complementary metal oxide semiconductor (CMOS) can be classified as dynamic power consumption and leakage or static power consumption. Leakage power is consumed at all times even in ideal states and it is dominating total power equation in advanced technologies. It is unnecessary and need to minimize it. On the other hand dynamic power consumption is due to the low impedance path between the rails formed through the switching devices. The switching at the output of logic gates can be due to desired functional transitions or due to spurious transitions called glitches. The glitches at the output of logic gates are due to differences in arrival times at various inputs. Glitch power in modern circuits account for 20% to 70% and it is 7% to 43%[1] of the dynamic power consumption. There are various published techniques to eliminate glitches in the logic circuits to accompany desired functioning of the logic circuit[2,3].

However glitches which occur close to the same time in data intensive architectures can cause peak dynamic voltage or IR drop power integrity challenges. This work proposes a selective glitch reduction technique to keep peak dynamic IR drop numbers within allowable limits using Synopsys design flow. The methods described here are based on the authors' research discussed in several papers[4, 5]. Rest of the paper is organized as follows. Section 2 presents background of the concept and definitions. Section 3 presents prior work and existing techniques for glitch reduction and motivation for proposed selective glitch reduction technique. Section 4 discusses proposed technique, flow and formulation. Section 5 discusses experimental results of proposed technique in comparison with Decap insertion technique and Section 6 concludes the work.

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2. Back Ground

2.1. Delay of a Gate

The primary contributing element in the design aspect for digital logic circuits is Gate. For a CMOS gate, the change in output signal follows the change in input signal with certain delay constraint. The on and off switching activity of the transistors in the logic gate depends on the slope of the input signals. So, the change in output signal depends on the low on resistance (R_{on}) path provided by the "ON" MOSFET and charging or discharging of the output load capacitance (C_L). The delay of a logic gate depends on the amount of resistance and capacitance offered by current path, is called gate delay or inertial delay. Gate delay or inertial delay can be defined as the time taken for a signal at the output of a gate to reach 50% of V_{dd} (logic 1 level) after the signal at the input of the gate reached 50% of Vdd. The inertial delay of logic gate is given by $R_{on} \times C_L$ (or stage delay), it can be varied by changing the width and length of the transistor[6].

2.2. Glitch and Dynamic Power

Glitches are the spurious transitions which occur due to difference in arrival times of signals at the gate inputs. These are not needed for the correct functioning of the logic circuit. Power consumed by glitches is called as Glitch power. Every signal net of a gate needs to be transmitted at most once in every clock cycle. But in the real scenario there are output transitions switching more than once in every clock cycle and these unnecessary transitions will also consume power and they contribute significantly to unexpected peak currents which are higher than that of original designs specifications. These peak currents occur in a very short period of time and bring about a large transient voltage or IR drop simultaneously. The IR drop is a power integrity issue and can impact circuit performance and reliability. So it is very advantageous to eliminate glitches in the circuits as power consumption is critical in today's chips. The flow of glitch in a digital logic circuit gate is shown in Fig (1),[7]. In a logic gate, the number of edges in the transients at the output of the gate may equal to the number of arriving signals at the gate. The maximum difference in the arrival time of the signals at the inputs of the gate is called as differential path delay. It is also the maximum width of the possible glitch at the circuit output. Consider Fig. 1, in the circuit we can see the unbalanced arrival times of the inputs due to the inverter circuit in the lower input path of the NAND gate. Thus the differential delay of the NAND gate is 2 units.

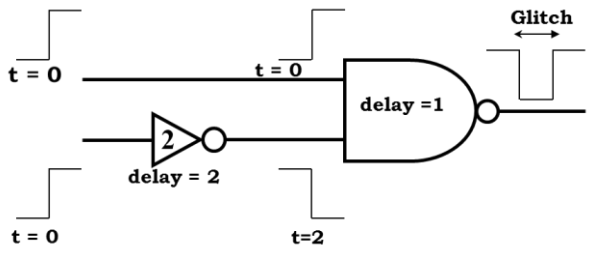

Figure 1. Circuit showing the formation of glitches. The inverter has a delay of 2 units and the NAND gate has a 1 unit delay. Due to differing arrival times at the inputs of the NAND gate, the output produces a glitch consisting of two transitions

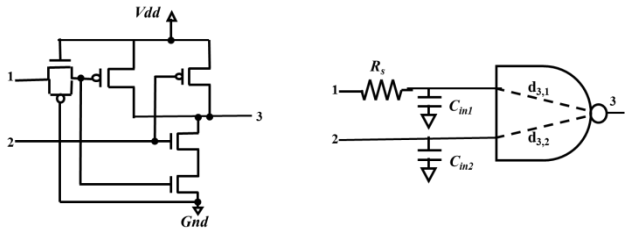

Figure 2. Schematic of a conventional 2-input CMOS NAND gate, with varying input delays by always-on CMOS transmission gate

This differential delay makes the NAND gate to switch 2 times more than the required functioning forming spurious transitions at the output which consume some dynamic power.

3. Prior Work and Motivation

3.1. Glitch Reduction

Till now there are have been many techniques developed to eliminate glitches in a logic circuit, like delay balancing, hazard filtering, gate sizing, transistor sizing and minimum dynamic power LP technique etc.

1. *Delay balancing:* In this method the inputs are made to arrive at the same time by inserting extra delay buffers on selected paths[8].
2. *Hazard filtering:* In this method the gate delay is made greater than the differential delay at the inputs of the gate to filter the glitch[9].
3. *Gate sizing:* In this method every gate is assumed to be an equivalent inverter[10].
4. *Transistor sizing:* This method treats every transistor's size as a variable and tries to find glitch-free design[11].
5. *Linear programming:* In this method the gate delays are treated as variables and optimum delays are found by solving a linear program (LP)[12,13] which is implemented using AMPL programming method[14].
6. *Variable input delay method:* Raja in[7] proposed variable input delay method which involves insertion of "permanently on" series transistor at the input of logic gate for glitch free digital circuits.

Among these mentioned techniques variable input delay method is most promising for glitch reduction on a post routed layout on selected combinational cells. This method can easily be stitched in to existing physical implementation flows. However the work in[7] was done using NMOS pass transistor which causes the transistor in the next stage to have a higher source-drain leakage current. This disadvantage can be eliminated by using a CMOS pass transistor as shown in Fig 2. In this work we have used pass transistor as glitch compensation circuit.

3.2. Dynamic IR Drop Reduction

Dynamic/Transient IR voltage drops are due to peak currents caused by large number of logic gates switching close to the short period of time in synchronous circuits. The

most commonly used methodology to resolve peak transient IR drop is to add the decoupling capacitance (Decap) cells in to layout. These Decap cells acts as local charge reservoirs and reduce the effect of peak IR drop on neighbouring circuits[15]. However Decap cells contribute significant gate tunnelling leakage current to the design and starting from 90nm technologies and below this contribution is even more due to gate oxide scaling[16].

3.3. Motivation

Optimizing power consumption has become a major challenge in modern chip design mainly because of constraints dictated by limit on standby leakage power requirements. So there is a need for alternate approach to Decap cell insertion methodology used to reduce transient/dynamic IR drop in order to limit the leakage power in the layout. Dynamic power consumption in circuits can be described as product of number of transitions (N_t) and average power per transition (P_t)[7]. In this work our primary motivation is to reduce Nt through glitch elimination in selected combinational cells which are contributing to peak IR drop. The peak IR drop transient time and combinational cells which are contributing to it can be determined from dynamic IR drop analysis. By using above mentioned variable input delay method with transmission gate as compensation circuit on selected combinational cells we can reduce peak current contribution due to glitches and thereby IR drop. In data intensive architectures P_t and N_t are not completely independent and hence reducing N_t on selected combinational cells can definitely reduce P_t.

4. Proposed Methodology

Dynamic voltage (IR) drop, unlike the static voltage drop depends on the switching activity of the design, and hence it is vector dependent. Dynamic IR drop Evaluates the IR drop caused when large amounts of circuitry switch simultaneously. One of the key requisites is to generate a realistic VCD (Value Change Dump) a file format that captures the switching information which accounts for the real cell and interconnect delays typically done by annotating an SDF (Standard Delay Format) in the gate level simulation. Such a simulation captures the realistic spread of switching activity in the design for duration of time window *(T)*. During dynamic IR drop analysis *T* will be break down in to several small time steps. The length of time step will be determined by the switching activity window or average transition time which can be obtained by the static timing analysis. After rail analysis the peak voltage drop V_{peak} at peak time "*t*" within *T* is due to peak current flow in power grid resistance "*R*" can be given as:

$$\Delta V = V - I(v,t)_{peak} \; R \quad (1)$$

$$\left(\text{where } I(v,t)_{peak} = \frac{P(v,t)_{peak}}{V(v,t)_{peak}} \right)$$

$$\Delta V = V - \left(\frac{P(v,t)_{peak}}{V(v,t)_{peak}} \right) R \quad (2)$$

$$\Delta V \propto P(v,t)_{peak} \quad (3)$$

Where Switching, short circuit and glitch components of $P(v,t)_{peak}$ can be expressed as:

$$P(v,t)_{peak} = P(v,t)_{Switching} + P(v,t)_{SC} + P(v,t)_{Glitch} \quad (4)$$

Considering "*m*" logic gates contributing to peak power:

$$P(v,t)_{Switching} = \sum_{i=1}^{m} Ci \times V^2(v,t) \times f \times D \quad (5)$$

$$P(v,t)_{SC} = \sum_{i=1}^{m} \left(\frac{1}{12} \right) \times \beta_i(v,t) \times (V_{dd} - 2V_T) \times \tau \times f \quad (6)$$

Where β_i is the gain factor of the gate, τ is raise or fall time of the input signal, V_T is threshold voltage, D is the activity factor, C_i load capacitance of the gate and f represents frequency. Glitch detection and glitch power calculation can be done by using power analysis results[17], where transmitted glitch can be defined as the pulse whose pulse width *(PW)* meets the following criteria:

$$PW < \left(\frac{t_{rise} + t_{fall}}{2} \right) \quad (7)$$

If the PW of the glitch doesn't meet the criteria in above equation, then the signal does not reach the full voltage levels. The pulse width is determined from the VCD file and compared with the sum of the rise and fall transition times obtained from static timing analysis. Suppose that a gate *G* with inertial delay is $dj(G)$ has "*n*" fanins $in_1, in_2, \ldots, in_n$ and the arrival times of each fanin nodes are $t_a(in_1), t_a(in_2), \ldots, t_a(in_n)$ respectively. When $Max(t_a(in_1), t_a(in_2), \ldots, t_a(in_m)) - Min(t_a(in_1), t_a(in_2), \ldots, t_a(in_m)) > dj(G)$, glitches on the fanout node of *G* can be generated depending on input signals. Let's further suppose that the PW of glitches at fanin nodes are $pw(in_1), pw(in_2), \ldots, pw(in_{n-1})$ respectively. These glitches on fanin nodes can only be propagated through gate *G* if $Max(pw(in_1), pw(in_2), \ldots, pw(in_n)) > d_j(G)$. Hence a constant called glitch ratio ($0 < GR < 1$) is used to model the glitch power. The dynamic power (P_{NG}) of the gate when there is no glitch is scaled with glitch ratio *(GR)* to estimate glitch power.

$$P(v,t)_{glitch} = GR \times P_{NG} \quad (8)$$

Where $GR = \left[\left[\left(\frac{PW \times 2}{t_{rise} + t_{fall}} \right) \right] \right]^2$

Hence we can conclude that:

$$P(v,t)_{glitch} \propto GR \quad (9)$$

$$GR \propto PW \quad (10)$$

$$PW \propto d_j(G) \quad (11)$$

Now considering "q" number of gates $(q < m \text{ and } q_j \subset m_i)$ which are contributing to peak power. The glitch power can be expressed as:

$$P(v,t)_{glitch} = \sum_{j=1}^{q} GR_j \times P_{NGj} \quad (12)$$

Reducing $P(v,t)_{glitch}$ is the subject of this work. For this we are using variable input delay method[7] which involves insertion of permanently on transmission gate at the input of logic gates to reduce differing delay at logic gate inputs. This intern will reduces glitch width and hence dynamic power. Consider the two input NAND gate shown in Fig 2. Suppose, the delay of path 1 to 3 is $d_{1\rightarrow3}$ and that of 2 to 3 is $d_{2\rightarrow3}$. The intrinsic inertial delay d_3 of node 3 is independent of the input causing the output to change. It depends upon the total capacitance of node 3 and the resistance of ON transistors within the gate. Now the differential delay caused due to earliest arrival time of path 1 to 3 can be compensated by inserting transmission gate which consists of parallel connection of NMOS and PMOS. The transmission gate will pass logic 0 and 1 respectively without effecting voltage level of the signal. The effective resistance R_{eff} of CMOS transmission gate is given by combined both transistors connected in parallel:

$$d_{1\rightarrow3} = R_{on} \times C_{in1} + d_3 \quad (13)$$

$$d_{2\rightarrow3} = R_{on} \times C_{in2} + d_3 \quad (14)$$

Where C_{in1} and C_{in2} are the input capacitances seen at the inputs of the gate and R_{on} is the series resistance of the ON transistors in the previous stage. The delay of the transmission gate due to R_{eff} along with R_{on} for charging C_{in1} is given by $(R_{on} + R_{eff}) \times C_{in1}$. The effective resistance R_{eff} can be increased by altering the *(W/L)* ratio of the transistors. We prepared a lookup table (LUT) using Synopsys SAED 90nm PDK for various R_{eff} values by changing *(W/L)* ratio's as shown in Table-1. C_{in1} values and arrival times can be obtained by static timing analysis results and R_{eff} can be computed. The proposed physical implementation flow is shown in Fig 3. From equation 1, 3, 9, 10, 11 & 14 we can conclude that the dynamic IR drop can effectively minimized by selective glitch reduction method using proposed flow.

5. Experimental Results

The proposed approach needs pre characterization of resistance cell created using pass gate. Resistance cell creation is done using Synopsys SAED 90nm PDKs[18]. HSPICE® is used to measure the effective resistance values of this pass gate structure and Look-up Tables (LUT) prepared as shown in in Table-1. Composite Current Source (CCS) Models for timing and power models are generated using Liberty-NCX® and standard cells layout for different dimensions of pass gate structure are created using Custom Designer®.

Table 1. LUTs for R_{eff} Prepared using Synopsys SAED 90nm PDK

W/L Ratio for T-gate Structure in µm		Equivalent Series Resistance Value in Ω
NMOS	PMOS	
0.12/0.1	0.36/0.1	3.0K
0.2/0.1	0.6/0.1	1.79K
0.4/0.1	1.2/0.1	894
0.6/0.1	1.8/0.1	597
1.0/0.1	3.0/0.1	361
2.0/0.1	6.0/0.1	184
4.0/0.1	12.0/0.1	95.6
6.0/0.1	18.0/0.1	66.2
10.0/0.1	30.0/0.1	42.7
12.0/0.1	36.0/0.1	36.8

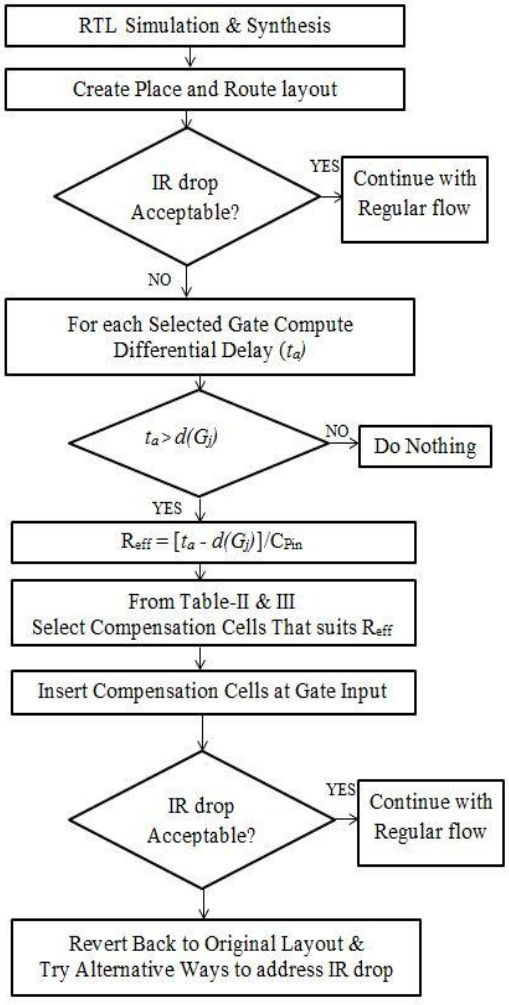

Figure 3. Flow diagram for Proposed Methodology

Table 2. MAC Layout Quality Metrics ComparedWith Proposed and Dcap Insertion Method

MAC Layout Quality of Results (QOR)	Original Place and Routed MAC layout (1301 Cells)	After Inserting Proposed Glitch Compensation Circuit to Reduce Dynamic IR Drop (57 Cells)	After Inserting Decoupling Capacitance (Decap) Cells to Reduce Dynamic IR Drop		
			Trail-1 (1953 Cells)	Trail-2 (68 Cells)	Trail-3 (31 Cells)
Glitch Power (W)	4.85E-05	4.25E-05	5.19E-05	5.23E-05	5.23E-05
Peak Power (W)	0.0394	0.0385	0.0398	0.0394	0.0394
Switching Power (mW)	0.6632	0.659446	0.686207	0.686195	0.686202
Short Ckt Power (mW)	2.44752	2.37256	2.44648	2.44682	2.44682
Internal Power (mW)	0.802345	0.744282	0.803834	0.803645	0.803646
Leakage Power (mW)	0.183135	0.181372	0.217156	0.18432	0.183675
Total Power (mW)	4.0962	3.95766	4.15367	4.12098	4.12035
Total Core Cap (nF)	6.55E-02	6.88E-02	3.87E+03	134.707	61.447
Worst Slack (ns)	2.2926	1.5515	2.292	2.2917	2.2916

Table 3. MAC Layout Peak IR Drop Reduction Numbers with Proposed and Decap Insertion Method

10 Peak Transient IR Drop Numbers in mV					Reduction in Peak IR Drop Numbers			
Original MAC Layout	With Proposed Method	Trail-1 Decap insertion	Trail-2 Decap insertion	Trail-3 Decap insertion	With Proposed Method	Trail-1 Decap insertion	Trail-2 Decap insertion	Trail-3 Decap insertion
7.047	6.223	6.013	6.771	6.754	12%	15%	4%	4%
7.002	5.933	6.013	6.771	6.754	15%	14%	3%	4%
6.725	5.007	4.558	6.771	6.754	26%	32%	-1%	0%
6.453	4.197	3.513	6.441	6.522	35%	46%	0%	-1%
6.423	3.505	3.206	6.441	6.522	45%	50%	0%	-2%
6.308	3.329	3.206	6.441	6.522	47%	49%	-2%	-3%
6.253	3.209	3.193	6.322	6.403	49%	49%	-1%	-2%
6.253	3.204	2.701	5.985	6.055	49%	57%	4%	3%
6.226	3.152	2.585	5.985	6.022	49%	58%	4%	3%
6.038	3.013	2.581	5.97	6.022	50%	57%	1%	0%

Multiply-Accumulate (MAC) architecture with 16X16 multiplier and 32 bit accumulator word length is taken to corroborate the proposed methodology. MAC layout was implemented using SAED 90nm libraries. Design Compiler® is the tool used for carrying out synthesis. IC Compiler® is used for Floorplan, placement and routing. VCS-MX® is used for gate level simulation with 120 test vectors to generate Value Change Dump (VCD) switching activity file. Prime Rail® is used for doing dynamic IR drop analysis and Decap insertion. Decap insertion was done on place and routed MAC layout in three different trails to have the balance between total designs coupling capacitance versus design leakage. After implementing the proposed flow in original place and routed MAC layout the Quality of Results (QOR) are tabulated in Table-2. The reduction in transient peak IR drop numbers on MAC layout using proposed method and Decap insertion methods are compared and tabulated in Table-3. The results shows 12% to 50% reduction in top 10 peak IR drop numbers with just 12% glitch power reduction in selected combinational cells using proposed technique. The Decap insertion with optimal design leakage in Trail-2 and Trail-3 could only achieve 4% reduction in peak IR drop. The proposed flow will ensure that no new timing violations will be created via glitch compensation cells insertion. The key observation form Table-3 is that there is no increase in design leakage with proposed method whereas with Decap insertion method in Trail-1 the leakage power is increased by 20%. With the proposed method 3% decrease in total designs power is observed due to 12% glitch reduction. Fig 4 shows dynamic IR drop maps from IC Compiler® tool.

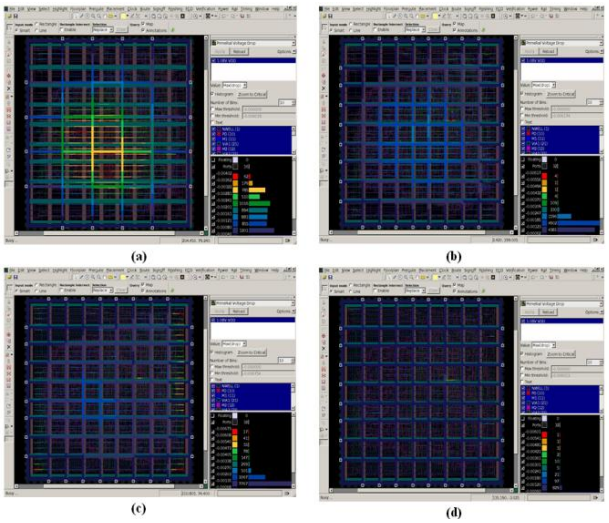

Figure 4. Dynamic IR Drop Maps of MAC layout: (a) Original Place and Routed Layout (b) With Proposed Glitch Reduction Method (c) With Trail-2 Decap Insertion (d) With Tail-1 Decap Insertion

6. Conclusions

By adopting the proposed selective glitch reduction technique the peak dynamic IR drop can be kept within allowable limits. The experimental results show that proposed technique it is more effective when compared to traditional Decap cell insertion technique with minimum compensation cells. The proposed flow can be seamlessly integrated into existing physical design flows.

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