Self-powered and Self-configurable Active Rectifier Using Low Voltage Controller for Wide Output Range Energy Harvesters

Zheng Jun Chew, *Member*, *IEEE*, Yang Kuang, and Meiling Zhu

***Abstract*—This paper presents a self-configurable and self-powered active rectifier that operates from 0.25–20 V for energy harvesting applications. The proposed circuit self-startups from a low voltage using a charge pump and amplifies the voltage with a voltage doubler (VD) topology to provide succeeding circuits such as boost converters with a higher voltage. When the voltage of the energy harvester reaches a high threshold, the circuit switches its topology to a full-wave rectifier (FR) that does not amplify the voltage. The start-up circuit can limit its voltage intake to prevent boosting the high voltage, which may damage the whole circuit. Comparators with a maximum operating voltage of 5.5 V used in the implementation of the rectifier are protected by a diode and resistor based circuit. A piezoelectric energy harvester (PEH) that has a wide open-circuit voltage of 0.4–15 V under the acceleration of 0.04–0.3 g was used to test the circuit. The experiment results showed the rectifier can startup from 0.25 V and switch its topology according to the PEH voltage. The voltage and power conversion efficiencies are over 90% in most cases.**

***Index Terms*—energy harvesting, full-wave rectifier, self-configurable, self-powered, voltage doubler, wide range.**

I. Introduction

ENERGY harvesting has been long sought as an alternative to batteries for powering wireless sensor nodes, especially for industrial monitoring applications because the need to replace the large numbers of batteries is costly [1]. Common energy harvesters are solar cells [2], thermoelectric generators [3], piezoelectric [4], and electromagnetic transducers [5]. The voltage amplitude output by the energy harvesters could be low, high, or span across a wide range due to factors such as ambient conditions [4], structural designs [6], dimensions [7], and transduction mechanisms [8]. For example, under normal operating conditions, an electromagnetic transducer outputs 1–60 V of open-circuit voltage V_{OC} when it is harvesting energy from a current-carrying rail track [9]. A piezoelectric energy harvester (PEH) that output an V_{OC} range of 0.5–11.6 V when excited at 0.05–0.25 g was also reported [10]. The output power of the aforementioned devices spans from hundreds of microwatts to over hundreds of milliwatts, which is enough to power wireless sensor nodes [11]. Thus, neither the low nor the high voltage range can be ignored. Since the first interface for transducers that usually have an ac output is generally a rectifier to convert the ac energy to dc, rectifiers require attention to manage wide output ranges efficiently.

Various types of rectifiers have been reported but very few can rectify wide output ranges efficiently. Standard rectifying circuits such as full-wave bridge rectifier (FBR) and voltage doubler (VD) are still widely implemented especially by using passive diodes. This is because passive diode-based rectifiers are simple and robust [12]. However, diodes have a forward voltage drop V_F of around 0.2–0.6 V. If an energy harvester has a low voltage or high current, the losses in the rectifier are high with only a fraction of the power delivered to the end device even when an optimally designed transducer generates a significant amount of usable power. FBRs and VDs suffer from $2V_F$ and V_F per rectifying cycle, respectively [13]. VDs have a lower loss than FBRs but they are not suitable for all the scenarios as VDs amplify the rectified voltage. When the energy harvester voltage becomes high, further increment of the high voltage by VDs could damage the circuits after the VDs, unless the circuits have high voltage ratings. This might not be feasible for some technologies due to the inherent voltage limitations and high costs [13], [14].

Instead of diodes, active rectifiers use MOSFETs to have improved performance in rectifying both high and low ac voltage because MOSFETs do not have V_F when they are turned on [15], [16]. Commonly used simple and low power design comprises two PMOS and two NMOS, which still have a voltage drop that needs to be overcome due to their inherent on/off threshold voltage [17]. The voltage drop of the NMOS can be reduced by driving their gate using comparators that take the voltage of an energy harvester directly as their input to produce the switching signals [17], [18]. The operating voltage of such design is limited by the supply and breakdown voltages of the comparator because the voltage to the input of the comparator cannot exceed these voltages, which is 5 V in many standard low power fabrication technologies [15], [18]. High voltage comparators are available but their power consumption rises with the supply voltage [19], which is undesirable in energy harvesting due to limited power.

As the only power source, the energy harvester also needs

This work was supported by EPSRC, through the project Zero Power, Large Area Rail Track Monitoring (EP/S024840/1) and Royal Society Industry Fellowship, through the project High Performance Energy Harvesting Sensor Systems for Critical Asset Monitoring (INF\R2\202021). All data are provided in full in the results section of this paper.

Z. J. Chew, Y. Kuang, and M. Zhu are with the College of Engineering, Mathematics and Physical Sciences, University of Exeter, Exeter EX4 4QF U.K. (e-mail: z.j.chew@exeter.ac.uk; y.kuang@exeter.ac.uk; m.zhu@exeter.ac.uk).

to output sufficiently high power and voltage to start-up the circuits for proper operation. The start-up voltage of active rectifiers could be over 1.2 V, which is similar to or even higher than V_F of passive rectifiers as they rely on the energy harvesters to directly produce the voltage required for their start-up [15], [18], [20]. To start-up from low voltage, voltage multipliers have been used to amplify the voltage for starting-up [8], [21]. Given that ambient conditions in the real world are highly dynamic, there will be occasions that energy harvesters output very high voltage. When the start-up circuit amplifies the already high voltage, the voltage from the start-up circuit could be so high that it damages the entire circuit.

Rectifiers that can reconfigure as FR or VD to operate over an extended voltage range than conventional fixed topology rectifiers have been proposed. They were implemented using either a passive rectifier [20] or an active rectifier [22]. However, they do not address the aforementioned issues, especially in operating above 5 V using low voltage and power driver for the active rectifier and starting-up from sub-1 V. This paper presents a self-powered and self-configurable active rectifier to address the narrow operating range issue of conventional active rectifiers for any energy harvesting applications. It uses different topologies of either FR or VD based on the voltage of the energy harvester to rectify the wide voltage range. Diode-resistor and transistor based solutions are applied on low voltage nanopower comparators and the start-up circuit, respectively. This allows the comparators to operate with the high voltage from the energy harvester as their input signal and the start-up circuit to limit high voltage intake, which avoids amplification of the high voltage that will damage the circuit. A PEH that has a wide output range was used to test the circuit as a use example.

II. System Description

Fig. 1 shows the diagram of the proposed rectifying circuit. It consists of a passive diode-based FBR in parallel with an active rectifier that can switch its topology, a control circuit that configures the rectifier topology, two driver circuits to switch the NMOS, and a start-up circuit. The whole system operation and switching mechanism will be explained here.

A. Whole System Operation

The two terminals of the PEH, each with the voltages V_{PZ1} and V_{PZ2}, respectively are connected to the circuit. The passive FBR and active rectifier are connected in parallel to output a rectified voltage V_{rect}. The PEH voltage is rectified by the FBR formed by four Schottky diodes, $D_{R1–4}$ when the circuit is starting up for the first time without energy stored in its energy storage capacitors. The output of the FBR $V_{rect,p}$ is fed into the start-up circuit, which is a charge pump driven directly by the PEH. Once the output from the start-up circuit V_{SU} reaches the minimum operating voltage to run the driver circuits, the active rectifier will be operating as a VD by default to give a higher rectified voltage to succeeding circuits at the output of the rectifier for an easier start-up in case of a low PEH voltage. The switching from one topology to another is based on the voltage requirement and limit of the succeeding circuits. The mode control circuit monitors V_{rect} to decide on the topology to be used. The rectifier switches to the full-wave rectifier (FR) when V_{rect} is sufficiently high as further voltage amplification in VD mode will be too high for the succeeding circuits and switches back to VD when V_{rect} becomes too low.

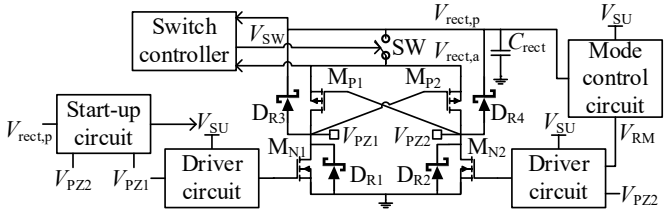

Fig. 1. System architecture of the proposed rectifying circuit.

B. Rectifier Operations and Topology Switching

The rectifier configures itself as either FR or VD using the same set of components. Fig. 2 shows the components in use and some key voltage waveforms of the rectifier in FR and VD modes once V_{SU} is sufficiently high for the whole system operation. The active rectifier is formed by two gate cross-coupled PMOS $M_{P1,2}$ that are driven by V_{PZ} with an arbitrary amplitude V and two NMOS $M_{N1,2}$ that are driven by driver circuits with the outputs V_{GN1} and V_{GN2} applied to the gates of M_{N1} and M_{N2}, respectively. A normally-off switch SW links the outputs of the passive and active rectifiers at specific times for a proper operation of the circuit. When the output of the active rectifier $V_{rect,a}$ is higher than the passive rectifier $V_{rect,p}$, SW is turned on by the signal V_{SW}. As SW closes, the outputs of both passive and active rectifiers are connected as a common output of V_{rect}. The active rectifier is the dominating element in rectifying ac voltage as the MOSFETs provide a current path with a lower voltage drop than V_F of the diodes that form the FBR. The switch is open to prevent energy backflow from the smoothing capacitor C_{rect} when $V_{rect,a}$ is lower than $V_{rect,p}$. As a FR, M_{P1} and M_{N2} are used to rectify the half cycle of the PEH output voltage when $V_{PZ1} > 0$ while M_{P2} and M_{N1} are used for the other half cycle when $V_{PZ2} > 0$.

To operate as a VD, NMOS M_{N2} is constantly turned on to bypass diode D_{R2}. Thus, the anode of D_{R4} and the terminal of the PEH at V_{PZ2} are pulled to ground. As a sufficiently large C_{rect} tends to hold charges at the output of the rectifier, there is usually a positive voltage at the cathode of D_{R3} and D_{R4}. Thus,

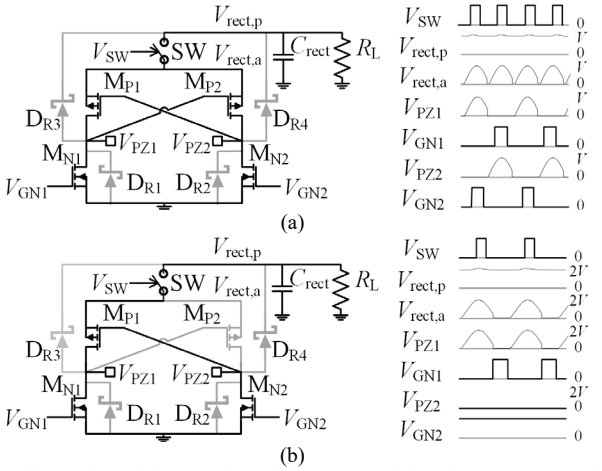

Fig. 2. Illustration of the operation of the proposed circuit as a (a) FR and (b) VD. Greyed out components are not a conduction path.

D_{R4} can be regarded as open circuited since it is reverse biased by the voltage at its cathode and ground connection at its anode. M_{P1} is always turned on as its gate is connected to V_{PZ2}, which is always LOW. This in turn connects the source and gate of M_{P2} together, which makes M_{P2} always off. As V_{PZ1} goes to zero, V_{GN1} from the driver circuit turns HIGH to turn on M_{N1} to charge up the intrinsic capacitor of the PEH. As the piezoelectric voltage increases again, the energy from the PEH is transferred to the output of the rectifier via M_{P1} and SW, which will be toggled as explained earlier. D_{R1} and D_{R3} are still valid current paths as VD but as in the case of the FR, M_{P1} and M_{N1} are the dominating elements, which without V_F provide a lower loss current path than the diodes.

III. System Design and Analysis

Low power is one of the main considerations as most of the harvested energy should be for the end device instead of being used by the interface circuit [12]. Thus, various methods to enable the low voltage components to operate over a wide voltage range are used in the rectifier, driver circuit, start-up circuit, and control circuit that all have different operating conditions as part of these individual subsystems.

A. Rectifier

Apart from $D_{R1–4}$, $M_{P1,2}$, and $M_{N1,2}$, resistors $R_{G1,2}$ and gate protection diodes $D_{GS1,2}$ are also part of the rectifier as shown in Fig. 3 to protect $M_{P1,2}$. A MOSFET may have a high drain-source voltage V_{DS} rating but its gate-source voltage V_{GS} rating is usually much lower. The possible high voltage from a PEH may cause $V_{rect,a}$ at the source of $M_{P1,2}$ to be high and the high voltage is held by C_{rect}. In the conventional cross-coupled connection, the gate of the PMOS at one side is connected directly to the terminal of the PEH at the other side as shown in Figs. 1 and 2. Thus, the voltage applied to the gate is V_{PZ}, which can be slightly lower than zero at its trough. With $V_{rect,a}$ remains high due to C_{rect}, V_{GS} can be very high that it exceeds the breakdown V_{GS} of M_P and permanently damages M_P. With a D_{GS} in between the source and gate of M_P and R_G between the gate and the ground as shown in Fig. 3, the gate voltage V_G of M_P no longer goes to a very low voltage that creates a high V_{GS}. D_{GS} suppresses V_{GS} to be within its clamping voltage if V_{GS} exceeds that voltage. The gate voltage of M_P drops across R_G. Thus, an appropriate value of R_G is required to reduce power dissipation without affecting the switching of M_P as R_G forms an *RC* circuit with the parasitic capacitance of M_P. The *RC* time constant needs to be much shorter than the period of the vibration applied to the PEH for a proper operation [23].

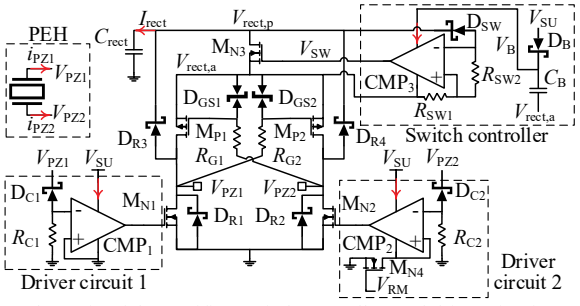

Fig. 3. Schematic of the rectifier, switch controller, and driver circuit.

B. Switch Controller

The switch SW is realized by an NMOS M_{N3}, which has its drain and source connected to the output of the passive and active rectifiers, respectively. Since the voltage at the source of M_{N3} is $V_{rect,a}$, M_{N3} is turned off when the voltage applied to its gate equals $V_{rect,a}$. To turn on M_{N3}, the voltage applied to its gate has to be at least $V_{rect,a}$ plus the threshold voltage V_{TH} of M_{N3}. A switch controller that comprises a comparator CMP_3, a diode D_{SW}, and two resistors R_{SW} is used to toggle M_{N3}. CMP_3 is driven by using a bootstrap capacitor power supply that is referenced to $V_{rect,a}$. The start-up circuit charges up the bootstrap capacitor C_B to voltage V_{SU} via diode D_B when $V_{rect,a}$ reaches its trough. As $V_{rect,a}$ increases, the voltage V_B across C_B increases accordingly to a level that is equal to V_{SU} plus $V_{rect,a}$ minus V_F of D_B to power up CMP_3. With the ground pin of CMP_3 at $V_{rect,a}$, this gives CMP_1 an output voltage of higher than $V_{rect,a}$ by V_{SU} minus V_F to fully turn on M_{N1} and a LOW output voltage of $V_{rect,a}$, which is low enough to turn off M_{N3}.

The positive input of CMP_3 is biased at the voltage $V_{rect,a}$ via R_{SW1}. The negative input is linked to $V_{rect,a}$ via R_{SW2} and $V_{rect,p}$ via D_{SW}. D_{SW} is reverse biased when $V_{rect,a}$ is lower than $V_{rect,p}$. Thus, the voltage at the negative and positive inputs are equal at $V_{rect,a}$ for CMP_3 to output a voltage V_{SW} that is LOW to keep M_{N1} off. When $V_{rect,a}$ becomes higher than $V_{rect,p}$, D_{SW} is forward biased and conducts current. This causes the voltage at the negative input to become slightly lower than the positive input due to the voltage drop across R_{SW2}. Thus, the switching voltage V_{SW} becomes HIGH to turn on M_{N3}. As the inputs and ground of CMP_3 and C_B are referenced to $V_{rect,a}$, a low voltage comparator can be used to implement CMP_3.

C. Driver Circuit

As mentioned earlier, conventional active rectifiers that connect the negative input of the comparator directly to the PEH have a limited operating voltage range unless a high voltage comparator is used [18]. The comparator turns on the NMOS whenever the voltage of the PEH at its negative input goes to zero or below as shown in Fig. 2. Since the comparator turns on the NMOS when the PEH voltage is LOW, the high voltage of the PEH is not needed and can be decoupled from the comparator. The proposed driver circuit uses a resistor R_C and a diode D_C with its anode connected to the negative input of $CMP_{1,2}$ to isolate the high voltage. The other end of R_C is connected to the ground and the cathode of D_C is connected to the terminal of the PEH. D_C is reverse biased when V_{PZ} is higher than its V_F since its anode is connected to the ground via R_C. Thus, D_C can be regarded as open-circuited, which prevents very high V_{PZ} to be directly applied to the negative input of CMP and damaging it. Before $M_{N1,2}$ are switched on, $D_{R1,2}$ are the current path due to their lower V_F than the inherent body diode of MOSFETs. Thus, the trough of V_{PZ} will go below zero to $-V_F$. This causes D_C to be forward biased, which applies a negative voltage at the input of CMP. With the positive input of $CMP_{1,2}$ at zero, which is higher than the negative voltage, $CMP_{1,2}$ output a HIGH signal $V_{GN1,2}$ to turn on $M_{N1,2}$. Thus, this circuit design allows an active rectifier to be implemented using low voltage comparators

regardless of the high PEH voltage with negligible power dissipation at D_C and R_C as their voltage drop is very low.

The positive input and ground terminal of CMP_2 are joined together and floated when the circuit is first started up. They are disconnected from the system ground by M_{N4}, which is in an OFF state initially. The floating voltage at the positive input of CMP_2 is always higher than the negative input that is pulled to the ground by R_{C2}. Thus, CMP_2 has an always-HIGH output that constantly turns on M_{N2} for a VD topology by default. M_{N4} will be turned on by the control circuit when V_{PZ} is sufficiently high to connect the negative input and ground pin of CMP_2 to the system ground. CMP_2 will then operate as described in the earlier paragraph, where it turns on M_{N4} for the rectifier to operate as a FR when V_{PZ2} reaches its trough.

D. Start-up Circuit

The start-up circuit consists of Schottky diodes D_V, flying capacitors C_V, four MOSFETs $M_{D1–4}$, and filter capacitors C_{Vi} and C_{Vo}, as shown in Fig. 4. $M_{D1–4}$ are used as the voltage regulator here by applying a regulating voltage at their gate. $M_{D1–4}$ are turned on when the applied $V_{GS} \geq V_{TH}$ of M_D. The voltage relationship can be rewritten as (1) and rearranged as (2). The applied gate voltage V_G limits the maximum voltage V_S that can present at the source terminal of M_D. $M_{D1–3}$ limit the voltage intake of V_{PZ} and $V_{rect,p}$, which can be very high. M_{D4} further limits the output from the charge pump to ensure V_{SU} is always within a safe level for the circuits.

$$V_G - V_S \geq V_{TH} \tag{1}$$

$$V_S \leq V_G - V_{TH} \tag{2}$$

The circuit has an even number of stages n with each D_V–C_V pair forming a multiplier stage. The start-up circuit takes $V_{rect,p}$ as its input with the PEH driving its flying capacitors C_V to provide an amplified voltage V_{SU} and current I_{SU} as in (3) for starting-up the driver and control circuits [24]. The source voltages $V_{S\text{-}MD3}$ of M_{D3} and V_{FLY} of $M_{D1,2}$ are equal to $V_{rect,p}$ and V_{PZ}, respectively, if they are lower than the condition on the right of (2). Otherwise, the voltages are limited by the V_G applied and V_{TH} of M_D. Since the flying capacitors are driven directly by V_{PZ}, f_{PZ} is the vibration frequency of the PEH.

$$V_{SU} = V_{S\text{-}MD3} - V_{F\text{-}DV} + n\left(V_{FLY} - V_{F\text{-}DV}\right) - nI_{SU}\left(C_V f_{PZ}\right)^{-1} \tag{3}$$

Depletion-mode MOSFETs are used as $M_{D1–4}$ as they are normally closed devices that allow current flow even when V_G applied to their gate is zero to enable cold start-up of the circuit. However, their channel resistance is usually higher than enhancement-mode MOSFETs such as $M_{P1,2}$ and $M_{N3,4}$. By taking one stage that is formed by C_{V1} and D_{V1} as an example, C_{V1} will be charged up to a voltage that is equal to $V_{rect,p}$ minus V_F of D_{V1} and the voltage drop of M_{D3}, and then boosted by V_{PZ1} minus the voltage drop of M_{D1}. The voltage drop of M_D increases with their resistances, which reduces the peak voltage at each stage and the output voltage of the start-up circuit. Thus, V_{SU} is applied to the gate of $M_{D1–3}$ to reduce their resistance for a higher V_{SU}. Depletion-mode MOSFETs have a negative V_{TH} where V_G has to be lower than V_S to meet the condition as given by (1). Instead of generating a negative V_G using an additional circuit, which consumes more power, C_{Vi} and C_{Vo} are used to hold the voltage at the source of $M_{D3,4}$ so that the minimum V_G can simply be zero to limit the voltage at the source of M_D to a voltage that is equal to the V_{TH} of M_D. A diode in between C_{Vn} and C_{Vo} to prevent backflow of the charges is not required in this design. When the rectifier is in FR mode, the amplitude of V_{PZ} is sufficiently high where the voltage at C_{Vn} has already exceeded V_{SU}, which is regulated by M_{D4}. In VD mode, the even-number stages are not acting as the multiplying stage because V_{PZ2} is at the ground. Thus, D_{Vn} at the last stage directly acts as the blocking diode here.

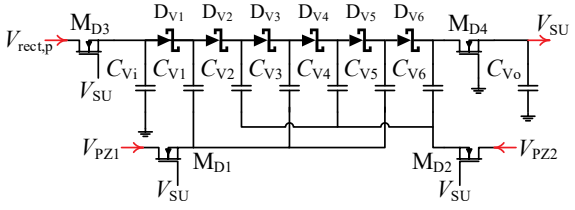

Fig. 4. Schematic of the start-up circuit.

E. Mode Control Circuit

The mode control circuit is shown in Fig. 5, which consists of a comparator CMP_4, a PMOS M_{ref}, and some resistors. Resistive voltage dividers are used to scale down V_{rect} and a reference voltage V_{ref} to an appropriate ratio as V_{RH} at the negative and V_{RD} at the positive inputs of CMP_4, respectively. V_{RH} is lower than V_{RD} in VD mode and vice versa in FR mode for CMP_4 to output V_{RM} that toggle M_{N4} as explained earlier in the driver circuit section and M_{ref} for switching the rectifying topology as V_{rect} reaches a threshold. Switching M_{ref} on and off leads to the rectifier operation as a VD and FR, respectively.

As the rectifier switches from VD to FR, V_{rect} and hence, V_{RD} reduce by half. If V_{RH} is unchanged, it could be higher than V_{RD}, causing CMP_4 to output a LOW signal that switches the circuit to operate as a VD again and amplify V_{rect}. This will trigger the circuit to switch back to FR again and the cycle repeats, alternating between the two rectifying modes in an unstable state. Thus, the value of V_{RH} needs to be adaptive to the rectifying mode. The reference in VD mode $V_{RH\text{-}VD}$ has to be higher than the one in FR mode $V_{RH\text{-}FR}$, which decreases as V_{RD} is halved. This is achieved by a reconfigurable resistive divider network formed by $R_{H1–3}$ and M_{ref}. When M_{ref} is turned on in VD mode, it acts as a closed switch to bypass the resistor R_{H1}. Thus, $V_{RH\text{-}VD}$ is given as (4):

$$V_{RH\text{-}VD} = \frac{R_{H3}}{R_{H2} + R_{H3}} V_{ref} \tag{4}$$

When M_{ref} is turned off, it does not have any effect on the resistive divider network. Thus, $V_{RH\text{-}FR}$ is expressed as (5):

$$V_{RH\text{-}FR} = \frac{R_{H3}}{R_{H1} + R_{H2} + R_{H3}} V_{ref} \tag{5}$$

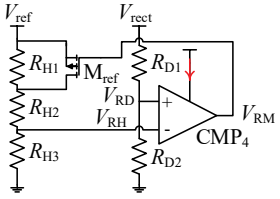

Fig. 5. Schematic of the mode control circuit.

Equation (4) slightly differ from (5) in the denominator where R_{H1} is excluded from (4) as M_{ref} is switched on as explained earlier. Thus, $V_{RH\text{-}VD}$ is higher than $V_{RH\text{-}FR}$ because of its smaller denominator. When M_{ref} is turned off in FR mode, R_{H1} is included in the voltage divider to reduce V_{RH} as V_{RD} is lowered due to the switching from VD to FR to prevent the repetitive mode toggling issue [20].

The diode-resistor or transistor-based method applied to the other circuits in earlier subsections are not used here as they isolate high voltage from the circuits or limit the voltage intake, which does not allow the scaling of the voltage. Although it is possible to use a resistive voltage divider in the other circuits, they are not ideal as the resistive networks continually dissipate power. Also, when the PEH voltage is very low, the scaled-down voltage will be even lower, which might not be recognized by the comparators as a valid signal.

IV. Experimental Verification

Fig. 6 shows the experimental setup with the PEH, which uses a piezoelectric stack as its active element (PICMA® P-887.91, PI ceramic) fixed on an electromagnetic shaker (V20, Data Physics). The acceleration exerted by the shaker was measured by a laser Doppler vibrometer (CLV2534, Polytech). The voltages and currents, which are represented by the arrows as indicated in Figs. 3–5 were measured using sourcemeter units (2612B, Keithley), which have the accuracies of within ±0.03% [25]. The terminals of the PEH were connected to a resistor first to characterize its power bandwidth. The frequency range of the bandwidth was used to test the circuit. The optimal resistance for each tested vibration is different [10]. Thus, the resistance was manually tuned until maximum power output from the PEH is obtained.

A. System Implementation

The circuit was implemented using discrete components on a breadboard. The enhancement-mode MOSFETs were chosen based on their low channel resistances, low gate charge, and low V_{TH}. $M_{N1–4}$ are BSS806N and $M_{P1,2}$ are DMG2301LK. An external D_{GS} is not used as $M_{P1,2}$ has a built-in gate protection diode. These MOSFETs have a breakdown voltage of 20 V, which sets the maximum operating voltage limit of this circuit. The chosen M_D (BSS159) has a $|V_{TH}|$ of 2.4–3.5 V, which is a common voltage range for many circuits if the applied V_G is 0. Comparators with a minimum operating voltage of 1 V and quiescent current I_Q of around 0.3 µA were used as $CMP_{1–3}$ (TS881) and CMP_4 (LTC1540) so that the circuit can operate from low voltage at low power. LTC1540 has a built-in bandgap reference voltage of 1.182 V to be used as V_{ref}.

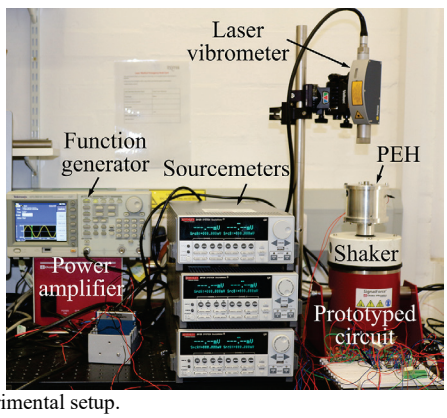

Fig. 6. Experimental setup.

CDBH0230 was used as $D_{R1–4}$, $D_{C1,2}$, D_{SW}, and D_B for their low V_F of 0.24 V. SDM02U30LP3 were chosen as D_V due to their low V_F of around 0.1 V so that the start-up circuit can generate a V_{SU} of at least 1 V with as few stages as possible. This is to ensure D_V and C_V, especially those at the later stages do not experience very high voltage but are still able to start-up the circuit. Assuming that the minimum voltage is 0.25 V, which is higher than V_F of CDBH0230 for the FBR to conduct and based on [3], a six-stage charge pump was used as the start-up circuit. SDM02U30LP3 was not used as the FBR as its leakage current is about 100 times of CDBH0230, which incurs higher losses and degrades the performance of the FBR.

From the datasheet, the input capacitance of $M_{P1,2}$ is around 0.2 nF [26]. To ensure a time constant that is much shorter than the period of the vibration, R_G was chosen to be 330 kΩ. Even with the gate protection circuit implemented, it is still best to avoid operating the circuit at very high voltage for a prolonged time. Considering that $M_{P1,2}$ have a V_{GS} of 12 V, the circuit was set to switch from VD to FR at around 11 V. R_{H1}, R_{H2}, and R_{H3} were set to be 100 MΩ, 20 MΩ, and 30 MΩ, respectively. This gives $V_{RH\text{-}VD}$ and $V_{RH\text{-}FR}$ the values of 11.06 V and 3.69 V, respectively. R_{D1} is 20 MΩ and R_{D2} is 1.37 MΩ, so that the maximum V_{RD} is 1.182 V, which is equal to V_{ref} when V_{rect} is 20 V. R_C and R_{SW} are 10 MΩ. The resistor values are in the tens of megaOhms range to limit the maximum power dissipation to nanowatts range.

B. Testing Methods

The first test was to determine the start-up capability of the prototype from the low voltages of the PEH. A range of low accelerations and frequencies was applied to the PEH via the shaker until the circuit started to operate. Then, the circuit was tested by sweeping across a frequency range around the bandwidth of the PEH, over a range of accelerations and resistive loads. The test includes verification of the topology switching and voltage regulation, power losses, as well as the voltage η_V and power η_P conversion efficiencies of the circuit as given by (6)–(8). The power at the different parts of the circuit was determined using (6). Δt of 0.5 ms is the sampling

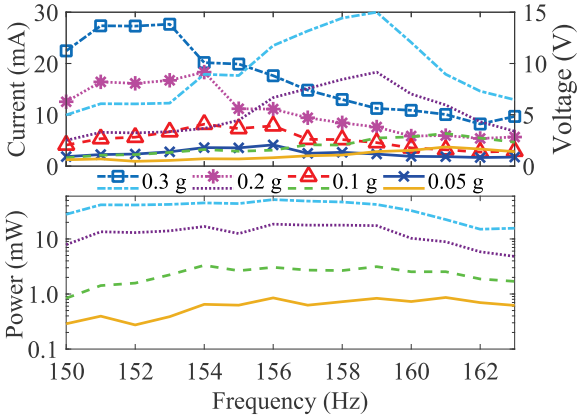

Fig. 7. Open-circuit voltage (top), current (marker), and power (bottom) with an optimal resistive load of the PEH excited by different accelerations.

period and t_N is 70 s to ensure sufficient data sample is taken. The subscript x represents the measurements made at different parts of the system such as 'PZ', 'rect', and so on.

$$P_x = \frac{\sum_{k=1}^{N} v_x(t_k) i_x(t_k) \Delta t}{t_N} \tag{6}$$

$$\eta_V = \frac{V_{rect}}{|V_{PZ}|} \times 100\% \tag{7}$$

$$\eta_P = \frac{P_{rect}}{P_{PZ}} \times 100\% \tag{8}$$

V. Results and Discussions

Fig. 7 shows the open-circuit voltage of the PEH that ranges from 0.4–15 V under the acceleration of 0.05–0.3 g, which is common in industrial environments [27]. When an optimal resistive load is connected to the PEH, the output current amplitude is 2–27.7 mA and power is 287.6 μW–51.74 mW. The vibration frequency of interest in this work is around 150–163 Hz, which is the power bandwidth of the PEH used [10].

A. Start-up

Fig. 8 shows the measured V_{PZ}, V_{SU}, V_{GN2}, and V_{CV6} when the PEH was excited at a vibration frequency of 153 Hz that swept over the accelerations from 0.04–0.2 g. The inset shows the transient state of the circuit. The start-up circuit can operate as soon as there is a voltage from the PEH. The start-up circuit produces V_{SU} of up to 1.1 V from $|V_{PZ}|$ of 0.25 V at the acceleration of 0.04 g to startup the rectifying circuit. The output voltage V_{GN2} from CMP_2 is fluctuating initially but becomes steady at around 0.65 V within 2 s and follows the amplitude of V_{SU} closely afterwards. As V_{GN2} reaches 0.6 V, which is sufficiently high to fully turn on M_{N2}, V_{PZ} in the negative half cycle reduces to almost zero. The gap between $|V_{rect}|$ and $|V_{PZ}|$ is large before V_{SU} reached 0.6 V as V_{PZ} is rectified by the passive FBR. When V_{SU} is higher than 0.6 V for the active rectifier to operate, $|V_{rect}|$ becomes close to $|V_{PZ}|$.

The acceleration was gradually increased to 0.2 g after 14 s where the amplitude of V_{PZ} reached 3.5 V. The voltage V_{CV6} at the last multiplier stage of the charge pump before M_{D4} of the start-up circuit is about 11 V, which is too high for most of the low power comparators. With the voltage regulation using M_{D4} as described in Section III.D, V_{SU} is regulated at 2.5 V.

B. Rectification and Self-configurability

Fig. 9 shows the measured V_{PZ}, V_{rect}, V_{GN1}, V_{GN2}, and V_{RM} as the PEH was excited by a gradually increased acceleration until the PEH voltage is 15 V and back to 0 g at 159 Hz to test the topology switching functionality of the circuit. The circuit begins its operation in VD mode by default, where V_{PZ} can be seen to have zero amplitude in the negative half cycle. V_{GN2} is also HIGH to keep M_{N2} always turned on. V_{rect} increases with the acceleration until it reaches around 11.22 V at 15.8 s. V_{RM} becomes HIGH to turn on M_{N4} and switches the circuit to FR mode where V_{PZ} can be seen to have an equal amplitude in both the positive and negative half-cycles. V_{rect} also reduces following the switch. V_{GN2} now becomes pulses to turn on M_{N2} at the appropriate time when V_{GN1} is LOW as shown in the inset. The results indicate the proposed diode-resistor circuit enables the low voltage comparators with the supply voltage of 2.5 V to operate using high voltage of over 10 V from the PEH as their input signal without being damaged. As the acceleration reduces, V_{PZ} decreases until V_{rect} drops to 3.77 V at 33.6 s. The circuit then switches back to VD mode when V_{RM} goes LOW. V_{rect} can be seen to increase and the negative half cycle of V_{PZ} disappears again. The voltages for topology switching are in good agreement with the calculated one.

Fig. 10 shows the measured currents i_{PZ} from the PEH and i_{rect} output by the rectifier at the acceleration of 0.3 g as an example. The frequencies used are 150 Hz and 159 Hz to get a low and high voltage, respectively. The MOSFETs are switching appropriately in either VD at 150 Hz or FR mode at 159 Hz, where the waveform of the rectified current i_{rect} closely follows the waveform of the input current i_{PZ}. In VD mode, i_{PZ} in the negative half cycle is used to charge up the PEH itself and is not passed through the output of the rectifier as i_{rect}. In FR mode, i_{PZ} in the negative half cycle is rectified as i_{rect} at the output of the rectifier. There is no backflow of i_{rect} from the rectifier output back to the PEH in both operation modes where the amplitude of i_{rect} does not go to negative.

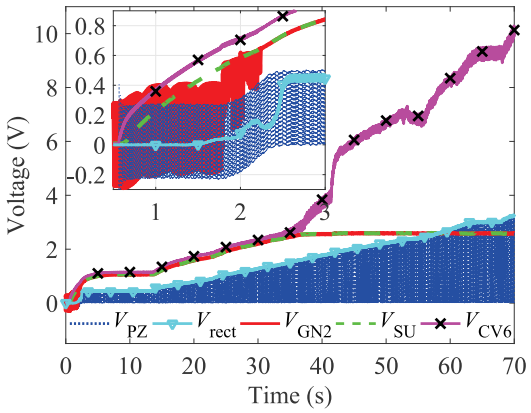

Fig. 8. Measured V_{PZ}, V_{rect}, V_{GN2}, V_{SU}, and V_{CV6} with the PEH excited by the acceleration from 0.04–0.2 g. Inset shows the enlarged view of the area from time 0 to 2.5 s.

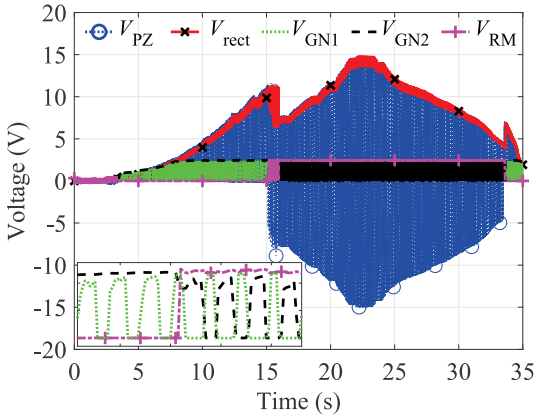

Fig. 9. Measured V_{PZ}, V_{rect}, V_{GN1}, V_{GN2}, and V_{RM} with the PEH excited by sweeping back and forth over a range of acceleration at 159 Hz. Inset shows the enlarged view of the area from time 15.8 to 15.9 s.

C. *Efficiencies and Losses*

Fig. 11 shows the output power versus different resistive loads from the proposed circuit, a conventional active rectifier, and a passive diode-based VD using BAS70, which has low V_F and reverse leakage current [28], with the PEH excited by an acceleration of 0.3 g at 159 Hz as an example. The power curves gradually increase until they reach a peak, which corresponds to the optimal load of the PEH before decreasing. Although the power output by the conventional active rectifier is similar to the proposed circuit, it can only operate up to the load of 100 Ω as further increase of the load will cause V_{PZ} to exceed its voltage limit. The passive diode-based VD has an output power of typically around 5% lower than the proposed circuit in this test due to the inherent V_F of the diodes, which lowers the output voltage as shown in Figs. 12 and 13. The difference can be over 13% especially when the input voltage is low at near to 1 V as shown in Fig. 12. There is also a voltage drop in the negative half cycle due to V_F during the voltage amplification, which increases the losses.

Fig. 14 compares the voltage conversion efficiencies of the proposed circuit with passive diode-based rectifiers from 0.05 – 0.3 g. Apart from the test condition at 0.05 g, the efficiency of the proposed circuit is over 90%, with a peak voltage efficiency of 99.14%. The amplitude of the gate threshold voltage of $M_{P1,2}$ used ranges from 0.3 V–1 V. Thus, when the input voltage to the rectifier is below 1 V, it is possible that $M_{P1,2}$ are not fully turned on and causes the efficiency to be lower than 90% as shown in Fig. 12. However, the prototyped circuit still outperforms the passive rectifier in all the test conditions, especially at low input voltage with an efficiency of about 20% higher. The efficiency of the passive rectifier becomes higher than 90% when the input voltage to the rectifier is over 4 V while the prototyped circuit can achieve such efficiency with an input voltage of about 1.5 V. It should be noted that the rectifier begins its operation as a VD that increases the amplitude of the piezoelectric voltage V_{PZ} by default. This means the actual output voltage from the PEH is about half of the input voltage to the rectifier. With the proposed circuit, the amplitude of V_{PZ} is amplified to allow the circuit to rectify voltage that is initially lower than the gate threshold voltage of the MOSFETs used in the rectifier. This is not possible in other conventional active rectifiers that only operate in a fixed FR mode where their minimum input voltage with a voltage conversion efficiency of 90% is usually beyond the threshold voltage of the MOSFETs [18], [29].

Fig. 15 compares the power conversion efficiencies of the proposed and passive rectifier circuits under the same test conditions as in Fig. 14. Similarly, the prototyped circuit has a higher efficiency than the passive diode-based rectifier in most of the test conditions. The efficiency is generally about 90%, with a peak of 95.43% except for the accelerations of 0.05 g

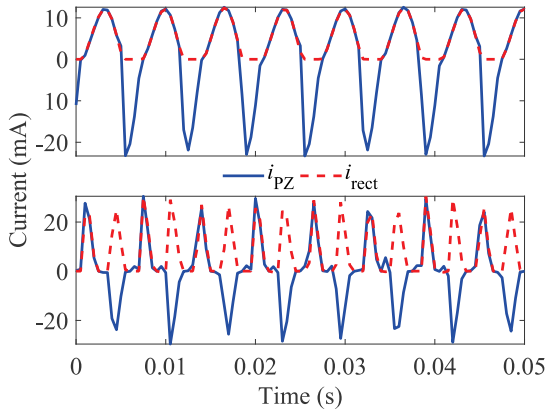

Fig. 10. Measured i_{PZ} and i_{rect} when the rectifier is in VD mode (top) and FR mode (bottom) with the PEH excited by an acceleration of 0.3 g at 150 Hz and 159 Hz, respectively.

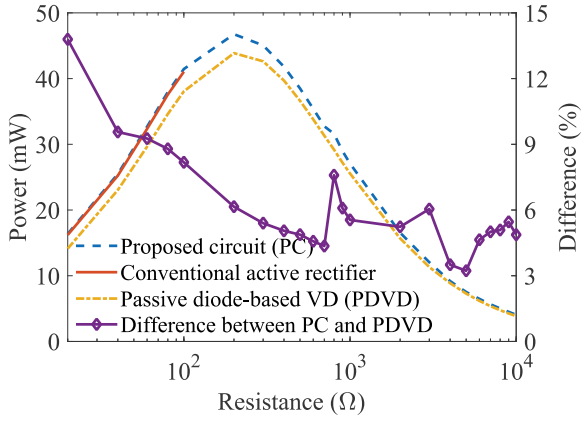

Fig. 11. Comparison of the output power with different resistive loads of 10 Ω to 10 kΩ connected to the output of the PC, a conventional active rectifier and a PVD with the PEH excited by an acceleration of 0.3 g at 159 Hz.

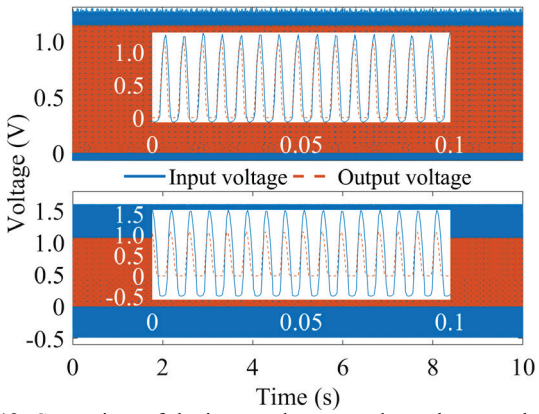

Fig. 12. Comparison of the input and output voltages between the proposed circuit (top) and passive rectifier (bottom) under low voltage condition with a 20 Ω load. The insets show the detailed waveforms.

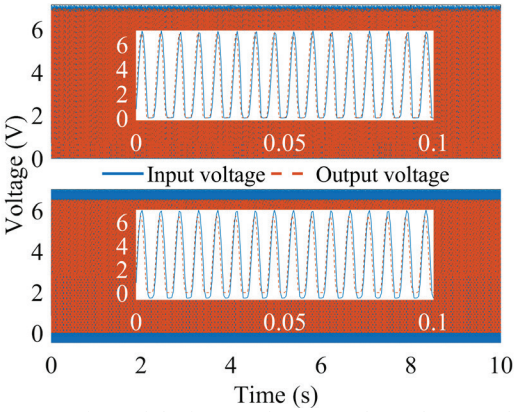

Fig. 13. Comparison of the input and output voltages between the proposed circuit (top) and passive rectifier (bottom) with a 300 Ω load. The insets show the detailed waveforms.

and 0.1 g especially when the voltage is low, which occurs at the vibration frequencies near 150 Hz and 163 Hz. This is because $M_{P1,2}$ cannot be fully turned on when the voltage is low as explained earlier, causing higher power dissipation in the MOSFETs. However, the passive rectifier performs poorer especially in low voltage, high current conditions around 150 Hz. For example, the passive rectifier has an efficiency of 2% while the prototyped circuit achieves an efficiency of 48.42% when the excitation acceleration is 0.05 g at 150 Hz. The efficiency of the passive rectifier is less than 70% most of the time in all the tests with different accelerations.

Fig. 16 shows the range of power consumed by different parts of the circuit. The power consumed by the circuit with CMP_{1-4} was calculated by using (6) plus the Ohmic loss (V^2/R) of any of the resistive branches. The power dissipated by the start-up circuit $P_{loss,\,SU} = P_{rect,p} + P_{PZ1} + P_{PZ2} - P_{SU}$. The power loss in the rectifier was obtained by subtracting P_{rect} and power consumed by the other circuits from P_{PZ}. The primary power loss in the prototyped circuit is caused by conduction loss of the MOSFETs with a turn-on resistance of a few hundreds milliOhms in each of the MOSFETs. The range of the power dissipated by the MOSFETs is from 48.71 µW to 2.68 mW, depending on the current from the PEH that ranges from a few to tens of milliamperes in the tested conditions. The mode control circuit consumes the lowest power at 0.39–1.26 µW as CMP_3 toggles M_{N4} and M_{ref} very infrequently. However, the resistive networks of R_H and R_D dissipate power continuously, which increases with V_{rect}. The switch controller, start-up, and driver circuits have comparable power consumptions as they are involved in switching operations regularly. The start-up circuit has the highest power losses among them but is in a couple of microwatts. This is because it supplies energy to all the other functional circuits. The total current consumed by all the other circuits has to flow through the diodes D_V, which have a voltage drop V_F. This causes 0.83–22.30 µW of power to be dissipated in the circuit. The switch controller consumes the least power at 0.43–10.77 µW as it only turns M_{N3} on very briefly when $V_{rect,a}$ is higher than $V_{rect,p}$.

All the driver circuits consume 0.11–19.18 µW of power. Among them, driver circuit 1 that consists of CMP_1 has a higher minimum power consumption as it is switching M_{N1} regularly. Driver circuit 2 that consists of CMP_2 and is also involved in the mode switching of the rectifier has a lower minimum power consumption range. It has virtually no power dissipation when CMP_2 is floated in the VD mode. Fig. 17 shows the current consumed and the voltage V_{GN2} output by CMP_2. It can be clearly seen that the current is very low when the rectifier is in VD mode with V_{GN2} always HIGH. Once the rectifier switches to FR mode, the current consumption increases drastically due to the regular switching operation involved. This also suggests that the proposed driver circuit for enabling the rectifier to begin its operation in VD mode by default does not draw much energy, which is especially crucial to ensure a successful start-up of the rectifier.

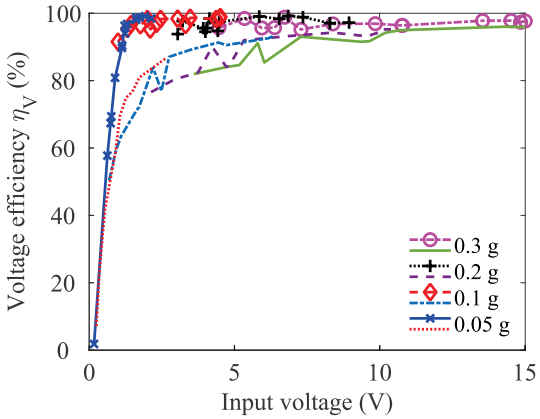

Fig. 14. Voltage conversion efficiency comparison of the proposed circuit (with markers) and passive rectifier under different tests.

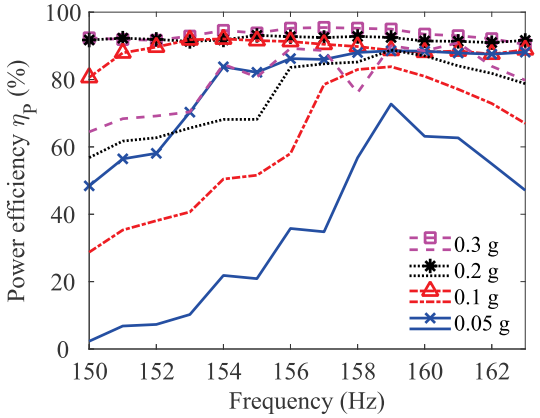

Fig. 15. Power conversion efficiency comparison of the proposed circuit (with markers) and passive rectifier under different tests.

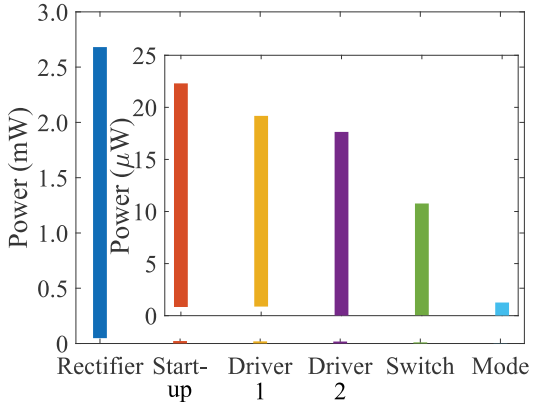

Fig. 16. Power consumption of the different parts of the prototyped circuit. Inset is the enlarged view of the results on the right of 'rectifier'.

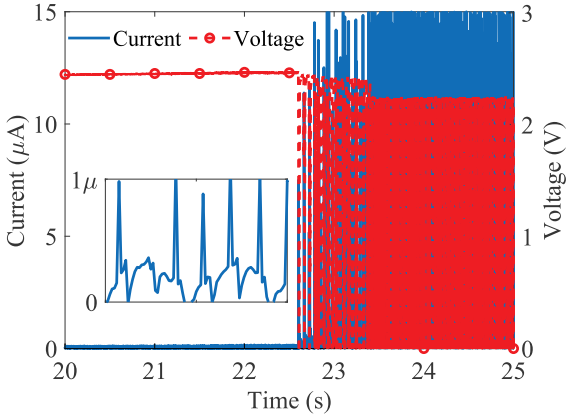

Fig. 17. Measured current consumed and voltage V_{GN2} output by CMP_2 as the rectifier switches from VD mode to FR mode.

D. Comparison With Other Rectifiers

Table I summarizes and compares some common features of the proposed rectifier with other circuits. The other circuits that were implemented as an active rectifier have a limited operating voltage range because of the direct connection of the energy harvester to the comparators, which have a low voltage rating of up to 5 V to drive the NMOS of the rectifier. The prototyped circuit can operate up to 20 V using low voltage comparators that are powered by a voltage supply of 1–2.5 V using the voltage regulation method described in Section III. Although the prototyped circuit was designed to operate up to 20 V, the circuit can be easily implemented to operate at a higher voltage by changing $M_{P1,2}$, $M_{N1,2}$, and $D_{C1,2}$ to have a higher voltage rating while using the same low voltage comparators. The passive diode-based rectifier can operate up to 20 V as no comparators are involved in rectification [20]. The efficiencies are up to 98% because the rectifier was tested using an energy harvester with high voltage and low current output, which has low power dissipation in the diodes. The circuits in [20], [22] are configurable to different rectifying topologies of either FR or VD just like this work. However, the minimum input voltage from the energy harvester that is required for the circuits to start operating is much higher than the proposed circuit because they do not have a start-up circuit. They rely on the energy harvester to generate a voltage that is sufficiently high for their start-up. The circuit in [29] can start-up at a low voltage that is close to the proposed circuit due to the low V_{TH} CMOS fabrication technology used. The peak η_V of the proposed circuit is the highest among all the circuits that are compared at 99.14%. The peak η_P of the proposed circuit is also the highest among the active rectifiers.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Reference	[19]	[29]	[30]	[21]	This work
Technology	0.18 µm CMOS	0.35 µm low V_{TH} CMOS	0.5 µm CMOS	Discrete	Discrete
Structure	Active FR	Active FR	Active FR/VD	Passive FR/VD	Active FR/VD
Self-configurable	No	No	Yes	Yes	Yes
Start-up mechanism	N/A	N/A	N/A	N/A	Charge pump
$V_{in,min}$ (V)	N/A	0.38	1.8	1.2	0.25
$V_{in,max}$ (V)	3	3.3	5	20	20
Peak η_V (%)	99	98	83.8	98	99.14
Peak η_P (%)	90	90	81	98	95.43

VI. CONCLUSION

A self-powered and self-configurable active rectifier for energy harvesters with a wide voltage range is presented. The circuit is able to startup from the low output voltage of an energy harvester and operates using VD topology by default to boost the voltage. Even though the voltage of the energy harvester is low, the voltage that has been amplified is sufficiently high to reach the gate threshold voltage of the MOSFETs used as the rectifier. This allows the rectifier to operate at higher efficiency and wider range than conventional active rectifiers that operate using a fixed topology. The circuit switches its topology to a FR, which does not amplify the voltage as the voltage of the energy harvester becomes sufficiently high. Low power and voltage comparators were used as the driver and control circuits. A novel and simple resistor-diode based solution was introduced to allow the low voltage comparators to operate using the high voltage from the energy harvester as the input signal. This allows the control and driver circuits to be fabricated using standard low voltage technology when implemented as integrated circuits. The circuit was tested using a PEH that has a wide output range and achieved voltage and power conversion efficiencies of over 90% in most of the tested conditions.

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