Self-Powered Integrated Systems-on-Chip (Energy Chip)

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ABSTRACT

In today's world, consumer driven technology wants more portable electronic gadgets to be developed, and the next big thing in line is self-powered handheld devices. Therefore to reduce the power consumption as well as to supply sufficient power to run those devices, several critical technical challenges need to be overcome:

a. Nanofabrication of macro/micro systems which incorporates the direct benefit of light weight (thus portability), low power consumption, faster response, higher sensitivity and batch production (low cost).
b. Integration of advanced nano-materials to meet the performance/cost benefit trend. Nano-materials may offer new functionalities that were previously underutilized in the macro/micro dimension.
c. Energy efficiency to reduce power consumption and to supply enough power to meet that low power demand.

We present a pragmatic perspective on a self-powered integrated System on Chip (SoC). We envision the integrated device will have two objectives: low power consumption/dissipation and on-chip power generation for implementation into handheld or remote technologies for defense, space, harsh environments and medical applications. This paper provides insight on materials choices, intelligent circuit design, and CMOS compatible integration.

Keywords: Self-powered, system-on-chip (SoC), thermoelectric, piezoelectric, solar cell, microbial fuel cell, NEMS.

1. Introduction

The ever increasing consumer demand for more powerful mobile devices has driven the search for longer lasting energy sources. In addition to this, harsh environment applications such as those within the oil & gas industries, deep sea exploration, and remote sensing require long-lasting unmanned devices. With this in mind, we introduce the concept of an energy independent system on a chip (SoC) (Fig. 1). The proposed device consists of two parts; power consumption and power generation. The power consumption section consists of the main control unit, the communications circuit and the sensors. Collectively these components are responsible for controlling the supply of power to the load application. The power generation section consists of a rechargeable Lithium Ion battery (LIB), a microbial fuel cell (uMFC), a thermoelectric generator (TEG), a solar cell and a piezo-electric energy harvester (PNG). DC power is drawn from the battery while the uMFC and the TEG serve as on-chip battery chargers.

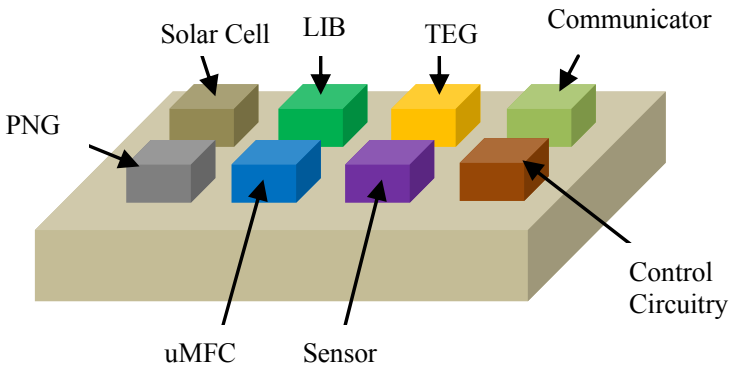

Fig. 1: Self-powered integrated systems-on-chip

Micro- and Nanotechnology Sensors, Systems, and Applications II,
edited by Thomas George, M. Saif Islam, Achyut K. Dutta, Proc. of SPIE Vol. 7679,
767914 · © 2010 SPIE · CCC code: 0277-786X/10/$18 · doi: 10.1117/12.850811

2. Power Consumption

The main objective of the chip is to achieve minimal power consumption. This boils down to the type of device being used in the control circuitry and communicator. As a consequence several device technologies have been studied for their feasibility in incorporating them within the energy SoC:

2.1 SOI and HK/MG technology

Because bulk CMOS technology is a well-established field and has been commercialized, it is a very important candidate for fabricating the energy chip components. Recent advances in process technology such as lithography, use of high-k/metal gate stack have helped in producing smaller, low power devices. As the purpose of the energy chip is to consume minimal power, chip components such as the control circuit and communicator need to have small, low power devices. Recently, Cheng et al. demonstrated a low cost ETSOI (Extreme Thin SOI) CMOS process. Although SOI technology is expensive, Cheng`s group claim that their ETSOI technology offsets this by using a reduced number of masks, implantation steps and process complexity. Featuring an un-doped channel and dual in-situ doped epitaxial S/D and extension regions, the ETSOI CMOS device achieves very low V_T variability and low V_{DD} at a gate length of 25 nm and an I_{off} of 300 pA/μm [1].

2.2 CNT (Carbon Nanotube) Technology

CNT technology is very quickly leaning towards the next generation of electronics in replacing standard MOS technology. CNTFETs in particular have taken the spotlight recently because of their ballistic charge transport property and low power consumption. CNTFETs with specifications that outperform current Si technology have been fabricated in the past, with the popular gate all around (GAA) fabrication process [2]. But this process technology suffers from a minimum dielectric thickness criteria of 8 nm. Our proposed topology would be to use the LBG (local back gate) geometry developed by Franklin et al. reporting a 1.2 nm diameter p-type CNTFET and an Lg of 38 nm exhibiting ballistic charge transport properties and an $I_{on}/I_{off} > 10^5$[3]. The benefits of using CNTFETs are numerous compared to standard Si technology such as low power operation. Besides this, a single CNT can be used to fabricate multiple gate transistors while at the same time allowing aggressive scaling. The proposed p-type CNTFETs consist of Pd-contacts because of the low Schottky Barrier (SB) between metal and the semiconducting CNT interface. For the n-type FETs, the local back gate is grounded and the channel region is covered by a normal high-k & metal gate stack. The source and drain regions are then doped with K (Potassium) [3].

2.3. NW (Nanowire) Technology

Nanowire based device technology is also an emerging field and is popular because of the ability to produce high density logic devices while occupying a lower chip real estate and consuming low power. This is an attractive technology for the energy SoC, but the major drawback of NW technology is their integration into circuits. Although there are several NW assembly techniques such as NW-TFTs, crossed NWs, direct NW growth [4], most of the integration processes involved are either not compatible or if they are they don't have the required performance. In a recent work, Kälblein et al. fabricated a back-gated ZnO NW nFET exhibiting an off-state drain current less than 1 pA, $I_{on}/I_{off} = 10^7$ and an electron mobility of 50 cm^2/Vs. The ZnO NWs are grown using wet chemical synthesis at 150 °C in an aqueous solution of sodium hydroxide and ammonium peroxodisulfate using a zinc foil as the growth substrate. Annealing at 600°C is performed to remove dopants from within the ZnO nanowires. The synthesized NWs are then transferred to a heavily doped thermally oxidized silicon substrate. Aluminum contacts are used for the source and drain. The heavily doped silicon substrate acts as the gate electrode [5].

2.4 NEMS (Nano electro mechanical systems) Switches

CNT and graphene based NEMS are currently in focus as these materials exhibit excellent mechanical properties and high electron mobility. Fujita et al., have demonstrated CNT- NEMS that operate in the GHz range at CMOS comparable gate voltages [6]. Graphene – NEMS have been explored by Chen et al., where vibrational frequencies in the MHz range were achieved [7]. Hybrid CMOS-NEMS circuits have been fabricated to combine memory and logic circuits together. Using CMOS integrating techniques, Han et al., successfully fabricated such a hybrid device using a fin flip-flop

actuated channel transistor, that exhibit very high data retention type [8]. Our proposal is to use such a hybrid design for certain portions of the control circuit.

3. Power Generation

3.1 Microbial Fuel Cell (uMFC)

A microbial fuel cell (Fig. 2) is an innovative device for energy production based on bio-electrochemical reactions made by bacteria when decomposing organic matter in anaerobic conditions [9]. Typically it consists of anode and cathode compartments separated by a membrane (Proton Exchange Membrane). In the anode compartment, fuel is oxidized by microorganisms, generating electrons and protons. Electrons are transferred to the cathode compartment through an external electric circuit (load), and the protons are transferred to the cathode compartment through the membrane. Electrons and protons are consumed in the cathode compartment, combining with oxygen to form water.

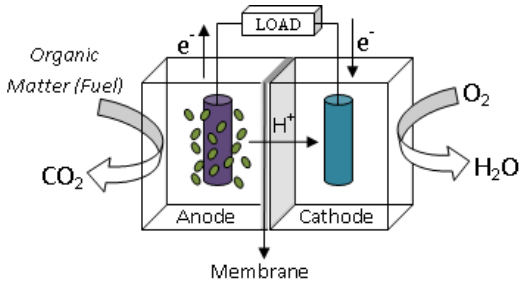

Fig. 2: Operation principle of a Microbial Fuel Cell

So far, researchers have focused their efforts to create macro-scale MFC for the massive production of energy [10-12]. In another approach, a micro version MFC could act as an alternative power source for self-powered microsystems [13]. In the energy SoC, our goal was to create an enhanced MFC using microfabrication techniques and novel nanomaterials, thus greatly improving the output energy density. The central breakthrough of this design encompasses the microfabrication of the smallest MFC reported thus far [14], and the use of a 3D structure CNT-based anode, with a high surface area-to-volume ratio [15] [Fig. 3]. The fabrication process of this proposed design is summarized in Fig. 4.

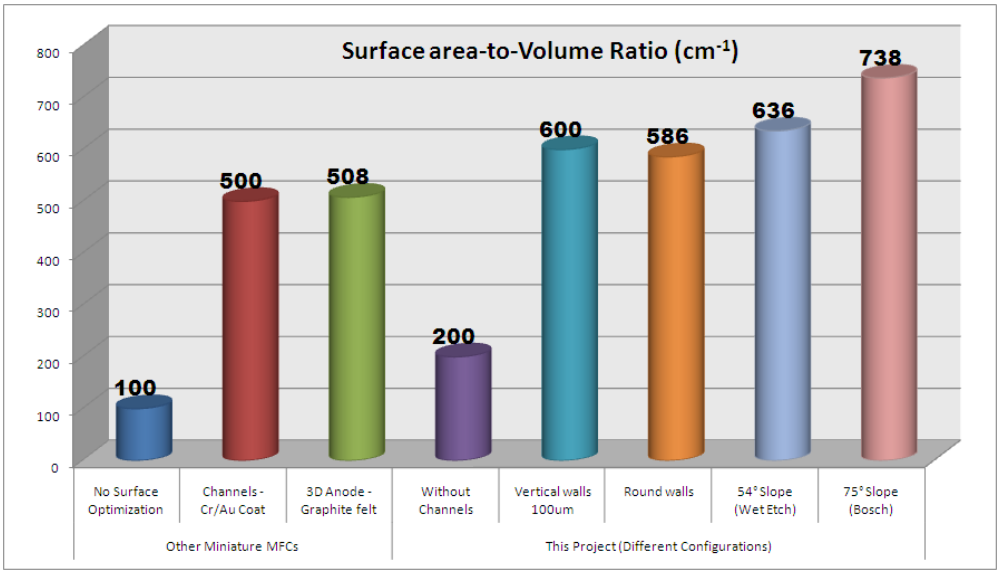

Fig. 3: With intelligent design it is possible to achieve very high SVR.

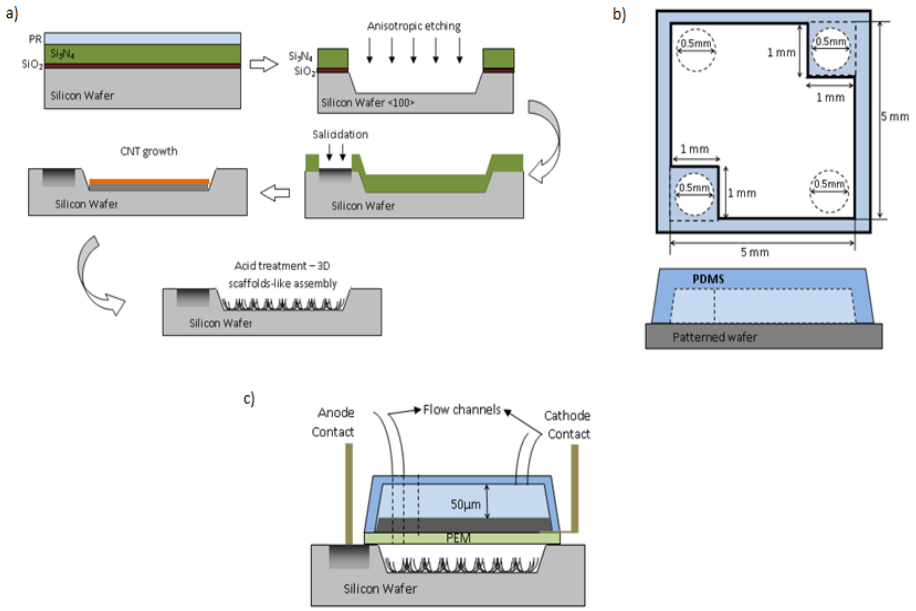

Fig. 4: Micro-sized Microbial Fuel Cell fabrication process. a) Anode chamber. b) Cathode chamber fabrication. c) Final MFC Assembly.

3.2 Lithium Ion Battery (LIB)

Without any doubt, the best option among the energy storage technologies is the Lithium Ion Battery (LIB). Its power density per unit volume or per unit mass cannot be matched. Consequently the LIB would be a key component in the energy generation module of the chip. Nowadays, increasing the energy density, cycling life and charge/discharge rate capability are the main concerns for the improvement of the LIB. In order to achieve this, two different alternatives are proposed [16]; the use of hollow nanostructures or the use of nanowires. In the first case, the energy storage capacity is increased due to the extra space for electrochemical reaction of lithium ions inside the cavities in the hollow structures. [17] For the second case, a particular composition for the nanowires can be used which combines the efficient electron conductivity of carbon and the very high lithium ion storage capacity of the silicon ($4200 mA.h.g^{-1}$). Using either of these schemes it is possible to increase the storage capacity and cycling life of the battery [18]. Fig. 5 shows the fabrication process to integrate one of the systems into the energy chip.

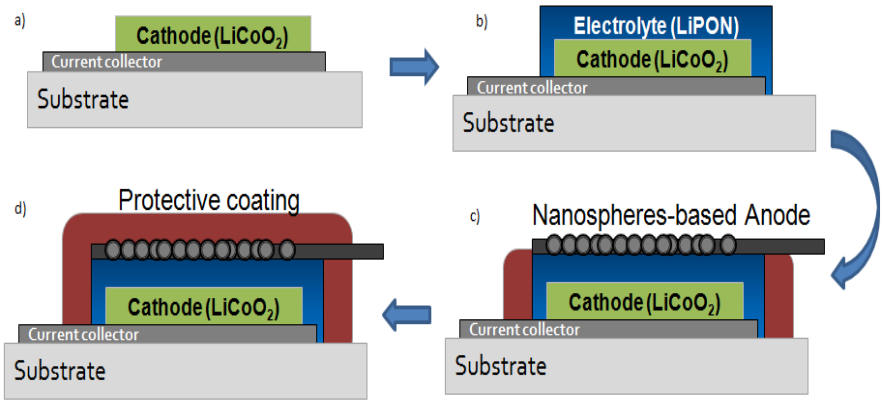

Fig. 5: Nanospheres-based Anode - Lithium Ion µBattery - fabrication process flow. a) Deposition of metal (current collector) and cathode ($LiCoO_2$). b) Deposition of solid electrolyte (LiPON). c) Deposition of a protective coating and placing of the NS-based Anode. (60 wt % NS, 30 wt % of conductive agent, 10 wt % of binder). d) Last Protective coating.

3.3 Thermoelectric Power Generator (TEG)

Aggressive scaling of transistor sizes from the micrometer to the nanometer range has caused a significant increase in power (gate-leakage) dissipation (Fig. 6). Removal of this heat is continually becoming a problem with conventional heat removal techniques, especially in portable mobile devices. To tackle this, transistors with different dielectric material and metal gate topologies have been proposed and developed. Nonetheless there will always be some amount of heat dissipation in CMOS circuits.

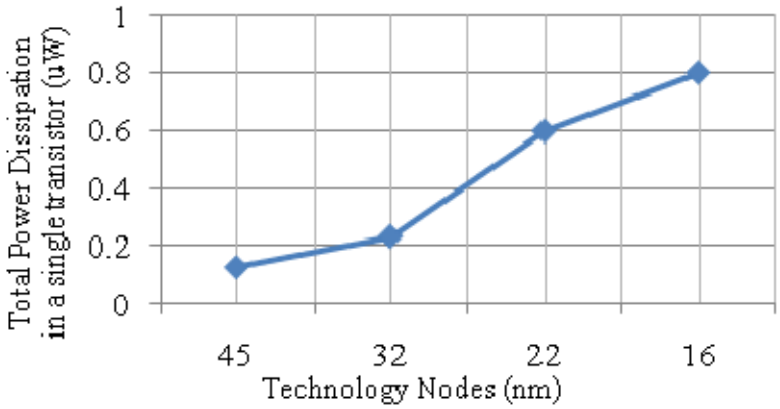

Fig. 6: Total power dissipation (μW) in a single transistor at different technology nodes using high-k (La_2O_3) dielectric material.

The Energy SoC is proposed to have a TEG that converts heat dissipated from the load application and the power consumption section into reusable energy that charges the LIB. Based on a comparative study on the conversion efficiency and figure of merit (ZT) for different thermoelectric materials Bi_2Te_3 & $(Bi,Sb)_2Te_3$ was chosen for the TEG [19]. Fig. 7 shows the thermal efficiency of this thermoelectric material.

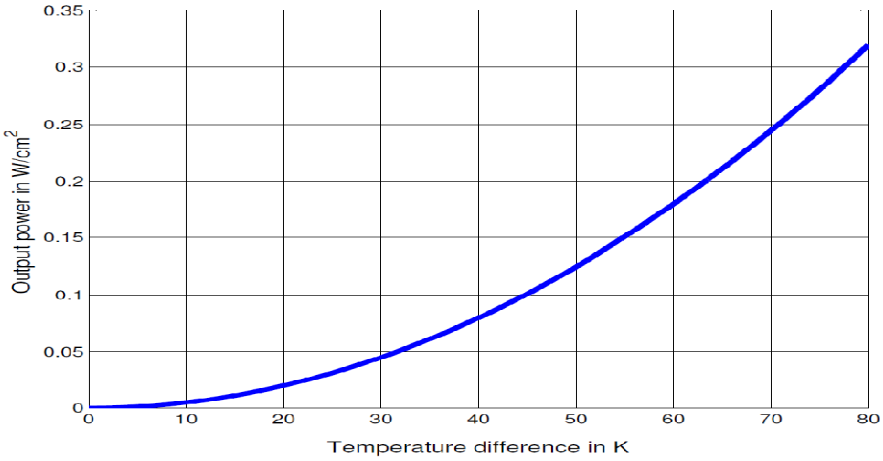

Fig. 7: Output power (W) of proposed TEG (per cm^2) vs. temperature difference (K).

3.4 Piezoelectric Nanogenerator (PNG)

The objective of the energy chip is to harness energy from a variety of sources. Because this device is targeted towards mobile/remote harsh environment applications, it will be subjected to lots of movement, strain & vibrations. Our proposed design of the energy chip is to include a piezoelectric device that converts these mechanical signals to electric power. A recent development in piezoelectric nanogenerators proposed by Wang et al. showed the possibility of using

ordered ZnO NWs (grown by VLS) and a zig-zag patterned Pt metal probe contact to convert the aforementioned mechanical signals into DC current. From a single 300 nm diameter & 0.2um-0.5um long ZnO, 45 mV output voltage has been reported. The target applications for the energy chip are proposed to be in remote applications that require one time installation. The NW based PNG is targeted for applications such as a pace-maker, day-to-day mechanical movements such as with cell phones and harsh environment scenarios such as in strong wind regions, changes in pressure, acoustic or ultrasonic waves. Because this PNG is targeted to work in a wide frequency band (Hz-MHz), the resonance of individual NWs does not play a role in power generation. The important thing is for the NWs in the PNG to experience movement/bending to generate DC current. Zhang et al., have proposed nanodevice applications using ZnO NW based piezoelectric generators in blood-pressure and sugar monitoring, in-vivo detection of cancer cells and remote sensing of gas and chemicals. The reported power density per unit substrate area was 0.1–0.2 $mWcm^{-2}$ [20] [26].

3.5 NW based solar cells

In addition to the above energy harvesters, a solar cell is also proposed to be integrated into the energy chip. In a recent publication, Javey et al. demonstrated a solar cell (SNOP) based on n-CdS nanowires grown on an anodized aluminum membrane and a p-CdTe thin film. The ordered single crystal CdS nanowire array coupled with the CdTe photo absorption layer, an efficiency of 6% was demonstrated from a 5 x 8 mm chip [21].

4. Analytical Calculations

Based on the data from previous miniature MFCs [22], and given the dimensions and improvements involved in our design, we estimate a power density of $10\mu W/cm^3$. So, considering the volume of our MFC to be 1.25µL, 12.5nW of power is achievable. For the purpose of analysis, the TEG assumed is the MPG-D602 device from Micropelt® having 450 (n-Bi_2Te_3 & p-$(Bi,Sb)_2Te_3$) couples and an area of $0.082cm^2$ [19]. The processors in mobile devices such as laptops, cell phones, PDAs etcetera can develop temperature differences of approximately 60^0C with respect to ambient, even after heat sinking/cooling and operation under normal load. Again for analytical purposes, a low temperature difference of 30^0C is chosen. Using the plot data in Fig.7, the TEG output power is estimated at 4mW. Looking at the thin film batteries that use a thick $LiCoO_2$ layer as cathode (>4µm), energy densities of 2-3mWh/cm^2 have been reported [23]. From this information, we can estimate an output power of 2-3mW, having integrated a battery of 1cmx1cm area, working for an hour. From [20] the PNG is reported to have an output power density of 0.1 - 0.2mW/cm^2. Assuming that the integrated PNG occupies an area of 1 cm^2, the output power ranges from 0.1-0.2mW. Considering that the NW based solar cell [21] occupies an area of $0.4cm^2$. Assuming that the illumination intensity over this area is 17-100 mW/cm^2 and that the efficiency if 6% as described in [21], the output power ranges from 0.41– 2.4mW.

The energy independent SoC is proposed to work in harsh environment conditions having significant temperature differences, changes in pressure or places with abundant solar energy. The SoC may or may not be subjected to all these conditions at the same time. The idea is to harvest energy from whatever condition is available at any given time and place. The maximum power that can be generated with the energy independent SoC, with all power generation components active (TEG, PNG, Solar Cell) is estimated to be between 5.51mW and 9.5mW based on above calculations. The recently introduced Phoenix processor is a very low power device that consumes just 39pW [24]. If this is assumed to be at the center of the on-chip control unit, using the plot in Fig. 6, the energy SoC is capable of running approximately 40000 transistors at the 45 nm node, 20000 transistors at the 32 nm node, 7000 transistors at the 22 nm node and a hypothetical 5000 transistors at the 16 nm technology node. Fig. 6 data on single transistor power dissipation at different technology nodes are based on theoretical calculations using the ASU predictive technology files at a 1 GHz clock frequency [25]. The above approximations were made also taking into consideration the use of high-k/metal-gate. We estimate an even higher number of transistors with CNT and NW technology.

5. Conclusion

We have presented a pragmatic analysis on the potential reality of a self-powered SoC for variety of important applications. We also show that it is possible to supply 4mW power to run an ultra low power system. Choice of materials, efficient circuit design and CMOS compatible integration will be keys to realize such device.

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