Semiconductor nanowire array: potential substrates for photocatalysis and photovoltaics

Yiying Wu, Haoquan Yan, Peidong Yang

Chemistry Department, University of California, Berkeley, CA 94720, USA

A novel vapor–liquid–solid epitaxy (VLSE) process has been developed to synthesize high-density semiconductor nanowire arrays. The nanowires generally are single crystalline and have diameters of 10–200 nm and aspect ratios of 10–100. The areal density of the array can readily approach 10^{10} cm^{-2}. Results based on Si and ZnO nanowire systems are reported here. Because of their single crystallinity and high surface area, these nanowire arrays could find unique applications in photocatalysis and photovoltaics.

KEY WORDS: semiconductor nanowires; Si and ZnO nanowires

1. Introduction

Nanoscale one-dimensional (1D) materials have stimulated great interest due to their importance in basic scientific research and potential technology applications [1,2]. A lot of unique and fascinating properties have been proposed and demonstrated for this class of materials, such as metal-insulator transition [3], superior mechanic toughness [4], higher luminescence efficiency [5,6], enhancement of thermoelectric figure of merit [7] and lowered lasing threshold [8–10]. One-dimensional materials can also be used as building blocks to construct a new generation of nanoscale electronic circuits and photonics [11–15]. While most of the research efforts have been directed towards the exploration of optoelectronic applications of these 1D nanostructures, chemical properties of the 1D nanostructures (catalysis, for example) have been overlooked. Many of these 1D nanostructures and their assemblies, with their excellent crystallinity and high surface area, could also be potentially used in several important chemical applications, for example, photocatalysis and photovoltaics.

An important issue in the study and application of 1D materials is how to assemble individual atoms into 1D structures in a fast and controllable way. A number of nanolithographic techniques, such as electron-beam lithography [16], proximal probe patterning [17,18] have been developed. These processes, however, generally are slow and the cost is high. Chemical synthesis represents another important approach to 1D structures [19–26]. It is much more promising, in terms of cost, throughput and potential for high volume production. A significant challenge of the chemical synthesis is how to rationally control the nanostructures so that their interface and ultimately their 2-dimensional and 3-dimensional superstructures can be tailor-made towards desired functionality. Below, we describe the investigations from our laboratory directed toward controlled growth of inorganic nanowires, particularly the controlled growth of semiconductor nanowire array through the vapor–liquid–solid epitaxy (VLSE) process.

2. Vapor–Liquid–Solid nanowire growth mechanism

Single crystalline inorganic nanowire is an interesting example of anisotropic form of crystal. The diameter of nanowires is in the range 1–200 nm and the length is several microns or longer. In general, nanowires will not be thermodynamically stable as compared to their bulk materials. Consequently, a central question in nanowire growth is how to promote anisotropic crystal growth kinetically. A well-accepted mechanism of nanowire growth via gas phase reaction is the so-called Vapor–Liquid–Solid (VLS) process proposed by Wagner in 1960s, during his studies of large single-crystalline whisker growth [27,28]. According to this mechanism, the anisotropic growth is promoted by the presence of liquid alloy–solid interface. This process is illustrated in figure 1 for the growth of Si nanowire with Au cluster as solvent at high temperature. Based on Si–Au binary phase diagram, Si (from the decomposition of SiH_4, for example) and Au will form liquid alloy when the temperature is higher than the eutectic point (363 °C, figure 1(I)). The liquid surface has a large accommodation coefficient and is therefore a preferred site of deposition for incoming Si vapor. After the liquid alloy becomes supersaturated with Si, Si nanowire growth occurs by precipitation at the solid–liquid interface (figure 1(II–III)).

Recently, the direct observation of Ge nanowire growth in real time was conducted in a high-temperature *in-situ* transmission electron microscope (TEM) [29]. The experiment result clearly shows three growth stages: formation of Au–Ge alloy (figure 2(b), (c)), nucleation of Ge nanocrystal (figure 2(d)) and elongation of Ge nanowire (figure 2(e), (f)). This experiment unambigu-

1022-5528/02/0400-0197/0 © 2002 Plenum Publishing Corporation

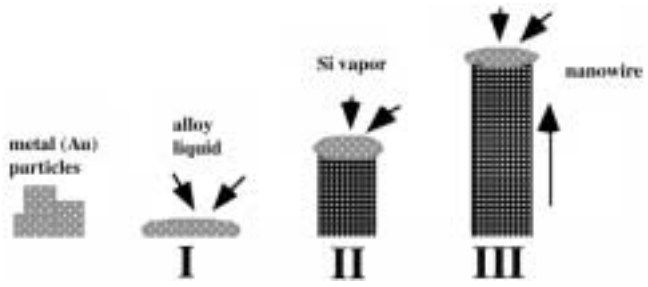

Figure 1. Schematic illustration of a vapor–liquid–solid nanowire growth mechanism including three stages: (I) alloying, (II) nucleation, and (III) axial growth.

ously demonstrates the validity of the VLS mechanism for nanowire growth. The establishment of a VLS mechanism at nanometer scale is very important for the rational control of inorganic nanowires since it provides the necessary underpinning for the prediction of solvents and preparation conditions.

Based on our mechanism study of the nanowire growth, it is conceivable that one can achieve controlled growth of nanowires at different levels. First of all, one can synthesize nanowires of different compositions by choosing suitable solvents and growth temperature. A good solvent should be able to form liquid alloy with the desired nanowire material, ideally two of them should be able to form eutectic; meantime, the growth temperature should be higher than the eutectic point, but lower than the melting point of the nanowire material. Both physical methods (laser ablation, arc discharge, thermal evaporation) and chemical methods (chemical vapor transport and chemical vapor deposition) can be used to generate the vapor species required during the nanowire growth. As an example, figure 3 shows Ge nanowires synthesized by a chemical vapor transport process [19]. Figure 3(a) shows the binary phase diagram of Au–Ge system. As shown in the diagram, Au is a good solvent for the growth of Ge nanowires because of the existence of the Au–Ge eutectic. Nanowires of many different materials have been synthesized by both chemical and physical methods, including elemental semiconductors (Si and Ge), III–V semiconductors (GaAs, GaP, InP, InAs), II–VI semiconductors (ZnS, ZnSe, CdS, CdSe), oxides (ZnO, MgO, SiO_2) [19–26].

One can further control the nanowire diameters by choosing metal clusters of different sizes, which we have successfully demonstrated in the Si nanowire case. By using monodispersed metal nanoclusters, nanowires with a narrow diameter distribution can be created. We have utilized this strategy to grow uniform Si nanowires in a chemical vapor deposition system [29]. Uniform nanowires with 20.6 ± 3.2, 24.6 ± 4.0, 29.3 ± 4.5 and 60.7 ± 6.2 nm in diameter were grown using Au clusters with sizes of 15.3 ± 2.4, 20.1 ± 3.1, 25.6 ± 4.1 and 52.4 ± 5.3 nm, respectively. Figure 4(a) shows a field emission scanning electron microscope (FESEM) image of uniform, long and flexible nanowires using 15 nm Au clusters as solvent. Figure 4(b) shows a TEM picture with both Au clusters and the grown Si nanowires. The correlation between the size of Au clusters and the diameter of Si nanowires can been clearly observed. Similar results have also been observed in GaP nanowires prepared by laser ablation method [30].

3. Vapor–Liquid–Solid Epitaxial growth of semiconductor nanowire array

More importantly, it is possible to apply the conventional epitaxial crystal growth technique into this VLS process to achieve orientation control. By choosing a suitable substrate whose lattice constants match with the desired nanowire crystal structure, the growth direction can be dictated by the choosing substrate orientation. This technique, vapor–liquid–solid epitaxy

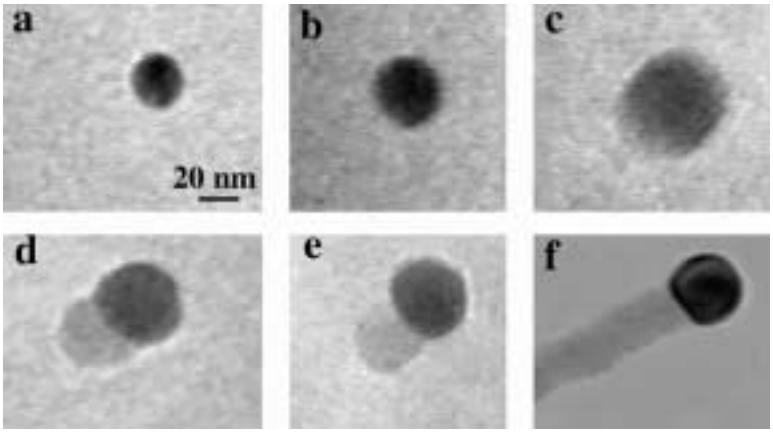

Figure 2. *In-situ* TEM images recorded during the process of nanowire growth. (a) Au nanoclusters in solid state at 500 °C; (b) alloying initiates at 800 °C, at this stage Au exists mostly in solid state; (c) liquid Au/Ge alloy; (d) the nucleation of Ge nanocrystal on the alloy surface; (e) Ge nanocrystal elongates with further Ge condensation and eventually forms a wire (f).

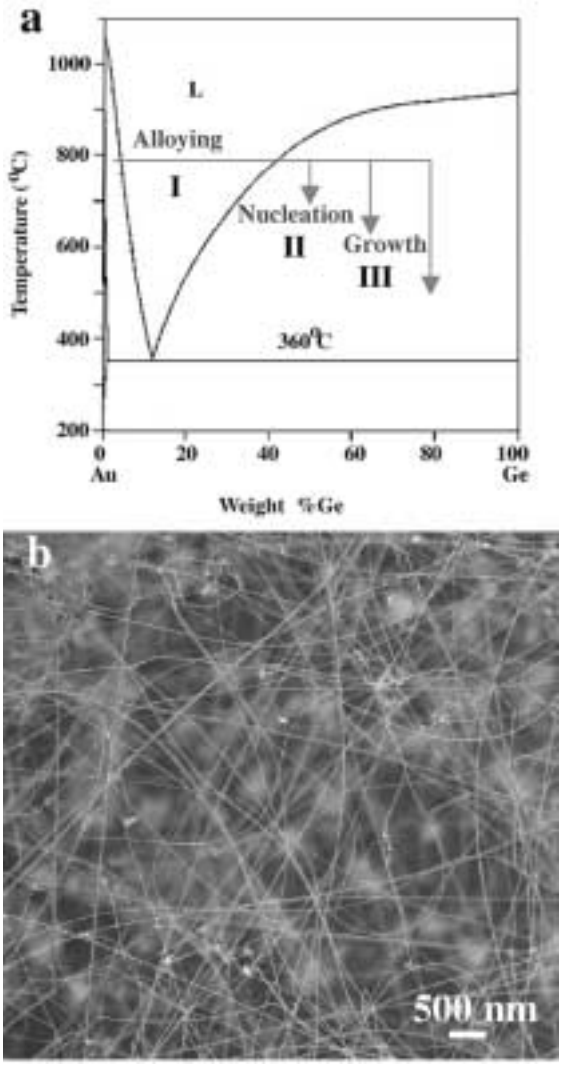

Figure 3. (a) Au–Ge binary phase diagram; (b) SEM image of the as-made Ge nanowires.

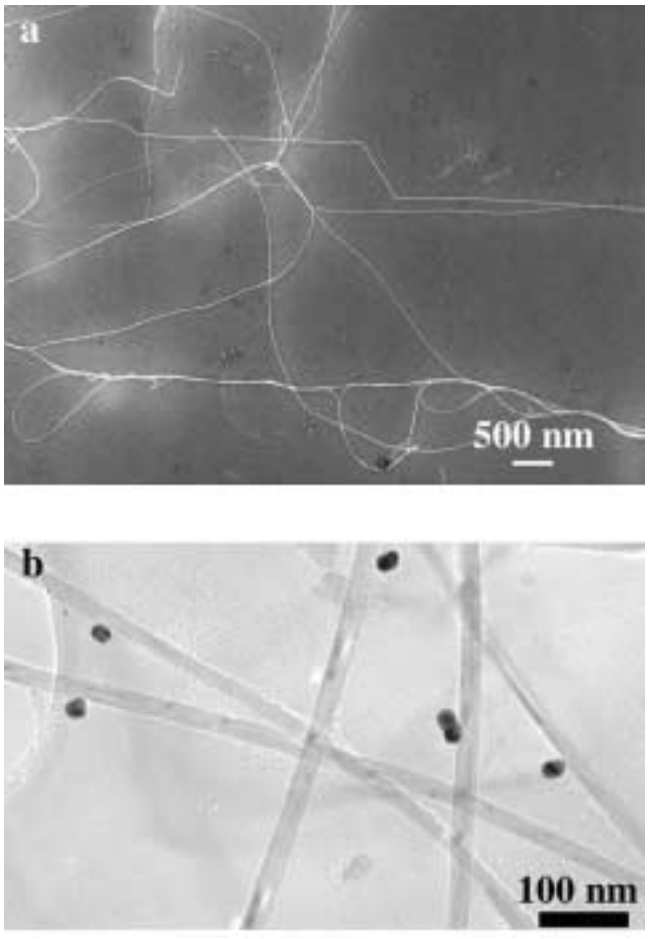

Figure 4. (a) FESEM image of Si nanowires grown on Au clusters embedded in mesoporous silica thin film; (b) TEM image of the nanowires and the Au clusters dispersed on the same copper grids.

(VLSE), is particularly powerful in controlled synthesis of nanowire arrays.

3.1. Orientation control

Controlling the growth orientation is important for many of the proposed application of nanowires. Nanowires generally have a preferred growth direction. For example, semiconductor Si nanowires prefer to grow along the $<111>$ direction, ZnO prefer to grow along the $<001>$ direction. One strategy to grow vertically-aligned nanowires is to properly choose the substrate and to control the reaction conditions, so that the nanowires grow epiaxially on the substrate. Take Si as an example, Si nanowires prefer to grow along the $<111>$ direction. If (111) Si wafer is used as a substrate, Si nanowires will grow epitaxially and vertically on the substrate and form nanowire array (figure 5(a)). Figure 5(b) shows the obtained Si nanowires array grown at 1050 °C with $SiCl_4$ and H_2 as reactants on (111) Si wafer. They are typically 80 nm in diameter and 10 microns in length. The effect of epitaxial nanowire growth is obvious. If (001) Si wafer was used as substrate instead, three sets of oriented Si nanowire arrays can be epitaxially grown out of the wafer surface along the three equivalent $<111>$ directions (figure 5(c)). As a comparison, Si nanowires grown randomly (non-epitaxially) on Si wafer coated with thick layer of SiO_2 (figure 4(a)).

Another VLSE example is ZnO nanowires grown epitaxially on *a*-plane (110) sapphire substrate [15]. ZnO nanowires have wurzite structure with lattice constant $a = 3.24$ Å and $c = 5.19$ Å and prefer to grow along $<001>$ direction. ZnO nanowire can grow epitaxially on (110) plane of sapphire, because ZnO *a* axis and sapphire *c* axis are related almost by a factor of 4 (mismatch less than 0.08% at room temperature, figure 6(a) [41]. Figure 6(b) shows vertical ZnO nanowire arrays on *a*-plane sapphire substrate. Their diameters range from 70–120 nm and lengths can be adjusted

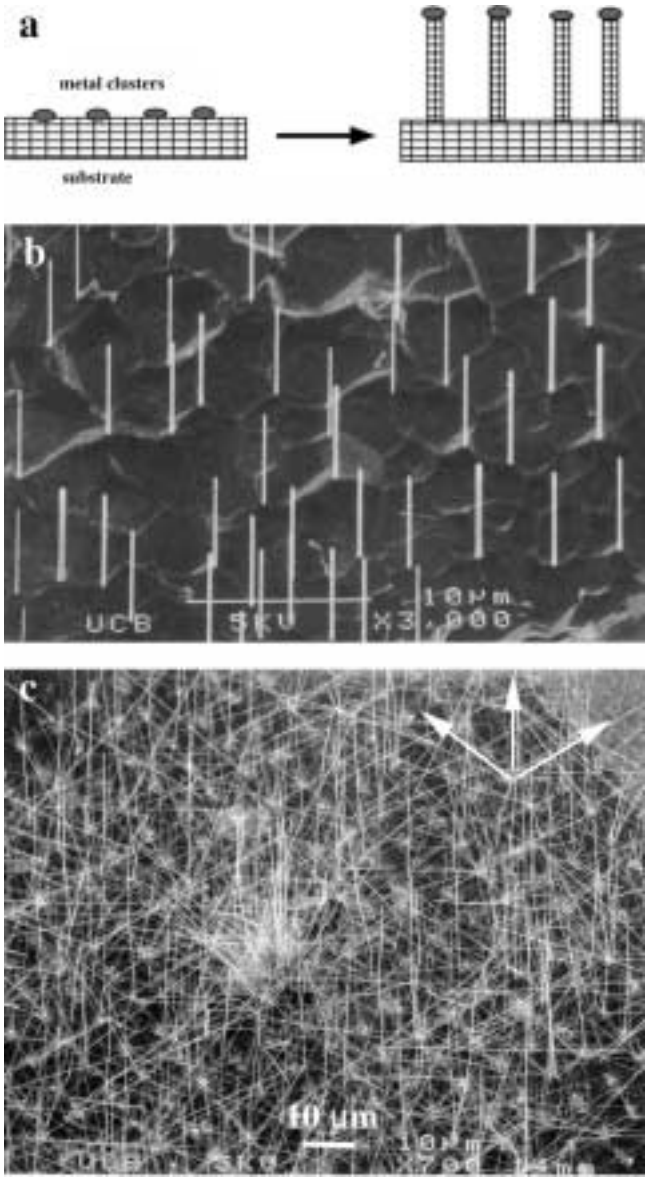

Figure 5. (a) Schematic illustration of the VLSE process; (b) vertical Si nanowire array grown on a (111) Si wafer; (c) three sets of Si nanowire arrays interpenetrate on the surface of a (100) Si substrate, the three preferred orientation were indicated by arrows.

between 2–10 microns. Previously, InAs nanowhiskers have been oriented on a Si substrate using a fairly complicated metalorganic vapor-phase epitaxy technique [31].

3.2. Positional control

It is almost apparent from the VLS nanowire growth mechanism that the positions of nanowires can be controlled by the initial position of Au clusters or thin films. Various lithographical techniques including, for example, soft lithography, *e*-beam and photo-

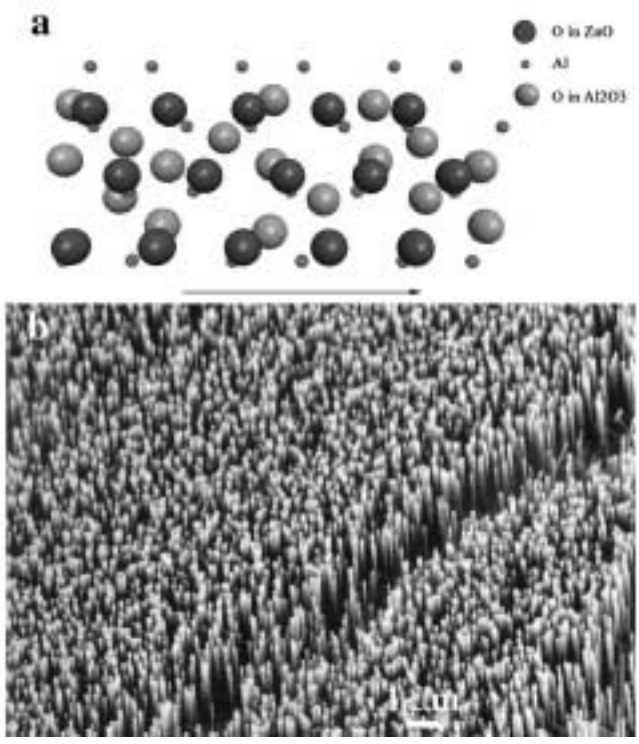

Figure 6. The epitaxial growth of ZnO nanowires on *a*-plane (110) sapphire can be readily seen by examination of the crystal structures of ZnO and sapphire ($a = 0.4754$ nm, $c = 1.299$ nm). (a). Schematic illustration of ZnO *ab*-plane overlapping with the underlying (110) plane of sapphire substrate. The arrow is drawn along the *a*-axis of ZnO structure and the *c*-axis of the sapphire crystal structure. (b) Arrays of ZnO nanowires grown on *a*-plane sapphire substrate.

lithography can be used to create patterns of Au thin film for the subsequent semiconductor nanowire growth. Figure 7 shows the SEM images of ZnO nanowires grown from the line and square Au pattern on *a*-plane sapphire substrate. It is clear that nanowires grow vertically only from the region that is coated by Au and form the designed pattern of ZnO nanowire array [15].

3.3. Density control

During the nanowire array growth, generally gold thin film was deposited as the solvent/initiator for the nanowire growth. Upon heat-up, these gold thin films will self-aggregate into high density of Au clusters. The diameters and the density of these clusters are determined by the thickness of the thin film and the growth temperature. Thus, it is possible to control the nanowire areal density by modifying the thin film thickness.

Another approach to control the areal density of the nanowire array is to use the solution-made Au clusters. By dispersing a different amount/density of Au clusters on the sapphire substrate, it is possible to obtain nanowire arrays with different densities. We can now

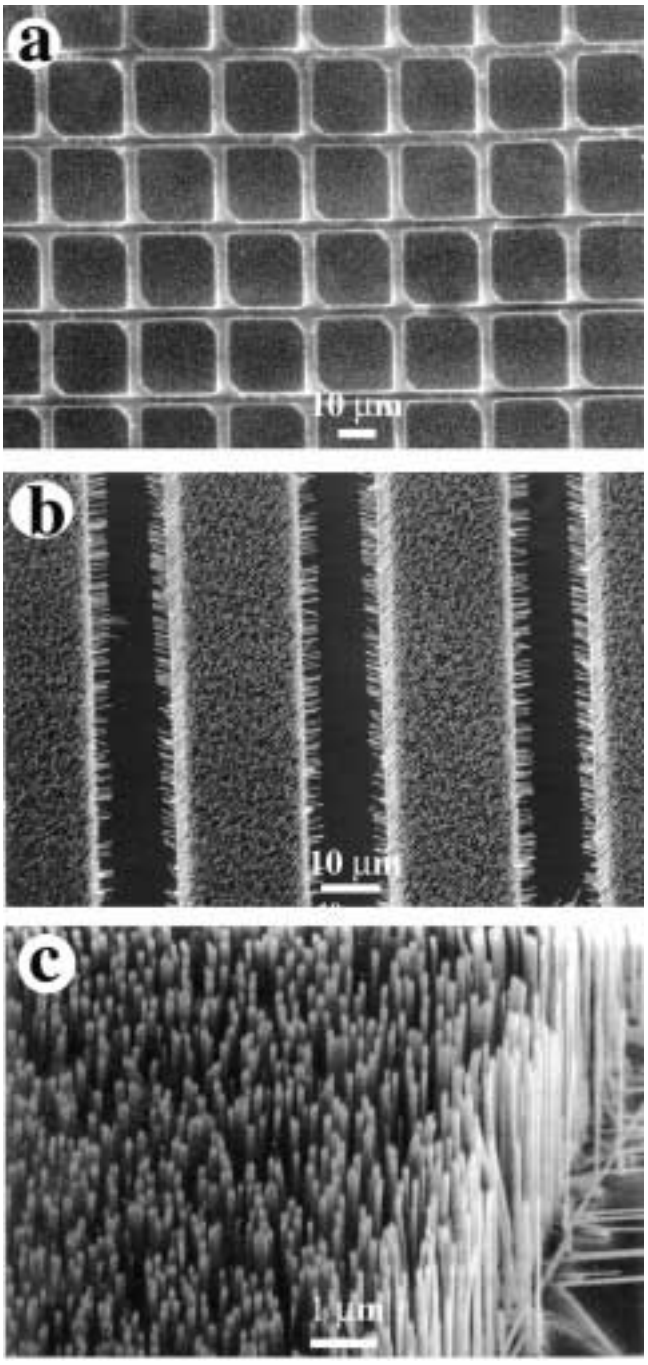

Figure 7. Site-selective growth of ZnO nanowire arrays on *a*-plane substrates. The pattern of nanowire array is defined by the initial Au thin film pattern fabricated by photolithography.

readily synthesize, for example, ZnO nanowire arrays with areal density spanning from 10^6 to $10^{10}\,cm^{-2}$.

3.4. Nanowire array as potential substrates for photocatalysis and photovoltaics

The characteristics of these semiconductor nanowire arrays (high crystallinity, high density, high surface area, and easy surface functionalization) suggest they could be used as a new class of semiconductor electrodes for photovoltaics. One of the exciting applications of these nanowire array electrodes could be the "Grätzel solar cell". Conventional cell is based on nanoporous and nanocrystalline TiO_2 or ZnO on which a monolayer of a light absorbing dye is adsorbed. Replacing nanoparticles with nanowires could remove one of the electron transport bottlenecks occurring in the conventional Grätzel cell, i.e., the tunneling process between neighboring oxide nanocrystals. With nanowire electrodes, electron can be transport directly to the conducting substrate without going through the multiple steps of the tunneling process, which is expected to be able to greatly decrease the probability of recombination across large heterogeneous interface and improve the overall efficiency of the solar cell [32].

In addition, these semiconductor nanowire arrays could also be used as sensitizers for a light-induced redox process. When these wires are illuminated with photons with energy larger than their band gap, electron hole pairs will be generated. If a suitable scavenger or surface defect state is available to trap the electron or hole, electron-hole recombination can be prevented and the surface redox process may occur consequently. The valence band holes are powerful oxidants while the conduction band electrons are good reductants. The high surface area and single crystallinity of the nanowires in the array architectures represents an interesting substrate to explore their capability to carry out photocatalytic reaction, for example, photocatalyzed oxidation of chlorinated hydrocarbon for environmental remediation applications [33].

4. Conclusion

In this article, we have given a brief survey of work, drawn primarily from the authors' laboratory, directed toward the rational growth of semiconductor nanowires. The VLS mechanism has proven to be a valuable guide in choosing catalyst and reaction conditions. Based on this mechanism, nanowires of a wide range of single-crystal elemental and compound materials have been prepared. The ability to control growth represents a significant step toward the applications of nanowires as building blocks in nanoscale electronics and photonics. In the future, many properties can be investigated, such as electron transport, optical, photoconductivity, thermoelectricity as well as their chemical properties.

Acknowledgement

This work was supported in part by a New Faculty Award from the Dreyfus Foundation, a Career Award from the National Science Foundation (DMR-0092086), Department of Energy and start-up funds from the Uni-

versity of California, Berkeley. P.Y. is an Alfred P. Sloan Research Fellow. P.Y. thanks the 3M company for an untenured faculty award. We thank the National Center for Electron Microscopy for the use of their facilities.

References

[1] *Handbook of Nanostructured Materials and Nanotechnology*, ed. H.S. Nalwa (Academic Press, 2000).
[2] J. Hu, T.W. Odom and C.M. Lieber, Acc. Chem. Res. 32 (1999) 435.
[3] *Highly Conducting One-Dimensional Solids*, eds. J.T. Devreese, R.P. Evrard and V.E. van Doren, (Plenum: New York, 1979).
[4] E.W. Wang, P.E. Sheehan and C.M. Lieber, Science 277 (1997) 1971.
[5] L.T. Canham, Appl. Phys. Lett. 57 (1990) 1046.
[6] J.D. Holmes, K.P. Johnston, R.C. Doty and B.A. Korgel, Science 287 (2000) 1471.
[7] L.D. Hicks and M.S. Dresselhaus, Phys. Rev. 47 (1996) 16631.
[8] Y. Arakawa and H. Sakaki, Appl. Phys. Lett., 40 (1982) 939.
[9] Y. Arakawa, A. Yariv, IEEE J. Quantum Electron. 22 (1986) 1887.
[10] Y. Miyamoto, Y. Miyake, M. Asada and Y. Suematsu, IEEE J. Quantum Electronics, 25 (1989) 2001.
[11] Y. Cui and C.M. Lieber, Science 291(2001) 851.
[12] T. Rueckes, K. Kim, E. Joselerich, G.Y. Tseng, C. Cheung and C.M. Lieber, Science 289 (2000) 94.
[13] M.S. Fuhrer, J. Nygard, L. Shih, M. Forero, Y. Yoon, M.S.C. Mazzoni, H.J. Choi, J. Ihm, S. Louie, A. Zettle and P.L. McEuen, Science 288 (2000) 494.
[14] S. Noda, K. Tomoda and N. Yamamoto, A. Chutinan, Science 289 (2000) 604.
[15] M. Huang, S. Mao, H. Feick, H. Yan, Y. Wu, H. Kind, E. Weber, R. Russo and P. Yang, Science 292 (2001) 1897.
[16] *Handbook of Microlithography, Micromachining, and Microfabrication*, ed. P. Rai-Choudhury (SPIE press, IEE, 1999).
[17] C.M. Lieber, J. Liu and P.E. Sheehan, Angew. Chem. Int. Ed. Engl. 35 (1996) 687.
[18] R.D. Piner, J. Zhu, F. Xu, S. Hong and C.A. Mirkin, Science 283 (1999) 661.
[19] Y. Wu and P. Yang, Chem. Mater. 12 (2000) 605.
[20] M.H. Huang, Y. Wu, H. Feick, E. Webber and P. Yang, Adv. Mater. 13 (2000) 113.
[21] A.M. Morales and C.M. Lieber, Science 279 (1998) 208.
[22] C.R. Martin, Science 266 (1994) 1961.
[23] W. Han, S. Fan, W. Li and Y. Hu, Science 277 (1997) 1287.
[24] T.J. Trentler, K.M. Hickman, S.C. Geol, A.M. Viano, P.C. Gibbons and W.E. Buhro, Science 270 (1995) 1791.
[25] Y. Li, Y. Ding and Z. Wang, Adv. Mater. 11 (1999) 847.
[26] X. Duan and C.M. Lieber, Adv. Mater. 12 (2000) 298.
[27] R.S. Wagner and W.C. Ellis, Appl. Phys. Lett. 4 (1964) 889.
[28] R.S. Wagner, in: *Whisker Technology*, ed. A.P. Levitt, (Wiley, New York, 1970) p. 47.
[29] Y. Wu and P. Yang, J. Am. Chem. Soc. 123 (2001) 3165.
[30] M.S. Gudiksen and C.M. Lieber, J. Am. Chem. Soc. 122 (2000) 8801.
[31] S.T. Hiruma, M. Shirai, K. Tominaga, K. Haraguchi, T. Katsuyama and T. Shimada, Appl. Phys. Lett. 66 (1995) 159.
[32] P.E. de Jongh, E.A. Meulenkamp, D.Vanmaekelbergh and J.J. Kelly, J. Phys. Chem. 104 (2000) 7686.
[33] M.R. Hoffmann, S.T. Martin, W. Choi and D.W. Bahnemann, Chem. Rev. 95 (1995) 69.