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Semiconductor Nanowires: From Self-Organization to Patterned Growth

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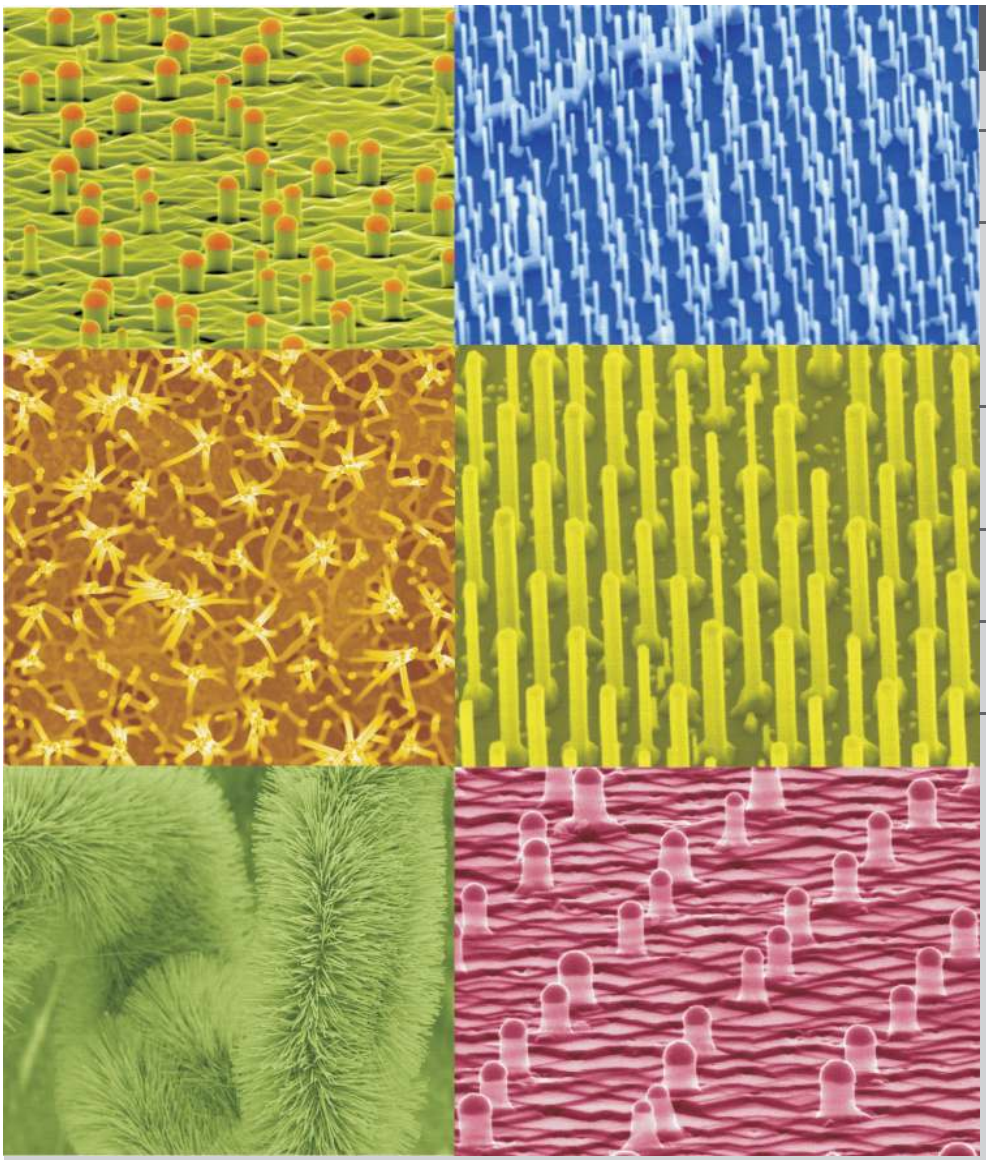

Growth of nanowires can be controlled so that ordered arrays can be prepared.

Keywords:
- nanopatterning
- nanowires
- self-assembly
- semiconductors
- template synthesis

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The synthesis of semiconductor nanowires has been studied intensively worldwide for a wide spectrum of materials. Such low-dimensional nanostructures are not only interesting for fundamental research due to their unique structural and physical properties relative to their bulk counterparts, but also offer fascinating potential for future technological applications. Deeper understanding and sufficient control of the growth of nanowires are central to the current research interest. This Review discusses the various growth processes, with a focus on the vapor–liquid–solid process, which offers an opportunity for the control of spatial positioning of nanowires. Strategies for position-controlled and nanopatterned growth of nanowire arrays are reviewed and demonstrated by selected examples as well as discussed in terms of larger-scale realization and future prospects. Issues on building up nanowire-based electronic and photonic devices are addressed at the end of the Review, accompanied by a brief survey of recent progress demonstrated so far on the laboratory level.

1. Introduction

A number of phenomena in solid-state physics that are closely related to artificial nanostructured materials have been established over the last 15 years. New methods and equipment for high-resolution investigation of solid-state materials have been developed, which have strongly affected current insight in nature. The first report on carbon nanotubes by Iijima[1] resulted in a worldwide exponential increase of research into one-dimensional structures based on carbon and other materials.

Ongoing device miniaturization and innovative new structures are major factors for the economical survival of the current integrated circuit industry. However, further decreases in device dimensions are now starting to reach the regime where classical physics becomes invalid and, hence, the function of the circuit might not be guaranteed. A typical example is the leakage problem of ultrathin gate oxides used in metal–oxide semiconductor (MOS) transistors. A current starts to flow even at an OFF state, which is caused by quantum tunneling of electrons or holes through the thin potential wells. Today's dominant ULSI (ultralarge-scale integration) technology for semiconductor structuring is the "top-down" process, which is based on a combination of photolithography, thin-film deposition, and etching steps. In general, the smallest features produced using projection lithography are roughly equal to the wavelength of the exposure source, for example, 248 nm if using a KrF excimer laser. Structures below the conventional Rayleigh diffraction limit can be designed with some sophisticated resolution-enhancing techniques with reasonable high controllability and repeatability. The consensus candidate for the next photolithography generation uses the 193-nm line of an ArF laser. For structures between 100 and 30 nm, electron-beam (e-beam) lithography is commercially available. Structuring below 30 nm, however, goes even beyond the reach of e-beam lithography to a certain degree. Further minimization of semiconductor devices requires higher-resolution processes, which will then involve high production costs for future production lines and sophisticated equipment such as extreme ultraviolet lithography. Such technologies are more and more exhaustive from points of production cost, electrical power consumption, and limitations of fundamental physics.

The above considerations necessitate a search for new technological concepts and/or materials; this search is now a central theme of discussion and research. The "bottom-up" approach is thought to be a potential alternative. The idea is to build-up nanosized structures and devices by using nanoscale building blocks to initiate growth directly at desired positions and with designed dimensions and properties. In contrast to the lithographic and etching techniques used in the top-down methodology, the bottom-up approach involves the direct growth of one-dimensional nanostructures onto a substrate. Figure 1 demonstrates examples for the two strategies. The SiO_2 pillar structure in Figure 1a was designed by e-beam lithography and ion-beam etching, whereas the Si nanowires (NWs) in Figure 1b are epitaxially grown on the substrate by molecular beam epitaxy (MBE). Based on the bottom-up principle, the synthesis of nanowires of common and technologically relevant semiconductor materials such as Si, GaAs, InP, and ZnO has become a focus in current interdisciplinary materials science research.

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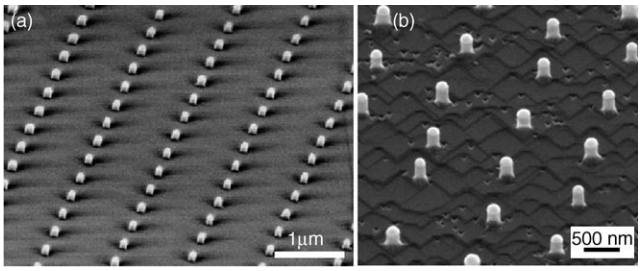

Figure 1. Nanopatterned periodic structures. a) The "top-down" approach: SiO_2 pillars by e-beam lithography and etching; b) the "bottom-up" approach: Si pillars grown by molecular beam epitaxy directed by an array of Au nanodots.

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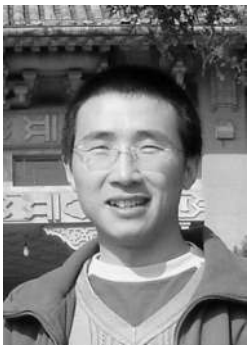

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In this Review, we will look at the growth of semiconductor nanowires and describe major trends in research and technology.

The growth of crystals can easily be observed, for example, as in the case of precipitation out of a supersaturated solution by putting a thread into a liquid solution at the starting point of the crystal growth. The material tends to precipitate at solid–liquid surfaces upon supersaturation, and such precipitates might have the geometrical form of needles. Different ways for locally activating a one-dimensional growth mode have been investigated, for example, using local inhomogeneities on the surfaces of substrates. In the 1930s, the formation of periodic structures on the micrometer scale was observed on crystal surfaces. These formations were intensively studied in the following decades both experimentally and theoretically to understand more deeply the ordering of such complex structures and their growth principles.

Figure 2 demonstrates examples of nanostructures and nanowires based on ZnO, which are produced by thermal evaporation and oxidation under various conditions. Some of them remind us from a morphological viewpoint of macroscopic whiskers that grow naturally in different environments, as already described 30 years ago.[2] The structures in Figure 2, however, are artificially grown and are 100–1000 times smaller. The synthesis of such anisotropic crystals can be realized if the thermodynamic and structural parameters of freedom are restricted during the growth. For example, for the ZnO nanostructures shown in Figure 2, only a small deviation of the growth conditions or a variation of the substrate morphology is needed. However, the aim of a future nanotechnology should be the growth of semiconductor NWs with defined length and diameters, in a periodic arrangement, and at a defined position of the substrate. This means that the process of complete "self-organization" has to be influenced and controlled. This might be possible by nanostructuring the substrate surface. Some of the methods might involve processes formerly developed for the microelectronics industry.

Development of the respective methods for design and growth of NWs has been reported by numerous research groups.[3] For directly grown semiconductor NWs, diameters from tens down to a few nanometers, and lengths between several-hundred nanometers and many micrometers are preferred depending on need, with respect to technology and physics. Some typical growth processes are summarized in Section 2. In particular, to fulfill the complex requirements and demands of a future nanotechnology, the challenges lie not only in growth itself but also in the control of position, dimensions, and large-range ordering of the NWs. In Section 3, we will review the different positioning approaches and discuss their respective advantages and disadvantages.

There are several issues where the fabrication of NW-based semiconductor devices are concerned. For example, concepts for electrically and selectively contacting the NWs have to be developed. Doping of the NWs may be needed to increase the carrier concentration or conveniently generate p–n junctions. Also, analogous to superlattice films in optoelectronic applications, the synthesis of NWs with het-

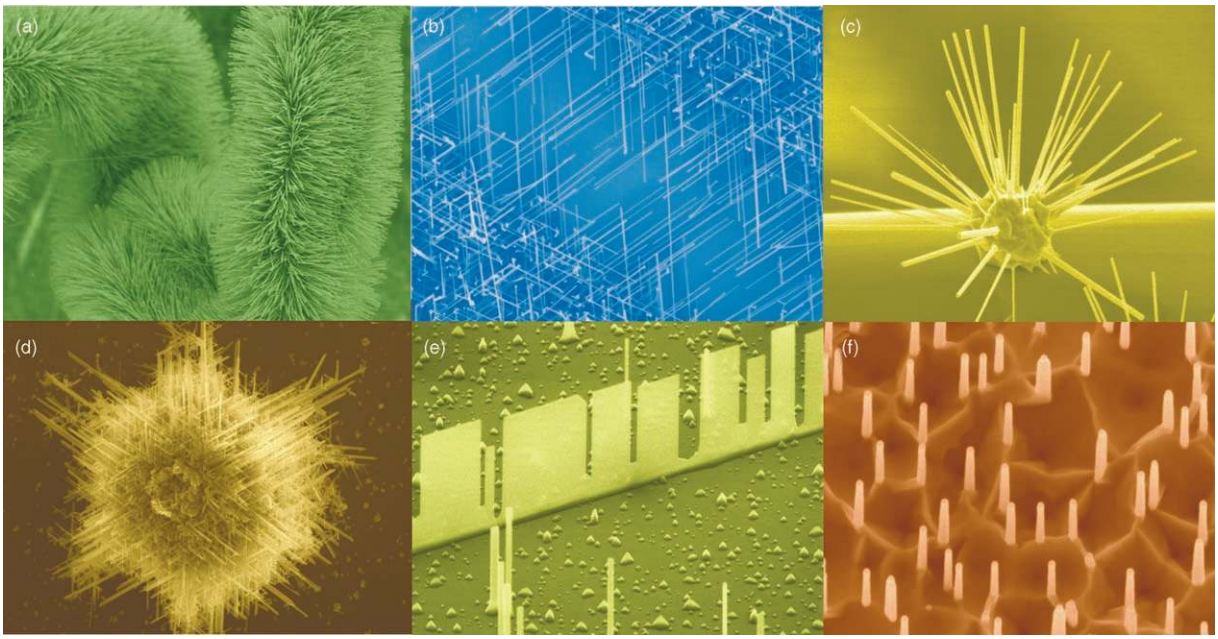

Figure 2. A group of nanostructures based on ZnO grown via self-organization: a) Cluster of nanowires growing like brushes around a microwire; b) nanowires oriented with threefold symmetry; c) nanorods growing radially on the surface of a particle; d) dendrites extending from the side faces of a polyhedral Zn microcrystal; e) nanofence along a GaN surface crack; f) nanorods extending from peaks of interconnected ZnO pyramids.

erostructures is also desired in many cases. Furthermore, the possible role played by the quantum effect should be considered. Such issues related to NW-based device fabrication are discussed in Section 4.

2. The Growth of Nanowires

2.1. The Vapor–Liquid–Solid (VLS) Process

The one-dimensional growth of NWs was demonstrated as early as the 1960s by Wagner et al.[4] At that time, the sizes of such structures were in the range of micrometers and the structures were denoted as "whiskers". A corresponding growth theory was then developed on the basis of the so-called "vapor–liquid–solid" (VLS) mechanism. The VLS process can be divided into two main steps, as schematically illustrated in Figure 3a and b: 1) the formation of a small liquid droplet, and 2) the alloying, nucleation, and growth of the NW.

Growth is started on a clean, defect-free surface of a substrate; in many cases semiconductor wafers are used, however, other materials such as sapphire or glasses have also been applied. First, small metal clusters (diameter below 100 nm) are deposited on the surface to initiate the NW growth. Different techniques, such as a number of self-organization methods for arranging the metal particles have been successfully developed, and will be reviewed below. The as-prepared substrates are placed in a reaction tube or chamber, heated until the clusters melt and form liquid droplets; this is frequently achieved by dissolving the semiconductor material to form an alloy with a reduced melting temperature as compared to the pure metal used. A suitable temperature in the range of 300–1100 °C is chosen according to the binary phase diagram between the metal and the target material. For epitaxial growth of NWs, direct contact of the droplet to the crystalline substrate must be assured. In a second step, a gas containing the growth material flows through the reaction tube. As the surface of the liquid droplet has a much larger sticking coefficient than the solid sub-

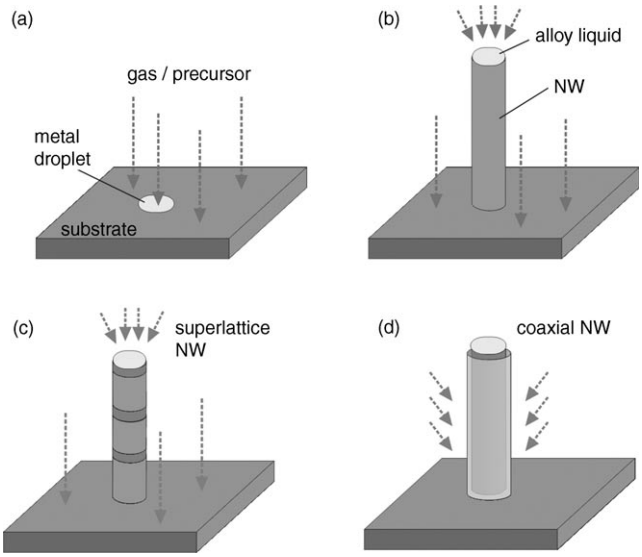

Figure 3. NWs of different structures based on the "bottom-up" growth mode: a) Exposure of a metal-droplet-coated substrate to reactant precursors; b) a monophase NW grown outwards, with the metal droplet acting as catalyst; c) a superlattice NW grown by consecutively alternating the reactant precursors; d) a coaxial NW formed by conformal coating of the preformed nanowire in (b) with a different material.

strate, the precursor atoms prefer to deposit on the surface of the liquid and forms an alloy. Continued incorporation of precursor atoms into the liquid droplet leads to an supersaturation of the semiconductor component. As a consequence, crystal growth occurs at the solid–liquid interface by precipitation and NW growth commences. The NW diameter is determined by the size of the droplet. The growth rate, however, depends much on the supersaturation, which can be influenced by the concentration of precursor vapor and the substrate temperature. The droplet in most cases remains at the tip of the NW in the course of the subsequent growth, as shown in Figure 3. A direct observation of the VLS growth of Ge nanowires was reported by Wu and Yang,[5] who identified the various growth stages in correlation to the Au–Ge binary phase diagram. More recently, similar in situ observation of VLS growth of Si NWs by using ultrahigh-vacuum transmission electron microscopy (UHV TEM) was reported by Ross et al.[6]

In 1992, Hitachi applied the VLS mechanism using gold droplets as catalysts for the growth of III–V NWs, for example, GaAs and InGaAs.[7] By that time, the doping of wires had already been demonstrated, which proved the general possibility for the formation of p–n junctions within the wires and, hence, for NW-based light-emitting diodes (LEDs). After these pioneering experiments, sparse progress was reported for several years until the Lieber group[8] at Harvard University reported new activities on the growth of Si NWs based on the Si–Au eutectic. The Si NWs were grown by chemical vapor deposition (CVD) and were "harvested" by cutting material from the substrate and then bringing them into suspension. By using Langmuir–Blodgett techniques, the individual NWs were assembled parallel to the surface of a handling substrate, which enabled the Lieber group to study basic physical properties of Si NWs and first demonstrate devices such as diodes and biosensors. The Yang group[9] investigated the formation of micropatterned NWs of ZnO by prepatterning catalytic Au. The group showed for the first time the lasing effect of ZnO NWs,[9] which sparked extensive interest in the fabrication of well-aligned and highly ordered ZnO NWs or rods. Recently, a large-scale arrangement of spatially separated ZnO NWs in a hexagonal pattern was demonstrated.[10] In addition, Samuelson concentrated on the VLS epitaxial growth of III–V NWs and NW heterostructures and the study of their application as nanoelectronic devices.[11]

Table 1 gives a brief overview of the different semiconductor/metal combinations and the growth methods for NWs. As can be seen, gold is the most frequently used metal for the VLS process. Nevertheless, the possible influence of gold incorporated in the semiconductor on the electric properties of NWs is still under discussion. For example, gold incorporation is known to result in deep-level defects near the mid gap of Si, which drastically reduces the minority carrier lifetime and generally should be avoided in the context of active devices. Also, it has been shown that gold can wet or diffuse on the surface of growing Si NWs in a UHV environment.[12,13]

In the case of heterostructural NWs (see Figure 3c and d), one or more layers of a second semiconductor compound material is added horizontally or radially to the first one by changing the type of precursor used. For bulk or thin-film devices, one of the main obstacles in combining dissimilar materials is their different lattice constants. For example, a lattice misfit of 4% in Si/Ge heterostructures makes a defect-free growth of extended layers difficult beyond a so-called "critical thickness" after which typically misfit dislocations are introduced in the layer, which generally degrades the electronic and optical materials.[28] For NW systems, the critical thickness is replaced by a "critical radius" below which growth free of misfit dislocations can be accomplished.[29] Below this radius, NWs of poorly lattice-constant-matched semiconductors without misfit dislocations can be formed. Examples of progress in this area are NWs involving superlattices of Si/SiGe[27] and of InP/InAs.[30] This special feature also allows the growth of epitaxial nanowires on substrates with a high misfit without the introduction of misfit dislocations.

A further important issue is the realization of special growth directions in epitaxial NWs. The aim here depends very much on the substrate–material combination, its possible crystallographic orientations, the growth process, and the desired applications. As an example, in the case of silicon, current semiconductor industry favors the <100> wafer orientation due to its associated superior structural

Table 1. Different semiconductor/metal combinations and growth methods for nanowires.

NW material	Source	Metal catalyst	Growth process[a]	Ref.
Si	$SiCl_4$	Au	CVD	[14,15]
Si	$SiCl_4$	Au, Ag, Cu, Pt	CVD	[4]
Si, Ge	SiH_4, GeH_4	Au	CVD	[16]
Si	SiH_4	Au	CVD	[17]
Si, Ge		Fe, Si/Fe, Ge/Fe	PLD	[8]
Si	Si_2H_6	Au	CBE	[18]
GaAs	GaAs/Au	Au	PLD	[19]
InP	InP/Au	Au	PLD	[19]
CdSe	CdSe/Au	Au	PLD	[19]
Si	Si	Ga	microwave plasma	[20]
GaAs	Et_3Ga, Bu_3As	Au	CBE	[21]
ZnO	ZnO, C	Au	evaporation	[9]
Si	Si	Au	MBE	[12]
Si	SiO	Au	evaporation	[22]
Si	silyl radicals	Ga	microwave plasma etching	[23]
Si	SiH_4 or SiH_2Cl_2	Ti	CVD	[24]
GaAs/GaP	GaAs/GaP	Au	PLD	[25]
GaAs/InAs	Me_3Ga, Bu_3As, Me_3In	Au	CBE	[26]
Si/SiGe	$SiCl_4$	Au	Si: CVD; Ge: PLD	[27]

[a] PLD: pulsed laser deposition; CBE: chemical beam epitaxy.

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and processing behavior and its electronic properties. However, VLS growth of Si NWs has until now been mainly successful in the <111> and <110> directions. In addition, there appears to be a diameter dependence on the growth direction.[31,32] The epitaxial growth of Si NWs using a CVD system results in a preferred <111> growth direction for wire diameters larger than 20 nm and a <110> orientation for diameters smaller than 20 nm. This behavior holds for epitaxial and nonepitaxial growth.[31,32] This can be mainly understood in terms of the influence of surface and interface energies of the respective material combinations in VLS growth. Another nice example is given by Kuykendall et al.,[33] who reported GaN nanowires with two types of growth orientations, namely $[1\bar{1}00]$ and [0001]. Substrates with different crystallographic orientations but having good lattice matching to GaN were chosen to induce the NW growth in specific orientations. The driving force behind this was an interface epitaxy at the nucleation stage of the VLS process.[33]

2.2. The Vapor–Solid (VS) Process

NWs can also be grown without extra metal catalysts by thermally evaporating a suitable source material near its melting point and then depositing at cooler temperatures.[34] Such a self-organization process, which does not involve liquid droplets as the catalyst, is referred to as a "vapor–solid" (VS) mechanism. In many cases, the growth mechanism works in an analogous way to the VLS process, differing in that here one component of the gaseous atoms might play the role of the catalyst itself.[35] Common examples are the formation of ZnO and Ga_2O_3 NWs. Either the precursor gas is decomposed due to a high reaction temperature or the pure metal (Zn and Ga) powder is evaporated under a suitable flow gas atmosphere.[36,37] Zn and Ga are characterized by low melting points and sublimation temperatures, which are comparable to the temperatures in the reaction chamber. Therefore, a segregate at the surface of the substrate, especially at places with inhomogeneties or defects, or at the cooler parts of the tube walls, is very probable. In the case of ZnO when oxygen is added to the reaction chamber, the liquid droplets solidify quickly by oxidation and the formation of ZnO wires can eventually be observed. A similar "decoration" of surface defects has been reported for GaN NWs formed on Si substrates. In the VS growth mode, control of the NW diameter is accomplished mainly by changing the evaporation and collection temperatures, as well as the vapor pressure. While fabrication of various hierarchical semiconductor nanostructures through the VS growth mode has been reported in the literature,[34,38] no tight control of the spatial arrangement has been achieved so far.

2.3. Electrochemical Deposition

In addition to the physical vapor-growth modes described above, NWs may also be grown by electrochemical deposition methods in combination with templates such as porous anodic aluminum oxide (AAO), nano-channel glass, and porous polymer films self-organized from diblock copolymers. The template is attached to the cathode, which is subsequently brought into contact with the deposition solution. The anode is placed in the deposition solution parallel to the cathode. When an electric field is applied, cations diffuse towards and reduce at the cathode, resulting in the growth of nanowires inside the pores of the template. After pore filling, free-standing nanowires can be obtained by dissolution of the template membrane. The length of the pores, which can be tuned by the etching process, determines then the length of the NWs. The most widely used templates for electrochemical deposition of NWs is AAO, which has been used for the fabrication of a wide range of NW materials including mainly metals, conductive polymers, and metal oxide materials,[39-41] as well as multisegmented NWs.[42] For semiconductors, the electrochemical deposition technique was used in 1996 for fabricating arrays of CdS NWs with lengths up to 1 μm and diameters as small as 9 nm.[43] More recently, Xu et al.[44,45] reported a group of II–IV semiconductor NW arrays (CdS, CdSe, and CdTe) by dc electrochemical deposition in porous AAO.

As a further step, the pores in the templates/membranes can be regularly arranged and have a cylindrical shape of a constant diameter. This is achieved by imprinting the aluminum surface prior to the anodization process with a lithographically prefabricated stamp to generate specific arrangements of pores, as will be discussed below.[46] Consequently, the resulting NWs are characterized by a narrow size distribution.[47]

Self-organization of metal and semiconductor NWs can also occur by electrochemical step-edge decoration of highly-oriented pyrolytic graphite surfaces, as demonstrated by the Penner group.[48-50] This represents a facile large-scale approach to fabricate supported NWs. When combined with modern nanolithography techniques,[51] this method can be potentially extended to horizontally aligned NWs of various shapes. However, while the material produced by this technique is limited mainly to metals, a second chemical reaction of the metal NWs is needed in order to transform them into semiconductors.[52]

The key issue for semiconductor NWs fabricated by electrochemical deposition is the crystalline quality. In most cases the NWs are not epitaxially grown and hence are either amorphous or polycrystalline in structure. They consist of small crystals with an abundance of defects, which might limit their technical application, especially in optics.

2.4. Solution Growth

The synthesis of nanocrystals by solution methods is well known for the II–VI materials.[53] The ability to systematically manipulate the shapes of such inorganic nanocrystals is an important goal in materials chemistry today. The formation of CdSe nanorods with aspect ratios of 30 were reported by, for example, Manna et al.,[54] who also investigated influential factors in shape control. In recent years,

there have been an increasing number of reports on the solution growth of NWs. Holmes et al.[55] used a supercritical fluid solution-phase approach to the growth of Si NWs, including a diameter control by using dodecanethiol-capped Au nanocrystals. In a similar way, Hanrath and Korgel[56] grew Ge NWs using alkanethiol-protected Au nanocrystals as seeds. The growth of ZnO NWs onto various substrates using thermal decomposition of methylamine and zinc nitrate in aqueous solution were reported by several groups.[57–60] In particular, a multistep, seeded-growth technique developed by the Liu and co-workers[61] allows control of the sequential nucleation and growth, leading to complex nanostructures composed of hierarchical nanorods. Overall, solution methods provide little control over the area density and the NWs have smaller aspect ratios than those grown by vapor-phase routes. Even worse, the NWs display poor vertical alignment although they exhibit certain texture. In case of ZnO, the growth and alignment direction is mainly along the *c* axis, which is detrimental to the UV lasing performance of ZnO NW arrays. The main advantage of such solution-based methods might be the possibility to create NW arrays at low temperatures on large scales at low cost, and on various (even flexible) substrates.[59]

3. Controlling Position, Arrangement, and Size of Catalytic Nuclei for Patterned Nanowire Growth

The patterning of semiconductor and other surfaces in a periodic fashion is of great interest for industrial applications. The term "nanopatterning" refers to approaches that provide periodic arrangements with feature sizes and lattice constants below 100 nm. The technological interest in the ongoing search for new nanopatterning techniques is based on the desire for inexpensive methods to pattern areas on the square-centimeter scale, and beyond. These methods should also be easier to realize than conventional e-beam lithography. Most of the methods are still at the laboratory stage, however, the possibility of parallel sequenced writing based on such nanopatterning methods has already been predicted. The realization of patterned metal arrays as catalysts for the growth of semiconductor NWs is a new application of the nanopatterning techniques. In this respect, the metal-catalyst arrays function as a template for the subsequent growth of NWs via the VLS model, so that the NWs would have the same pattern as the metal dots and the diameters of the nanowires are correlated to the size of the catalyst dots. Therefore, when position control of spatially separated NWs is desired, nanopatterning techniques become essential. In the following section, we will review some typical approaches that have been demonstrated, or are potentially applicable, for position- and size-control of semiconductor NWs.

Gold-dot arrays are preferred for the positioning of NWs, but other metals have also been tested. Table 1 provides an overview for the material combinations and processes used. As high temperatures in the range of 500–1000 °C are usually needed for the growth of semiconductor NWs, the problem of high mobility and diffusion of the metals, which can destroy the predefined catalyst pattern, has to be solved for the controlled growth of NW arrays. A number of patterning and templating methods can be applied for the controlled preparation of metal dots or metal-dot arrays on a substrate surface, including photo- or e-beam lithography, manipulation of single gold nanodots, arrangement of Au nanocrystals from suspensions, nanosphere lithography, gold deposition masks based on porous alumina templates, nanoimprint lithography, block copolymers for nanolithography, as well as other catalyst-positioning approaches. All of these above methods are distinguished by the effort required and their ability to pattern over a large area, as discussed below.

3.1. Photolithography or e-Beam Lithography

Greyson et al.[62] used a phase-shift photolithography procedure for the patterned growth of ZnO NWs. Here, masks containing lines with variable spacing were used twice, with rotated orientations, for exposures of positive-tone photoresist. The resulting pattern was transferred by isotropic wet etching into a rather thick gold film, resulting in ordered arrays of Au pads (see Figure 4a). The advantage with this technique is that the gold pads can be patterned on a large (square inch) scale with variable symmetry (square, hexagonal, and rectangular) and spacing. However, the grown NWs demonstrated in their work are not straight or uniformly oriented. Several wires (up to 20) with diameters of 10–15 nm grow from one defined Au site (see Figure 4b). The behavior is caused by the large size (50–200 nm) and thickness (15–20 nm) of the Au pads used, as well as the use of *a*-plane sapphire as the substrate.

As a conventional structuring tool in the sub-100 nm range, e-beam lithography (EBL) has also been applied to obtain Au nanodot arrays for NW growth. For example, Ng et al.[63] grew nanopatterned ZnO NWs on 6H-SiC substrates (see Figure 5a) through vapor transport and deposition. Under optimized growth conditions, a single long wire was obtained at each gold site protruding from a group of short rods. Mårtensson et al.[64] fabricated InP NW arrays on InP(111)B substrates by combining EBL catalyst nanopatterning and chemical beam epitaxy (CBE, see Figure 5b). Applying the same technique, Jensen et al.[65] fabricated well-ordered InAs nanowires on an InAs (111)B surface (see Figure 5c). The advantage of EBL is the good control obtained for the separation of wire sites, for example, 2 μm in Figure 5a and 250 nm in Figure 5b, and of the gold nanodisk size (below 100 nm). The major drawbacks are high costs and low throughput due to long beam writing times over mm^2 areas. In addition, the EBL system may not be stable over very long e-beam writing times, which also limits its applications for large-area structuring. Hence, in the case where numerous NW growth experiments are needed, EBL is not a desirable approach.

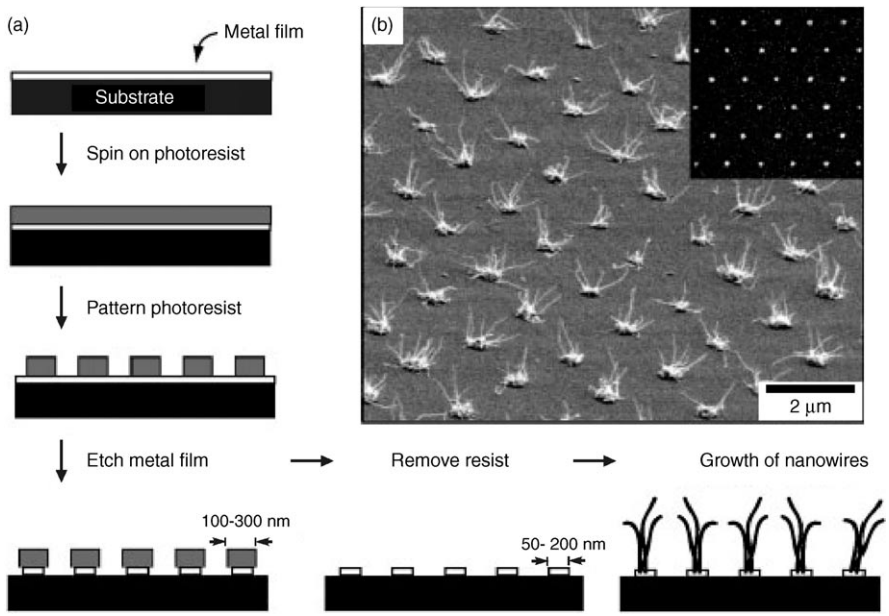

Figure 4. a) Schematic diagram depicting the patterning of catalytic gold dots through phase-shift photolithography and etching, and the growth of NWs. b) An example of the ZnO NWs in a hexagonal array. Inset: the corresponding initial gold pattern (area: $12 \times 12\ \mu m^2$). Reproduced from Ref. [62].

3.2. Manipulation of Single Gold Nanodots

The manipulation of single Au nanodots on the surface of a substrate for the site-specific growth of GaAs NWs was reported by Ohlsson et al.[66] Such single dots were positioned point-by-point on small areas of the substrate. In the case of NW growth, the critical issue of this method is contamination, which should be avoided between the substrate surface and the gold crystals. In particular, any thin film of amorphous oxide that may be present has to be removed because it would hinder epitaxial growth of the NWs. In this respect, the positioning of the gold nanodots has to be carried out under ultrahigh vacuum including an in situ transport of the substrates to the growth chamber. Therefore, this technique can be used for a feasibility study but is not really suitable from the point of view of technology development since the output of nanodevices is very limited by the approach.

3.3. Arrangements of Au Nanocrystals from Suspensions

Suspensions of gold crystallites can be received from a number of suppliers and are characterized by a narrow size distribution. The advantage of using gold suspensions is the size control and the possibility to realize dot diameters below ≈ 50 nm without any need for lithography. Solutions of Au nanocrystals of sizes down to 2 nm are available. Therefore, the NW diameters are also tunable in a precise way while keeping the other growth parameters constant. In addition, the number density of the wires can be varied by using colloids of different concentrations. The important factors for a homogenous coating of a substrate are the surface properties of the substrates (hydrophilic, hydrophobic) and the type of solvent used for the suspension, which should help to prevent the agglomeration of the nanocrystals during drying up. This could be achieved by using an intermediate layer such as poly-L-lysine.[67] In this case, the negatively charged nanoclusters stick to the positively charged poly-L-lysine. However, such an intermediate layer prevents epitaxial growth of the wires. Si NWs obtained

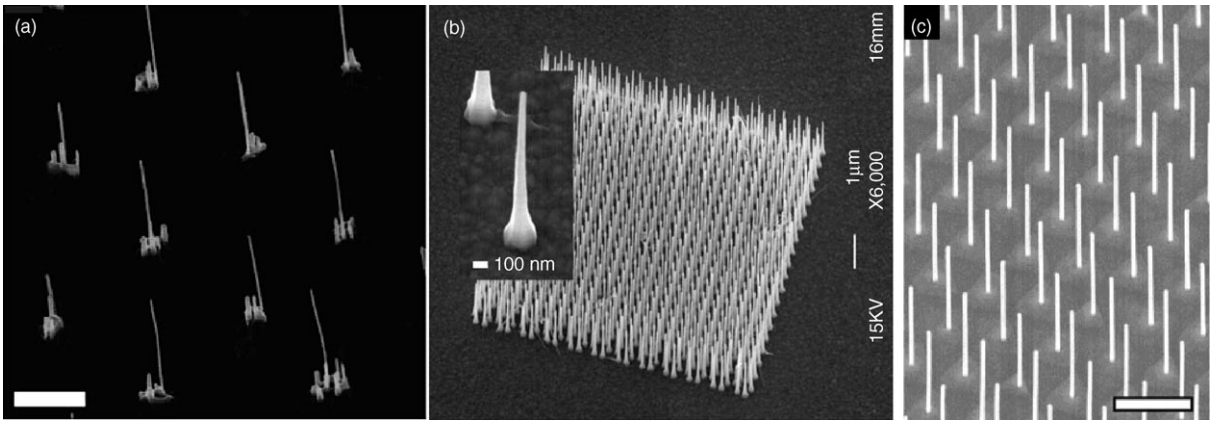

Figure 5. NW arrays growing from Au pads fabricated using e-beam lithography. a) ZnO NWs of 40-nm diameter grown from Au pads (200 nm wide and 1.5–2 nm thick). Reprinted with permission.[63] b) Tapered InP NWs (tip diameter: 50 nm) grown from Au pads (45 nm wide and 17 nm thick). Reprinted with permission.[64] c) InAs NWs of 80-nm diameter and an interwire distance of 750 nm. Reprinted with permission.[65] All scale bars: 1 μm.

with this procedure were like a "nanowool", but had a size similar to the Au nanocrystals used.

Precautions should also be taken to eliminate the amorphous native oxide of the substrate if epitaxial growth is desired. Very recently, Yang and co-workers successfully grew epitaxial Si NWs on Si substrates using gold colloids of different diameters and solution concentrations (see Figure 6).[68] The colloids were immobilized by coating the Si surface with a thin layer of a polyelectrolyte, which provides electrostatic attraction to the Au colloids. The polymer and the native oxide were removed in situ during the growth of the Si NWs by high-temperature annealing and gaseous HCl etching, respectively. Concerning the patterned growth, the main problem of using Au suspensions is its lack of controllable ordering of the Au nanocrystals on the substrate surface. Nevertheless, sub-micrometer patterning can still be realized if an additional lithography process is involved (see below).

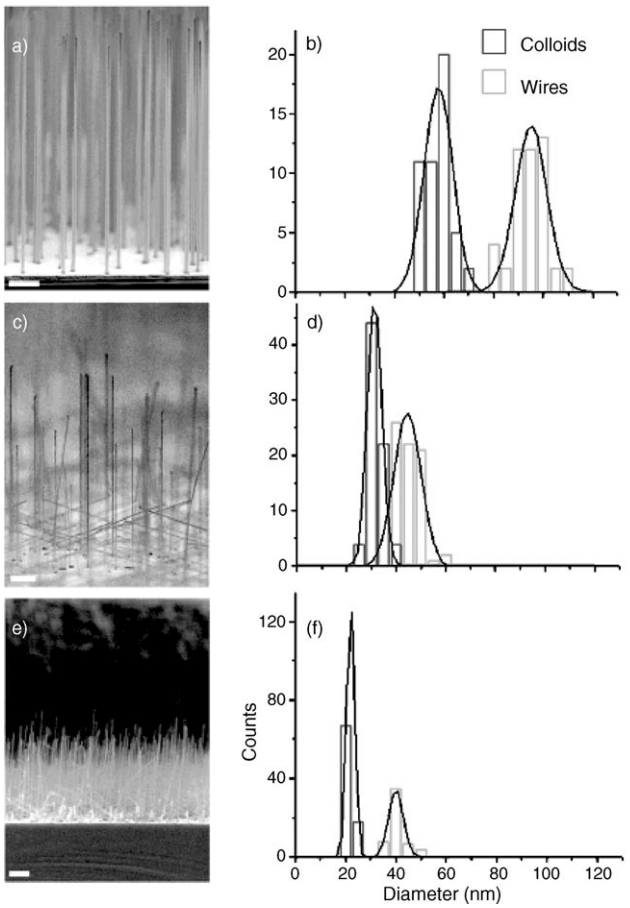

Figure 6. a, c, e) SEM images of Si NWs grown from 50, 30, and 20 nm (nominally) Au colloids, respectively. Scale bars are 1 μm. b, d, f) Size distributions of Au colloids and the resulting Si NW diameters. Reprinted with permission.[68]

3.4. Nanosphere Lithography

The self-organization of sub-micrometer spheres into a monolayer with a hexagonal close-packed structure is the basis of the so-called nanosphere lithography (NSL).[69] Typical materials used for the spheres are silica and polystyrene, which are commercially available with narrow size distributions. The deposition of a single layer of the spheres on a substrate can be used as a lithography shadow mask and template to nanostructure the substrate surface. After the spheres are dissolved (using hydrofluoric acid for SiO_2 spheres and acetone for polystyrene), a honeycomb pattern of triangular metal islands is obtained. The smaller the spheres the shorter the distance of the metal islands and the smaller their dimension. This approach can produce hexagonal arrays of more than $1\,cm^2$ with defect-free single domains of up to $100 \times 100\,\mu m$.[70] Furthermore, other patterns can also be realized if more than one nanosphere layer or a combination of spheres with different sizes are deposited.[71] NSL offers a simple, cost-effective, and high-throughput lithographical approach, and has been widely utilized for the fabrication of a wealth of nanostructure arrays, including semiconductor NWs.

Figure 7a shows ZnO NW arrays on a sapphire surface fabricated by Wang et al. using monolayer NSL.[72] The initial honeycomb pattern of Au islands

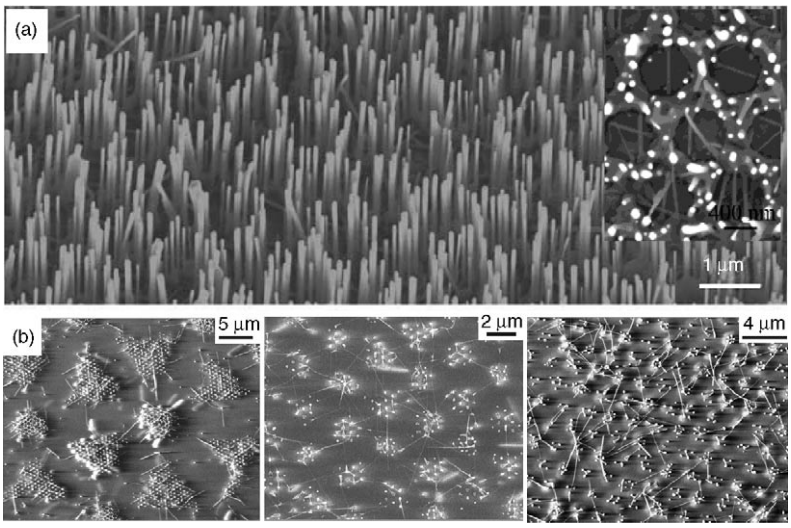

Figure 7. Arrays of ZnO NWs grown from a Au nanodot template fabricated by NSL; a) NW arrays correspond to monolayer NSL. Inset: a top view of the NWs, showing the honeycomb pattern. Reproduced with permission.[72] b) NW arrays grown on a Ni nanodot template arranged in a higher-order pattern by bilayer NSL. The relative angle between the two sphere monolayers are 2, 7, and 10° from left to right. Reproduced with permission.[71]

NANO MICRO small

was preserved after the NW growth. However, as the size of the initial gold islands is much larger than the NW diameters (50–150 nm), a cluster of wire appears at each lattice site, forming an interconnected NW network. Rybczynski et al.[71] demonstrated the growth of ZnO NWs in various superarrays by using bilayers for Ni deposition and adjusting the relative angles between the two polystyrene monolayers (see Figure 7b). In both cases, the used substrates were *a*-plane sapphire. The ZnO NWs grow mainly vertical to the substrate surface while some unwanted inclined NWs also appear. This seems to be an intrinsic problem if using *a*-plane sapphire as the epitaxial substrate, which is related either to an epitaxial growth of ZnO in vicinal crystallographic equivalent orientations, or to the wetting property of ZnO on sapphire at the initial nucleation stage.

In contrast, Fan et al.[73] used GaN epilayers grown on Si as substrates for ZnO nanowire growth. GaN is a suitable substrate for the heteroepitaxial growth of ZnO NWs because of their similar optical bandgap energy (≈3.4 eV), low misfit of the lattice constant (1.9%), and potential for p-GaN/n-ZnO nano-heterojunctions. However, the GaN surface is hydrophobic, which prevents the direct self-assembly of polystyrene spheres. To overcome this problem, a "mask-transfer" technique was used by Fan et al. to transfer the sphere layers from a hydrophilic SiO_2 substrate to the GaN/Si substrates.[73] Figure 8 schematically shows the modified NSL process and examples of such ZnO NWs grown on a GaN epilayer. The hexagonal and triangular lattices of the resulting NW arrays (Figure 8b–e) correspond to monolayer and bilayer NSL, respectively. Advantages of this mask-transfer technique include: 1) the transfer is substrate friendly, and 2) the intersphere holes are narrowed by the metal coating, which results in size reduction (down to 30 nm compared to 100 nm in usual cases) and a good separation of the deposited Au nanodots. This is highly desirable for size-specific individual NW arrays on conductive substrates, as needed for device applications such as sensor or field-emitter arrays.

Application of NSL for the patterned growth of Si nanorods was also reported recently by Fuhrmann et al.[74] (see Figure 9). Here, the normal NSL process was performed on

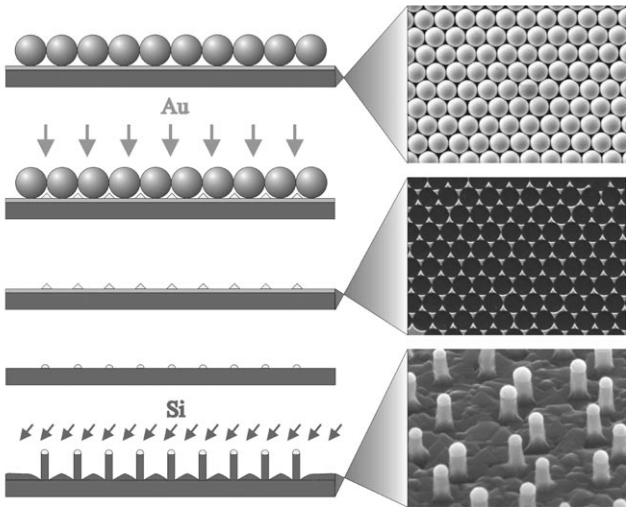

Figure 9. Monolayer NSL-assisted fabrication of Si NW arrays. Left column: Fabrication procedure. Prior to NW growth, the substrate was thermal annealed in an MBE chamber to remove the native oxide and convert the triangular Au islands to hemispheres. Right column: Corresponding SEM images of the sample surface. Reprinted with permission.[74]

Si(111) substrates. The Au-island-decorated substrate was annealed prior to NW growth inside a UHV molecular beam epitaxy (MBE) chamber in order to remove the native oxide layer and to convert the triangular dots into spheres (Figure 9). The Si NWs were then grown by MBE via a diffusion-assisted VLS mechanism.[12] The vertical alignment of the nanorods indicates an epitaxial relationship between the Si(111) substrate and the <111>-elongated rods, and successful removal of the native oxide layer.

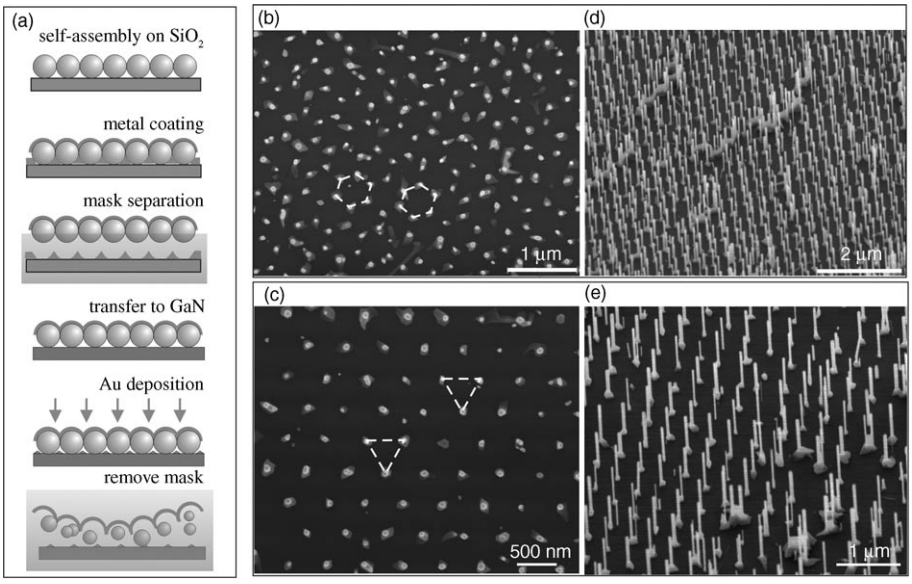

Figure 8. Uniform vertically aligned ZnO NWs on a GaN substrate fabricated via a modified NSL technique. a) Schematics of the fabrication of the catalytic Au nanodot template, which involves transferring the mask from SiO_2 to GaN. b, d) Top and perspective views of the NW array in a honeycomb pattern; c, e) Top and perspective views of the NW array in a hexagonal pattern. Reproduced with permission.[73]

3.5. Gold Deposition Masks based on Porous Alumina

In the 1920s, a process for the electrochemical oxidation of aluminum (anodization) was discovered, with which disordered porous alumina was fabricated with pore diameters in the sub-micrometer range. Since the work by

Masuda and Fukuda in 1995,[75] the systematic use of AAO nanopore arrays for nanotechnology has evolved. These researchers observed that ordered domains of Al_2O_3 pores were established under certain conditions. If the self-organization process is combined with a lithographic prestructuring of the aluminum surface, one can force the pores into monodomain hexagonal order over a cm^2 range, that is, on a macroscopic scale.[46] Free-standing AAO membranes can also be formed and used as metal deposition masks. However, such membranes should be reasonably thick due to stability problems with the brittle porous alumina material and, hence, shadowing effects occur if they are used directly for a masking procedure.

The application of AAO membranes as lithography shadow masks for Au deposition was performed by Wu et al.[76] for MBE growth of GaAs NWs on a GaAs (111)B substrate, and by Chik et al.[77] for the growth of ZnO NWs on a GaN substrate. In both cases, the free-standing thin AAO templates (150–200 nm and 500 nm, respectively) were transferred directly onto the substrates via van de Waals bonding. The obtained NWs exhibited a much narrower diameter distribution than those grown by using a gold film. A careful examination of the SEM images show that the NWs were polydomain ordered and tended to merge due to their small spatial separations.

Such thin AAO membranes are difficult to handle due to their stiffness and transparency, which is a major shortcoming and limits the pattern transfer to small areas. Recently, a new technique was developed to transfer the AAO pore arrays into a metal membrane.[78] This was achieved by evaporating a thin metal film on top of the AAO followed by electrochemical deposition of metal onto the inner walls of the pores. Afterwards, the AAO is chemically dissolved, resulting in a freestanding metal membrane that is mechanically stable and can be used as a macroscopically sized mask for various applications.[78]

Such metal membranes were used for large-scale nanopatterned growth of NWs.[10] The fabrication process is schematically shown in Figure 10a. Gold nanodot arrays on GaN were obtained (see Figure 10b) using the ordered pores of the metal membrane as a mask (see inset in Figure 10b). According to the top view of the sample after NW growth (Figure 10c), ZnO NWs separated by 500 nm and arranged with large-scale hexagonal order were obtained with a single wire at each of the initial Au sites (i.e., one-to-one growth). A change of the NW diameter can be realized by using mask membranes with different pore sizes, which can be controlled by the electrochemical Au-deposition parameters. NWs fabricated in this way are still not perfect in terms of diameter distribution and lattice vacancies. These shortcomings can be avoided by using, for example, pulsed laser deposition (PLD) instead of thermal evaporation and by further optimization of the growth conditions.

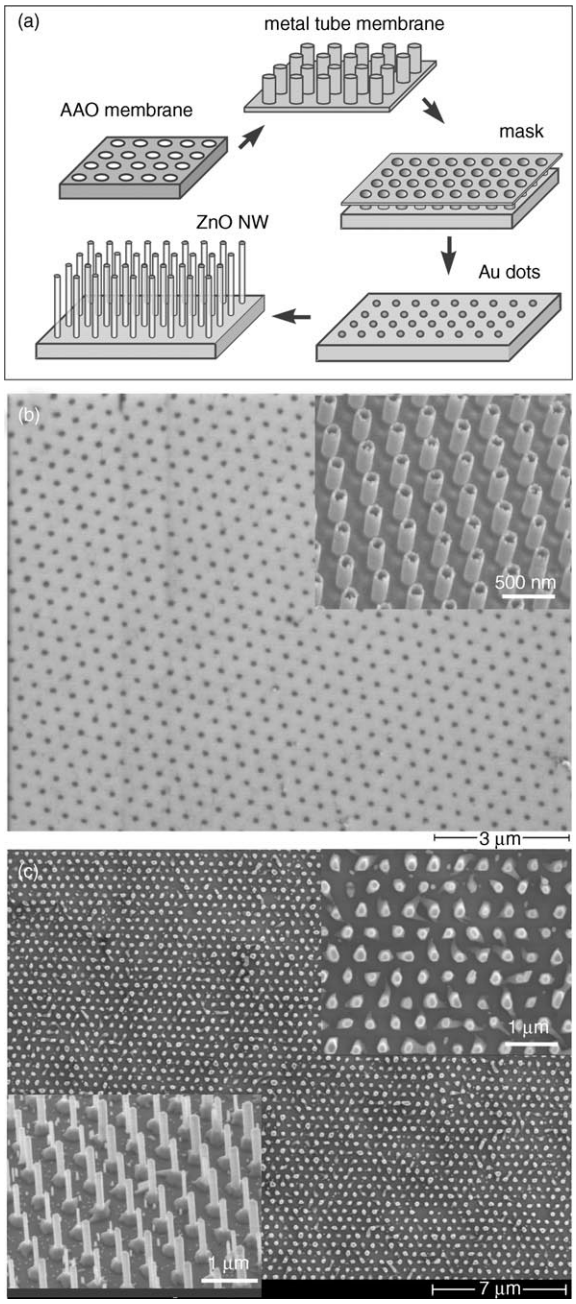

Figure 10. Large-scale monodomain-ordered and vertically aligned ZnO NWs on GaN fabricated using metal nanotube membranes as lithographic masks. a) Schematics of the fabrication process; b) Au nanodot arrays using the tube membrane (inset) as a deposition mask; c) a top view of the ZnO NW array, showing the monodomain ordering. Insets: corresponding top and perspective magnified view of the NWs. Reproduced with permission.[10]

3.6. Nanoimprint Lithography (NIL)

Nanoimprint lithography (NIL) is becoming an important technique both for research and industrial purposes as it is in many respects capable of producing structures comparable to, or even smaller than, those of e-beam lithography but at considerably lower cost and with much higher throughput.[51,79,80] NIL basically consists of two steps: imprint and etching. In the imprint step, a mold/stamp is first replicated from a relief-structured master, and then pressed into a thin resist cast on the final substrate, followed by the removal of the mold. This step transfers the pattern of the

NANO MICRO small

mold into the resist film. The etching step is the pattern transfer from the resist film to the underlying substrate. For nanopatterning of metals, chemical functionalization of the mold and/or the substrate, or a metal-film deposition process is usually an additional requirement. NIL can be combined with other techniques such as nanosphere lithography and colloidal crystals to produce diverse patterns with adjustable pitches and feature sizes,[81,82] which further increases its flexibility and capability.

As an example, Mårtensson et al.[83] created highly ordered and spatially separated metal-catalyst dots for subsequent growth of InP NW arrays (see Figure 11 a). These NW arrays with a tunable number density (by predefining the master pattern) and aspect ratios (by controlling the growth time) are attractive for applications such as nanophotonics. Hochbaum et al.[68] demonstrated the combination of Au colloids with NIL for the patterned growth of Si NWs (see Figure 11 b) on a sub-micrometer scale. Nikoobakht et al.[84] applied NIL to pattern sapphire substrates with narrow (<10 nm) Au lines for the subsequent growth of ultrathin (≈12 nm) ZnO NWs in the plane of the surface. Improved size control of the catalytic Au may allow large-scale production of well-assembled quantum wires. Overall, the NIL technology seems to be one of the most attractive and cost-effective technologies, already having some impact not only on the field of NWs, but also more generally in nanotechnology.

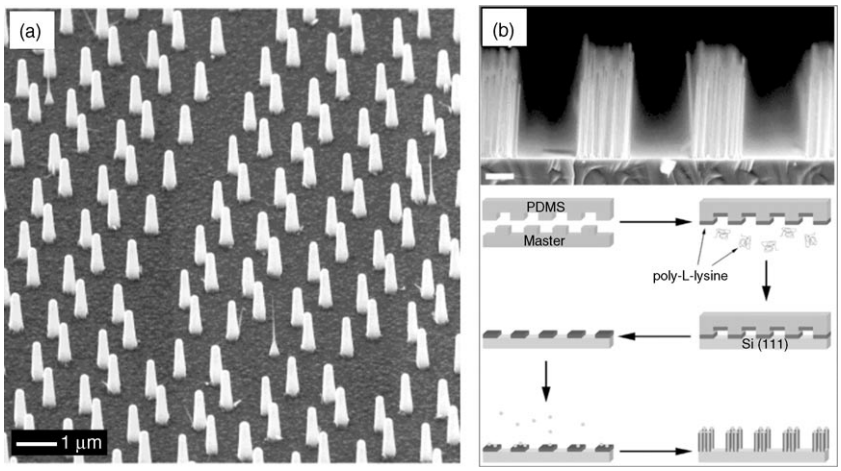

Figure 11. a) NIL-assisted fabrication of InP NW arrays. The dimensions are chosen for a photonic crystal structure operating at wavelengths of 1 μm. Reprinted with permission.[83] b) Patterned growth of Si NWs using Au colloids and NIL. Top: SEM image of the NW array. Scale bar: 1 μm. Bottom: Schematic of NIL process. Reproduced with permission.[68]

3.7. Block Copolymers for Nanolithography

Thin films of diblock copolymers can form large-scale patterns with a periodicity in the nanometer range. The resulting structures can be strongly influenced by the choice of the two different components of the block polymers. The microphase structures generally observed in such systems consist of periodic arrangements of lamellae, cylinders, and spheres. When one polymer material is selectively removed by organic dissolution, a porous film is obtained. The size and periodicity of such pore structures is the result of the length of the block-copolymer chains and is typically in the range of some tens of nanometers. In the work by Park et al.,[85] holes with a diameter of around 20 nm and a separation of 40 nm were produced over a large-scale area (7×10^{10} holes per cm^2). The porous polymer thin film can be used as a lithography mask to create metal nanodot arrays, or as an etching mask to produce high-density cavities on the substrate. A useful application is that, when the polymer film is prepared on a silicon nitride film, the pore structure can be transferred into the nitride layer, or even to the Si substrate underneath. Subsequently, the substrates could be used as promising growth templates for high-density NW arrays if the holes are homogeneously decorated with a metal.

Another way of applying diblock copolymers was demonstrated by Glas et al.[86,87] Here, self-assembly of block-copolymer micelles was combined with e-beam lithography for the deposition of metal nanoparticles. Such a method is capable of generating gold nanodots or lines with a large variety of rather complex patterns. The pattern dimension and geometry is controlled by combining the self-assembly of the block copolymer micelles with the pre-structures formed by e-beam or photolithography. Gold nanodots of 5 and 6 nm in size were arranged in two differently spaced patterns (57 or 73 nm). It can be envisaged that block copolymer micelle nanolithography may offer great potential for growing spatially separated arrays of very-small-sized nanowires.

3.8. Other Catalyst-Positioning Approaches

In addition to the above "conventional" approaches, some other innovative techniques have been demonstrated for the controllable assembly of metal catalysts. Two examples are given here: The first is a growth-in-place VLS approach used by Shan et al.,[88] in which Au stripes confined inside horizontal nanochannels were lithographically fabricated. Subsequently, the vapor precursor flows into the channels until it meets the Au, forcing the NWs to grow along the channels via a VLS mechanism. The size, shape, and position of the NWs were defined by the size, shape, and alignment of the channels. Such horizontal templates

are an integral component of the final devices and provide contacts and interconnects of the NWs without the normal "pick-and-place" or printing steps.

A second example, which can be called "crack lithography", was demonstrated by Adelung et al.[89] The process begins by creating nanoscopic cracks in a brittle thin sacrificial film by inducing mechanical stresses in the film. Once formed, these cracks can be used as templates for horizontal NW formation by depositing material into the cracks. In this way, metal NWs with diameters down to 14 nm can easily be realized. While this approach could in principle be extended to the deposition of horizontal NWs of almost any composition, the challenge is the uniformity, alignment, and crystallinity of the NWs. Nevertheless, the metal NWs created in this way could be used as catalysts for further conventional VLS growth of semiconductor NWs where single-crystalline substrates are used.

4. Patterned Nanowire Arrays by Non-VLS-based Techniques

While most site-defined NW fabrication techniques involve metal-catalyst templates, there are also some interesting and reliable approaches to catalyst-free and non-VLS-based growth of NW arrays. Fukui and co-workers have used a so-called selective-area metalorganic vapor phase epitaxy technique to fabricate vertically aligned III–V NW arrays on selectively masked epitaxial substrates (see Figure 12).[90-92] The process begins with spatially controlled growth of an epitaxial layer through an opening in a SiO_2 mask (which was predeposited by plasma sputtering). NWs were formed by further growth based on the epitaxial layer. The length, diameter, shape, and position of the NWs were controlled by manipulating the growth conditions and mask patterning.[90] More remarkably, epitaxial core–shell GaAs/InGaAs and InP/InAs NW arrays were also realized by the sequential feeding of metalorganic precursors (Figure 12c).[91,92] Further, by dry etching the core material, they also obtained arrays of semiconductor nanotubes that exhibit reasonably good electrical conductivity (Figure 12d).[92]

In catalyst-free aqueous-phase growth modes, the result is usually a film of closely packed NWs covering the whole substrate surface. However, by applying microcontact printing,[61,93] micromolding,[94] or conventional lithography techniques[95] to pattern the substrate surface or a predeposited seed layer, it is also possible to achieve cm^2-scale ordered NWs arrays in dots, lines, and a variety of complex structures, as demonstrated recently. Although the patterns are still on the micrometer scale, the concept can be extended to nanopatterning when interference photolithography or modern soft-lithography techniques are utilized.

5. Towards Devices and Functions

The growth mechanisms used in various NW fabrication processes are still far from being understood in detail, and various nanolithographic approaches are under development to realize a better control of the spatial arrangement of the NWs. Nevertheless, investigation on multifunctional applications of semiconductor NWs have already started. Due to their high anisotropy in structure, such one-dimensional structures are distinguished from their bulk counterparts in various aspects of their properties, as has been demonstrated by theory and numerous experiments. It was shown that NWs might have unique size-dependent mechanical properties,[96,97] an increased luminescence efficiency,[98] a reduced threshold for laser operation,[9] an enhanced electromechanical response,[99] and an enhanced thermoelectric efficiency compared to conventional Peltier elements.[100]

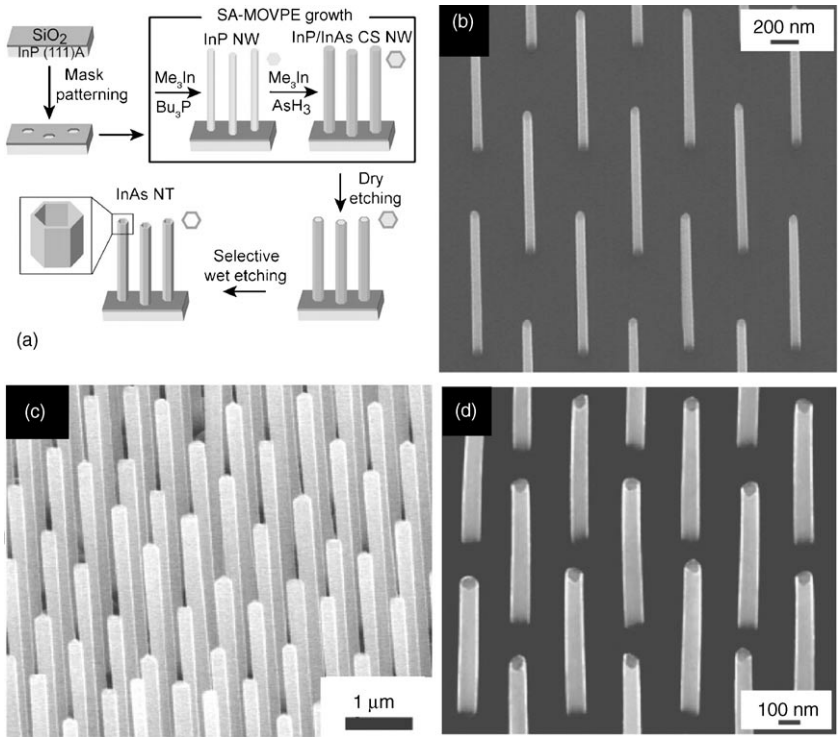

Figure 12. Well-ordered NW arrays by selective-area metalorganic vapor phase epitaxy (SA-MOVPE): a) Schematic of the fabrication technique, which enables the size-defined growth of NWs, core–shell NWs, as well as nanotubes of III–V semiconductors; b) an InP NW array; c) GaAs/AlGaAs core–shell NWs; d) InAs nanotubes after removing the InP core of initial core–shell NWs. Reprinted with permission.[90-92]

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Application of NWs in advanced nanoscale devices will require high reproducibility in the synthesis of highly regular NW arrays directly on the chosen device substrate, as well as new and innovative processes for device integration and electrical contacts. Such processes should retain the structural integrity of the NWs and conserve their properties of interest while being within the constraints of a technology. An example for a NW-based device is the field-effect transistor (FET). In this concept, a current flows through a semiconductor NW and the respective ends work as a source and drain for the electrical carriers. A certain area of the wire, whose length determines the active channel length of the FET, is covered by a suitable insulating material where a gate voltage can be provided. Particularly, epitaxial growth of vertical NWs on a highly doped single-crystal substrate offers advantages over other approaches: For example, the transistor gate can be wrapped around the vertically oriented NW, and the substrate can act as the drain. Such a wrap-around gate allows better electrostatic gate control of the conducting channel and offers the potential to drive a higher current per device area than is possible in a conventional planar architecture.[101] From the viewpoint of technology this configuration seems to be favored over structures in which the NWs extend parallel to the substrate. Realization of such a concept was recently demonstrated by Ng et al.,[102] who reported a vertical surround-gate field-effect transistor (VSG-FET) based on a single ZnO NW (≈30 nm diameter) grown on a SiC substrate (see Figure 13a). More recently, Schmidt et al.[103] reported a similar VSG-FET based on homoepitaxial Si nanowires (≈40 nm diameter; see Figure 13b). Similar results were demonstrated by the Kamins group at Hewlett–Packard.[104] Although the superiority of such VSG-FETs over conventional FETs in ICs has still to be shown experimentally, these demonstrations provide at least a proof of principle for the processing techniques, which certainly paves the way for the industrial use of the epitaxial NW-based vertical FETs.

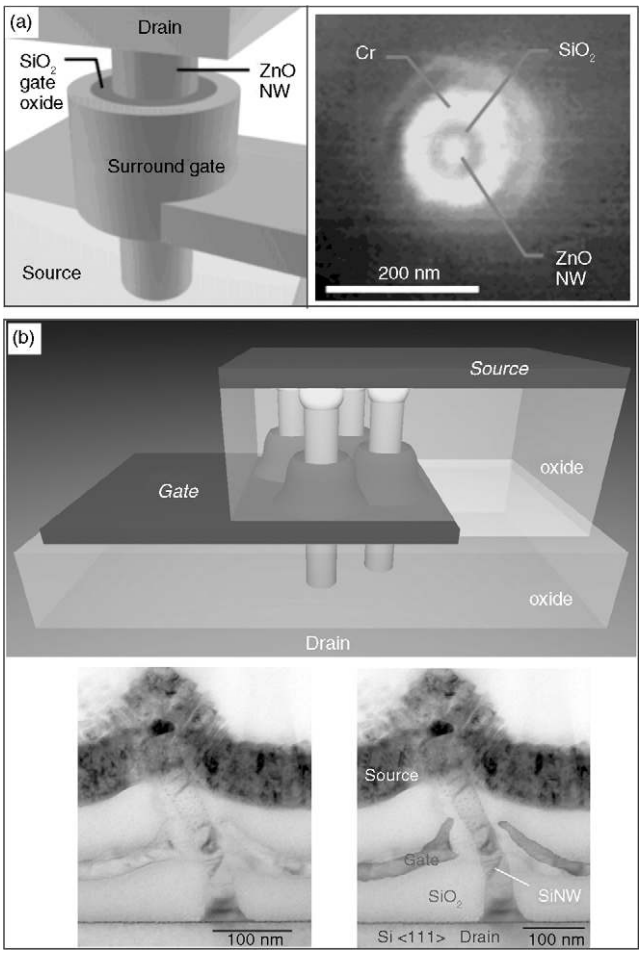

Figure 13. Vertical surround-gate field-effect transistors based on a) ZnO NWs (reproduced with permission[102]) and b) Si NWs (reproduced from Ref. [103]). Three-dimensional schemes of the device configuration are shown along with corresponding electron microscopy images (top-view SEM image in (a) and cross-sectional TEM image in (b)).

Because of the high aspect ratio of NWs, electrons can be easily extracted out from NW tips by an electric field. It has been demonstrated that semiconductor NWs (e.g., GaN, AlN, CdS, ZnO) grown vertically on conductive substrates show strong, low-threshold, and stable field-emission currents.[105] Therefore, analogous to carbon nanotubes, semiconductor NWs also possess applications in field-emission displays and microelectron source instruments. Gangloff et al.[106] demonstrated the production of integrated-gate nanocathodes consisting of a single carbon nanotube or Si NW per gate aperture (see Figure 14). Such gated arrays of NW cathodes can be fabricated easily on a large scale when coupled with current nanoimprint or interference lithography, and can be based on many other semiconductor NWs when combined with advances in the controlled deposition of ordered NW arrays.

There has also been much interest paid to the optical properties of semiconductor NWs, because of their promising prospects as building blocks for nanoscale optoelectronic detectors, light-emitting diodes, lasers, optical waveguides, and nonlinear optical frequency converters. In particular, the integration of light sources with complementary metal–oxide semiconductor (CMOS) devices would be a revolution in information technology. In this concept, the electric signals carrying the information in conventional circuits are converted into optical pulses. Such optical signals, which nowadays are formed by light-emitting diodes or lasers based on III–V materials, can also be initiated by NWs. In a similar concept, NW-based light detectors, as well as light transmitters between adjacent device components, can also be generated. Electroluminescence of n-ZnO NW arrays vertically grown on p-GaN substrate was reported by Park et al.,[107] however, with a peak position that still favors the yellow (560 nm) emission normally assigned to defects.

With respect to lasers, Yang and co-workers have already demonstrated that a ZnO NW can function as a natural optical resonator cavity and gain medium, so that lasing can be observed from vertically aligned NWs when they are grown to a suitable thickness and length.[9,108] Similar lasing effects were also observed from NWs of other wide-bandgap materials including GaN,[109] CdS,[110] and ZnS.[111] For nanoscale optical device applications, heterostructural semicon-

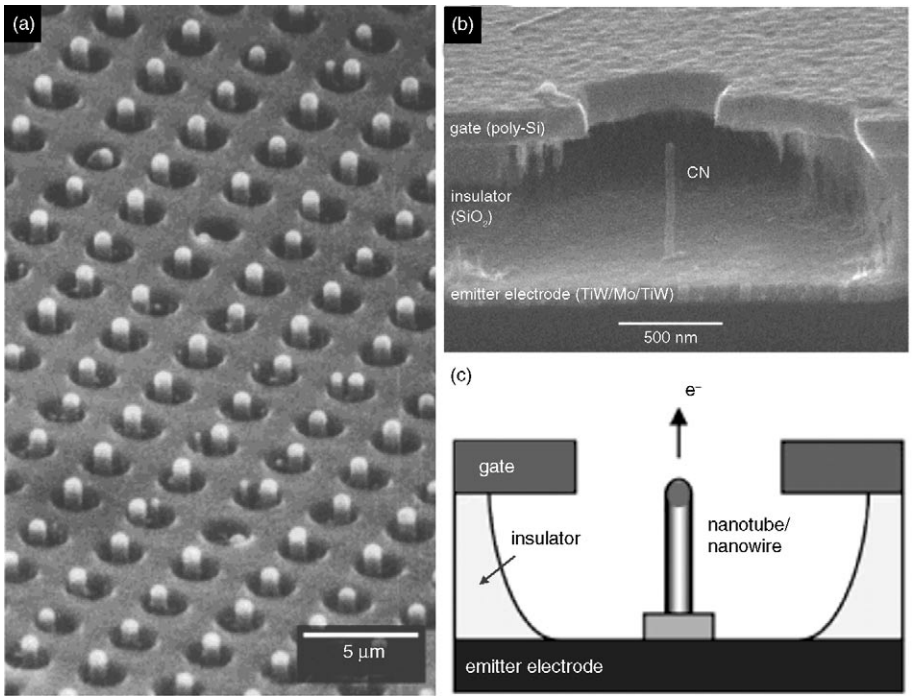

Figure 14. Gated arrays of individual 1D nanostructures for application as emitter arrays. a) An array of integrated gate Si NW cathodes; b) SEM image of an integrated carbon nanotube cathode showing the gate electrode, insulator, and emitter electrode; c) schematics of a single nanowire/nanotube emitter. Reproduced with permission.[106]

ductor NWs with modulated compositions might be superior to NWs of pure composition. Surface states are known to cause some deleterious effects. For example, they can act as recombination centers for minority carriers, thus degrading the performance of optoelectronic devices of NWs.[112] Such negative consequences can be avoided by passivating the nanowire surface immediately after core definition, forming core–shell nanowires. A shell dielectric could be used to form a high-quality optical cavity around a small-core NW acting as the gain medium. More novel material combinations involving, for example, hetero- or homoepitaxial semiconductors (e.g., Si–Ge,[113] ZnO–GaN,[114] p–n GaN[115]), ferroelectric and magnetic materials (e.g., MgO–PZT,[116] MgO–Fe_3O_4[117]) open the door to a wide variety of functionalities in such core–shell NWs.

Semiconductor NWs of sufficiently small diameter (i.e., close to the corresponding exciton Bohr radius) should exhibit quantum-confinement-related effects, which, for example, strongly influence the optical properties. This has already been demonstrated for NWs of III–V semiconductors,[118] ZnO,[119,120] as well as for silicon.[121,122] Silicon is the most important microelectronic material. However, it has poor optical emission properties due to its indirect bandgap transitions. It is expected that Si and Si/Ge nanostructures may have a much higher luminescence efficiency than bulk Si, because the band structure of a NW can be modified in a way that the radiative recombination probability is significantly enhanced. Consequently, new (group IV) optoelectronic devices might be realized. This could allow the combination of electrical and optical functions on the same Si-based chip. It was also reported that quantum effects could reduce the heat conductance, which could be used for new cooling concepts based on NWs.[123] For electric-carrier transport in NWs, phenomena of interest include: 1) the aforementioned quantum confinement, 2) ballistic carrier transport, which corresponds to a high mobility, and 3) tunneling of electrons between NWs and corresponding heterostructures ("Coulomb blockade"). At the moment it is to early to judge in which way these properties might have a use in future technology.

One possible application of NWs lies in the field of biotechnology; different functional concepts are under discussion. NW nanosensors have been suggested for highly sensitive and selective detection of biological and chemical species.[124] This approach might even offer the possibility to detect the selected attachment of single molecules. Although most of the discussed concepts for the use of NWs in the field of human medicine are still speculative, a fast development of applications in various fields is expected within the next decade. There have been a number of national and multinational initiatives for nanotechnology launched during the last couple of years, which should serve to advance these concepts. Parallel to this scientific and technological evolution, one should also keep in mind the potential environmental risks associated with nanowires, although this risk should be minimal for semiconductor nanowires embedded in circuits.

6. Summary and Outlook

With the remarkable progress in research on the synthesis of semiconductor nanowires over recent years, one-dimensional growth with superior control in structure, dimension, and spatial alignment becomes more and more important. In this Review, typical growth approaches for semiconductor NWs were discussed, which fall into two main categories: vapor-phase and wet-chemical approaches. We focused on the vapor–liquid–solid growth mode because it provides a technical opportunity for in situ position, definition, and size control of the nanowires. Nearly all existing technologies, from conventional photolithography to state-of-the-art nanoimprint lithography, have been employed for

NANO MICRO small

the spatial control of the positioning of nanowires. The trend for better control of nanowire growth is accompanied by progress in templating techniques.

Nevertheless, for the nanopatterned growth of semiconductor NWs on a macroscopic scale, an improvement of current techniques is still needed and/or an innovative technology should be developed. Such new techniques should give high processing resolution and efficiency, and allow epitaxial NW growth with good crystallinity. This is highly desirable to future nanomanufacturing and applications, and is in particular an essential step towards in situ integration of well-aligned nanowires into devices with existing technologies, for example, vertical transistors, electron field-emitter arrays, and biosensor arrays.

This Review also covered some concerns and recent demonstrations for using semiconductor NW as electronic and photonic devices. Due to their low dimensionality and semiconducting nature, the NWs may exhibit unique electronic and optical properties relative to bulk semiconductors. In many cases, the detailed mechanisms behind their behavior are not yet understood in detail. Nevertheless, independent of whether these properties are desirable or not, they should be well understood when using semiconductor NWs. There is not doubt that NWs will create countless new opportunities in research and hopefully also in technology.

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