SENSING CIRCUIT DESIGN FOR AN ION MOBILITY SPECTROMETER

by

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A project

submitted in partial fulfillment

of the requirements for the degree of

Master of Science in Electrical Engineering,

Boise State University

July, 2005

The project presented by Surendranath C Eruvuru entitled SENSING CIRCUIT DESIGN FOR AN ION MOBILITY SPECTROMETER is hereby approved:

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ACKNOWLEDGEMENTS

It has been a great honor to do my Masters degree in Electrical Engineering at Boise State University.

First of all, I would like to thank my advisor, Dr. Jake Baker who has given me a quality education, guidance, and motivation. I thank the Environmental Protection Agency (EPA) for funding the sensor project and providing an opportunity to me for research. I also thank the Project Investigator, Dr. Molly Gribb and other team members whose suggestions have helped me complete this project. I would like to thank Dr. William B. Knowlton for his guidance through out my Master's degree and last but not least Dr. Sin Ming Loo for agreeing to be on my committee.

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ABSTRACT

Ion Mobility Spectrometer (IMS), one of the potential scientific instruments that have served major airports and defense systems as a detector for narcotics, military gases, explosives, and pollutants. Some of the essential parts of the IMS are drift tube, ionization region, Tyndall gate, aperture/collector, diffuser gate, drift gas source, sensing circuit, high power supply, microcontroller, wireless transmitter, etc.

A sensing circuit is necessary to amplify and digitize the output signals from the Ion Mobility Spectrometer so that they can be read and interpreted by the microcontroller. The Sensing circuit design was realized using a low-cost, low-bandwidth, low-power consuming high-resolution analog to digital converter. Since the input signal is too low for the circuit to digitize, a preamplifier has been employed. The design is conceived by using a unique technique called Delta Sigma modulation, which is widely used in sensing memory cells and Complimentary Metal Oxide Semiconductor (CMOS) imaging. Delta sigma modulation uses a simple logic of averaging and some basic analog electronics. It’s a very low cost technique that achieves high resolution by shaping the Quantization noise.

The prototype of the sensing circuit was successfully built and assembled on a printed circuit board and was tested using IMS in Washington State University and with the IMS, which was built by Boise State University.

LIST OF ABBREVIATIONS

AC …… Alternate Current

ADC …… Analog to Digital Converter

BSU ……...Boise State University

DC ……..Direct Current

DFF ……. D flip-flop

DSM ……..Delta Sigma Modulation

EPA ……... Environmental Protection Agency

FPGA ….……... Field Programmable Gate Array

HRIMS ...…… High Resolution Ion Mobility Spectrometer

IMS ...……. Ion Mobility Spectrometer

LTCC ...…… Low Temperature Co Fired Ceramics

MOS ……...……. Metal Oxide Semiconductor

NTF ……... Noise Transfer Function

NS ……...…….. Noise Shaping

PCB …… Printed Circuit Board

PSD ……..……... Power Spectral Density

RMS ……... Root Mean Square

RIP …….. Reaction Ion Peak

SPICE …… Simulation Program with Integrated Circuit Emphasis

SNR ……... Signal to Noise Ratio

LIST OF FIGURES

REPORT ORGANIZATION

This project is divided in to seven chapters:

- Chapter one gives an overview of the Sensor Project and a brief description of the concept of Ion Mobility Spectrometry. The assembly of an IMS is also described. Additionally, it identifies the design requirements to be met.
- Chapter two gives an introduction of the sensing circuit needed for the IMS and the concept of delta sigma modulation.
- Chapter three gives an introduction of the design for the preamplifier stage of the Sensing Circuit.
- Chapter four describes the design of the delta sigma modulator circuit used for digitization.
- Chapter five describes noise analysis of the circuit.
- Chapter six describes the implementation of delta sigma modulator and the sensing circuit, the layout of the printed circuit board and the experimental results obtained.
- Chapter seven briefs the conclusions, drawbacks, and future work of the project.
- Appendix
- References

Achievements

- Board level testing has been successfully completed for the preamplifier stage of the sensing circuit for IMS.
- The preamplifier for the IMS has been successfully built and tested with the IMS in Washington State University.
- Delta-Sigma modulator circuit has been developed and tested at board level.
- Both the preamplifier stage and the delta-sigma modulator have been integrated and tested to complete the board level design for the sensing circuit.
- The sensing circuit has been integrated with the FPGA to test the correspondence of the digital output to the analog input from the IMS.
- The sensing circuit has been tested with the IMS in Washington State University and the IMS built by Boise State University.

CHAPTER ONE: INTRODUCTION OF THE IMS

The Multipurpose Sensors project to detect and analyze environmental [subsurface] contaminants was started in July 2002. The goal of this project is to develop sensors that would provide real time data, not only on the quantity but also identification of contaminants like heavy metals and volatile organic compounds underwater. This involves development of solid-state electrochemical sensors for heavy metals, and fabrication of a miniaturized High Resolution Ion Mobility Spectrometer (HRIMS). The whole IMS system consists of sub-systems like IMS, sampling system, high power supply, gate control, sensing circuitry, embedded microcontroller or field programmable gate array (FPGA), temperature and pressure sensors, wireless transmission subsystem, optional GPS Subsystem and a host data acquisition computer with software to accumulate transmitted data from sensors [1]–[7].

The system overview would look as shown in figure 1.1.

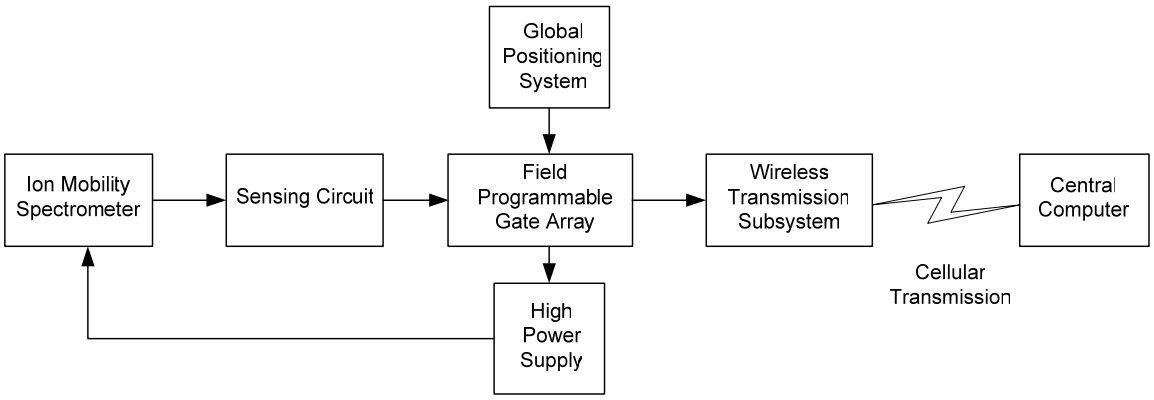


Figure 1.1 Overview of the IMS system

Our group was assigned to design the power supply and sensing circuit for the IMS. The microcontroller turns on the power supply to power up the IMS when a sensing cycle starts. After measured period of sensing is done, the power supply of the IMS is turned off. During this period, the output signals of the IMS represent the contaminants and their concentrations. Since the output signals obtained from IMS are too small (in the range of nano-amperes) to determine the contaminant, a sensing circuit is used to amplify and digitize these signals to levels that can be read by the microcontroller. The microcontroller collects data through the sensing circuit and transmits this data to the data acquisition computer for further processing [1]–[7].

1. Construction and Working of an IMS

Originally, IMS was designed for detection of trace compounds within a gas or gaseous mixture. This particular idea has been extended to find the contaminants and their concentrations in ground water. The basis of the IMS is the drift of ions under the influence of an electric field at ambient pressure. The drift time of the ions across a fixed length in an electric field is measured to determine the mobility. The drift time is calculated from the time of ion injection from the source region to the drift region. Several key features of the IMS being constructed are small size, low weight, low power requirements, and reliable performance [1]–[7].

A miniaturized drift tube has been constructed using 114 (24.6mm) layers of low temperature co-fired ceramics (LTCC). Resistor paste has been applied to each LTCC layer in which a conductor has been printed to connect the resistances on each ceramic

layer. This has been done to maintain uniform electric field in the tube. In Figure 1.2, the construction schematic describes some of the essential parts of the IMS. As we can see in the schematic of IMS, two inlets are provided for the sample and the drift gas on either end of the IMS. The region where the sample enters the tube is called the Ionization region. There are different ways of ionizing the sample molecules but the most common is using an UV (ultra- violet) lamp (typical UV lamp is 10.6eV, 116.9nm Kr $1p_0$-$1s_2$) [1]. There are three different gates placed in between the ceramic layers; Tyndall gate, Aperture/collector, and diffuser. The Tyndall Gate is used to control the flow of ions down the drift tube. It is inserted in between the ceramic layers in the form of two parallel rings with a wire mesh normal to the flow of ions. The Tyndall gate is the separator in between the ionization region and the drift tube region, which is used as a sample inlet to drift tube region. The drift tube region is defined as the region in between the Tyndall gate and Aperture. The ions travel along the drift tube from the sample inlet towards Aperture gate. The third gate is called the Diffuser. The purpose of this gate is to stop all the ions which have already passed through Aperture and heading towards the end of the ceramic tube. In order to accomplish this, the diffuser gate is held at a higher potential than Aperture. All the three gates are connected to electrodes and routed through the ceramic layers for external connection [1] [2].

The process of detecting a chemical contaminant starts with the ionization of sample in the ionization region. This process begins with emission of high-energy electrons (beta particles) from a radioactive source. The molecules of the sample are

ionized when hit by the beta particles and thus the ions are propelled through the drift tube section. The Tyndall gate, which is controlled by the microcontroller, controls the flow of ions into the drift region. The drift region has an arrangement which provides a constant drop of voltage across each ring when a supply voltage is connected across the tube. This arrangement allows the ions to move under the gradient of electric field and the ions attain a velocity according to their mobility. The flow of ions is stopped by raising the field voltage at the diffuser gate above the field voltage in the tube. A steady flow of drift gas is swept through the drift tube to minimize the secondary effect of buildup of impurities that could otherwise react with ions and distort mobility spectra [1]–[4].

Figure 1.2 shows the schematic of the IMS system. The Aperture grid intercepts ions, on their way to ion collector from Tyndall gate. This interception is used for the electrostatic field radiated by the approaching ion cloud so that it no longer induces current flow in the collector. It capacitively decouples the current signal detected at the collector plate from the approaching ions.

At the collector, the reactant ions strike the detector and ion current is recorded as peaks separated by arrival times. These signals have to be sensed, amplified and digitized electronically so that they feed to the microcontroller for transmission to the data acquisition computer. Figure 1.4 shows the conceptual drawing of the IMS in solid works [1]-[4].

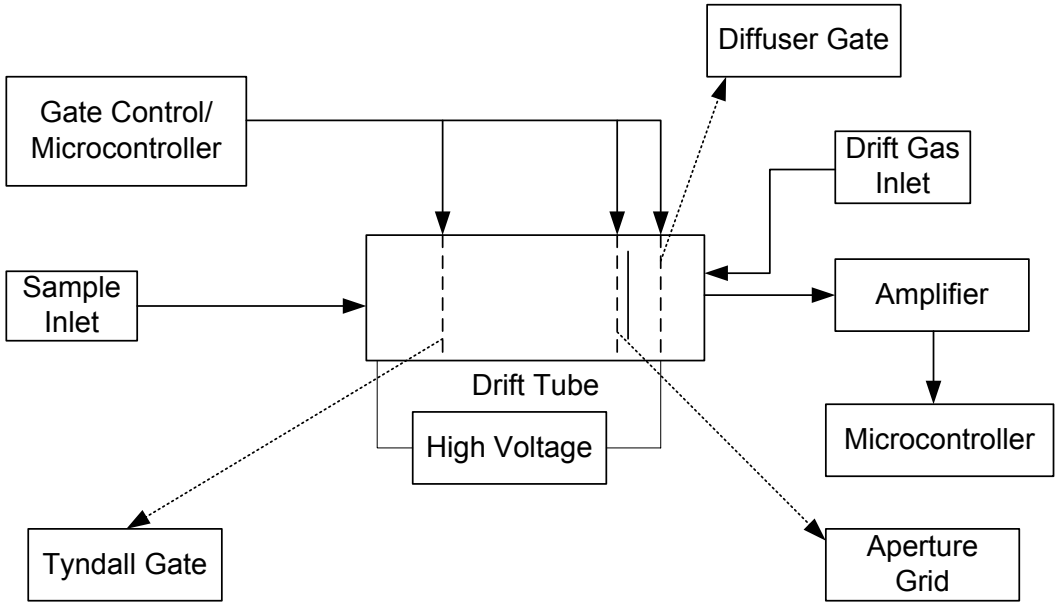


Figure 1.2 Block diagram of IMS

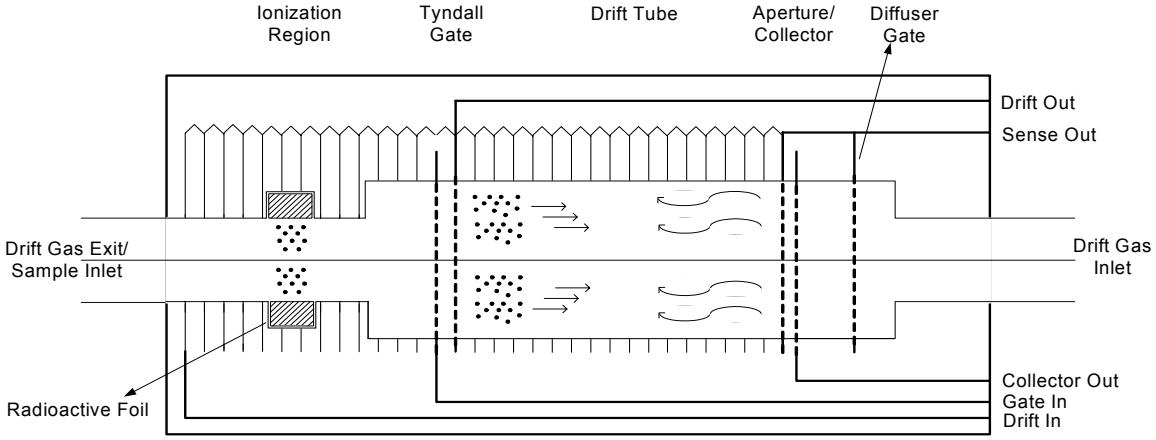


Figure 1.3 Schematic of the IMS [2]

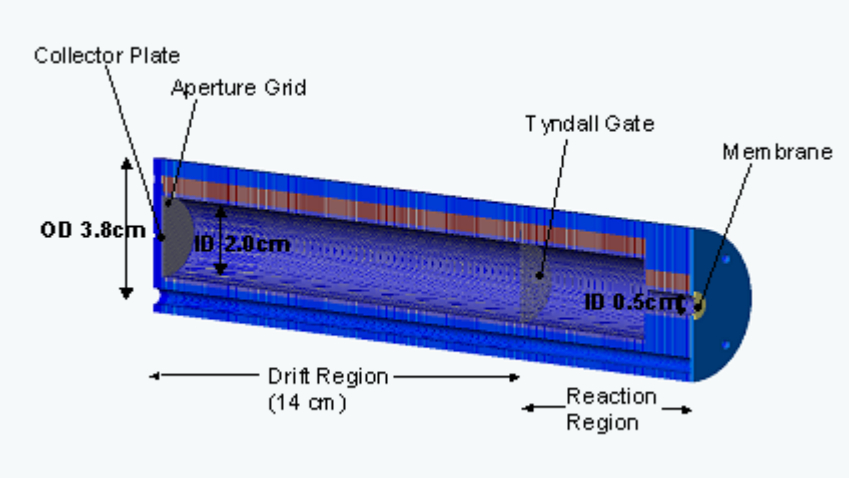


Figure 1.4 Conceptual drawings of an IMS [2]

2. Design Requirements

Prior introduction of the IMS suggests that the noise level of the output signal that is obtained from the faraday plate of the IMS will be high. Since the analog signal level at the faraday plate is too small (in the range of nA), the signal to noise ratio (SNR) will be too low. The purpose of the sensing circuit is to sense the ion current peaks, amplify, and digitize. The complete IMS signal occurs within a 20ms period. The peak spikes in the IMS signal occur within a time period of 0.5-1ms and have an amplitude of about 3-10nA. The sampling rate should be much higher than the frequency of the peaks coming from IMS. This selection of the sampling rate will effect the detection of the peak. So, the sensing circuit should provide an amplified value of the signal for at least every single sample.

The microcontroller in the sensor scheme uses its own VDD (3.3V) as a reference voltage and does not support incoming signals higher than VDD. So the sensing circuit output should be limited to the maximum voltage input of the microcontroller, VDD.

CHAPTER TWO: INTRODUCTION TO THE SENSING CIRCUIT

The collector plate, also called a Faraday plate, at the end of the IMS, collects ions and delivers a time dependent signal corresponding to the mobility of the arriving ions. The output signal peaks correspond to the various compounds in the mixture. The resulting ion mobility spectrum consists of information about different trace compounds present in the sampled gas [1]-[4]. As stated before, the complete IMS signal occurs within a 20ms period. The peak spikes in the IMS signal occur within a time period of 0.5-1 ms and have an amplitude of about 3-10nA (depending on the IMS used). These small amplitudes of current should be amplified for the analog to digital converter (ADC) to convert the information to digital form. Figure 2.1 shows the typical signal that is

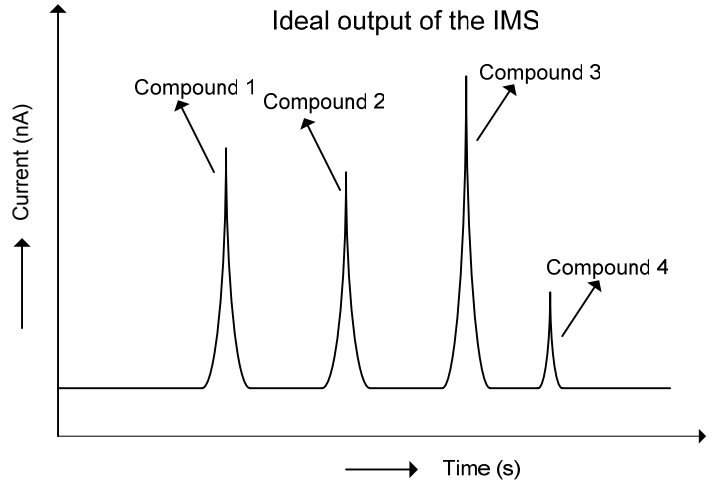


Figure 2.1 Typical output signals from the IMS

obtained from IMS. The time of flight of each ion will be different due to the molecular weight of compound [2].

1. Block Diagram of Sensing Circuit

Prior explanation of the IMS suggests that the required sensing circuit should have a current amplifier (or preamplifying stage) and an ADC. The block diagram for the sensing circuit will be as following:

Figure 2.2 Block diagram of sensing circuit

Since we know the order of the input currents from the IMS, the gain of the preamplifier should be large enough to boast the signal to a level that can be detected by the ΔΣ modulator. Usually, an operational amplifier (op-amp) is used for amplifying a signal. Due to the high noise surroundings, the selection of the op-amp is critical in this case. A wrong selection of the op-amp could distort the signal and would result in low SNR. We have to pick a low-noise op-amp with good common mode range and precision to sense smaller currents.

2. Preamplifier Stage

One of the good signal amplifying circuit topologies for analog signals is an inverting amplifier. In this topology, feedback is used to control and stabilize the amplifier gain. Stabilization is obtained by feeding the output back into the input (closed negative feedback loop). In this way the closed-loop gain does not depend on the

amplifier characteristics. Figure 2.3 shows the conventional inverting amplifier with equal positive and negative power supplies. The gain of the inverting amplifier can be

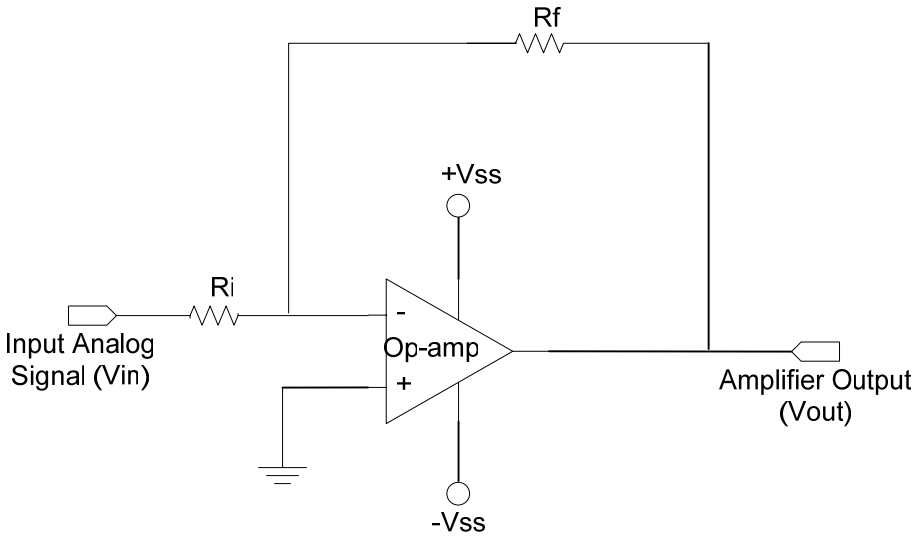


Figure 2.3 Conventional inverting amplifier circuit

calculated using following equations:

$$\frac{V_{in}-0}{R_i}=\frac{0-V_{out}}{R_f} \qquad \text{..... (2.1)}$$

$$\frac{V_{out}}{V_{in}}=-\frac{R_f}{R_i} \qquad \text{..... (2.2)}$$

Equation (2.1) gives the gain of the inverting amplifier. Negative in the equation indicates that the output signal is an inverted version of the input. Remembering that the input signal for the preamplifier is current, not voltage, the input resistance should be removed and the signal should be fed directly to the inverting terminal of the op-amp. In order to attain huge gain in this circuit, R_f should be very big. Figure 2.4 shows the

inverting current amplifier circuit, which has been used as a base model preamplifier to the IMS. The relation between the input current and the output voltage will be:

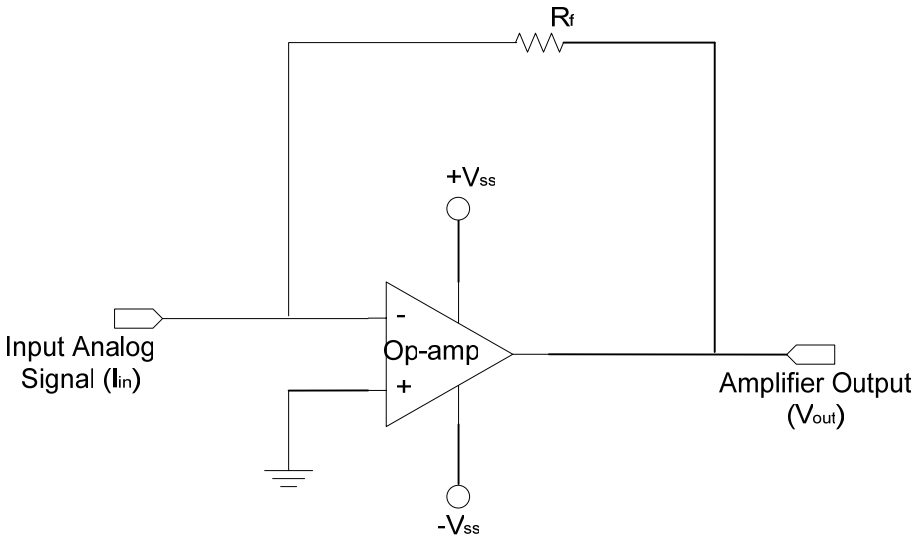


Figure 2.4 Base model of the preamplifier circuit

$$I_{in} = \frac{(0 - V_{out})}{R_f} \qquad \text{….. (2.3)}$$

$$V_{out} = -I_{in}R_f \qquad \text{….. (2.4)}$$

Characterizing, realizing huge gain and the interfacing with ADC of the preamplifier stage will be discussed elaborately in chapter III.

3. Delta-Sigma Modulator (ADC)

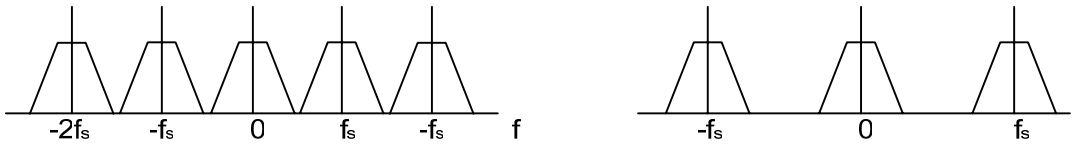
We always have relied on the digital circuits for their robustness and extremely small and simple structures. The digitization of the output signal from the IMS is vital for the FPGA to acquire the data for further processing. Choosing the ADC is another critical aspect in the construction of sensing circuit. Some of the requirements in the ADC for

this particular purpose are precision, resolution, good noise shaping, fidelity etc. In a way, ADC's are classified into two main categories: Nyquist-rate and oversampled converters. In the former category, there exists a one-to-one correspondence between the input and output samples. Each input sample, regardless of the earlier inputs, is separately processed. These types of converters have no memory of the previous inputs or outputs. As name implicates, the sampling rate f_S of the Nyquist-rate converters can be as low as Nyquist's criterion requires, which is twice the bandwidth f_B of the input signal. For practical reasons, the actual rate is usually higher than this minimum value. On the other hand, we have oversampling data converters which give a higher resolution and decent conversion speeds by relying on a trade-off. They use sampling rates much higher than the Nyquist rate, typically higher by a factor, and generate each output utilizing all preceding input values. Thus, the converter incorporates memory elements in its structure. This property destroys the one-to-one relation between input and output samples. Now only a comparison of the complete input and output waveforms can be used to evaluate the converter's accuracy, either in the time or in the frequency domain [8][9].

Traditional ADC architectures like successive approximation converters and dual-slope converters provide high resolution but trimming is needed for accuracy. They provide high resolution at the expense of using high-speed and high accuracy integrators and high-precision sample and hold circuits. Oversampling ADCs are preferred over

these because they achieve high resolution with digital signal processing techniques used in place of precise and complex analog components [8] [9].

The signal is sampled at a rate much higher than the signal bandwidth, so aliasing is not a major factor. If we consider the frequency domain representation of an oversampling converter, the frequency spectra are widely spaced. So, there is no problem of frequency spectra overlap and aliasing. So compared to Nyquist rate converters, oversampling ADCs achieve higher resolution, need simple anti-aliasing circuitry and less analog circuitry, have accuracy independent of component matching. The only disadvantage compared to Nyquist rate converters is that they operate at higher frequencies to sample the input resulting in higher power dissipation. Indeed, oversampling ADCs tradeoff time resolution for amplitude resolution [8] [9].



(a) **(b)**

Figure 2.5 Frequency domain for (a) Nyquist rate converter (b) an oversampling converter [9] [10]

The delta-sigma modulator uses the oversampling technique to achieve the high resolution and averaging effect in the conversion process. The input signal is sampled, quantized and modulated. The modulator outputs a digital signal whose continuous average represents of the input signal. This type of modulation is referred to as sigma-delta or delta-sigma modulation. The oversampling converter can take hundreds of

samples over a period of time to output a digital signal. Digital filters are used to filter the quantization noise and attenuate spurious signals [8] [9] [10].

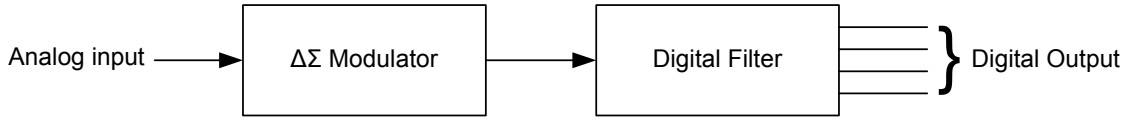


Figure 2.6 Basic block diagram of an oversampling ADC

CHAPTER THREE: PREAMPLIFIER CIRCUIT

1. Analysis of the Preamplifier Circuit

In this chapter, the preamplifier is completely characterized using simulations and experiments. Figure 3.1 shows the preamplifier with a resistive T-network used to model the input current from the IMS for on-bench test purpose. R1 and R3 at the input act as a resistive divider for the IMS output signal modeling (for on-bench test, a laboratory level function generator has been used). For example, if the input to the circuit is 1V and resistors R1 and R3 are 1MEGΩ and 1KΩ then the node V2 will be at 1mV. R2 is used as voltage to current converter to model the IMS output current. TLC 2201, an op-amp, is a precision low noise amplifier, which uses Texas Instruments Advanced LinCMOS process [7]. These op-amps combine the noise performance of the low-noise JFET amplifiers with the DC precision available previously only in bipolar amplifiers. The combination of excellent DC and noise performance with a common-mode input voltage range that includes the negative rail makes these devices an ideal choice for high-impedance, low-level signal-conditioning applications in either single-supply or split-supply. The power supply of -3V to +3V has been used to keep the reference at ground. This will force the output to use the ground as a reference. Discussing the feedback path in the circuit, a similar resistive T-network was used to realize the huge resistor requirement for acquiring huge gain. Since the input of current will be in nA, the effective resistance of the feedback path should be in the order of GΩs. As discussed in

chapter II, the topology used is a conventional inverting amplifier. This suggests that the output of the circuit will be an inverted signal of the input. Figure 3.1 shows the schematic of the preamplifier with the input resistive network and some of the derivations for the circuit derived follow.

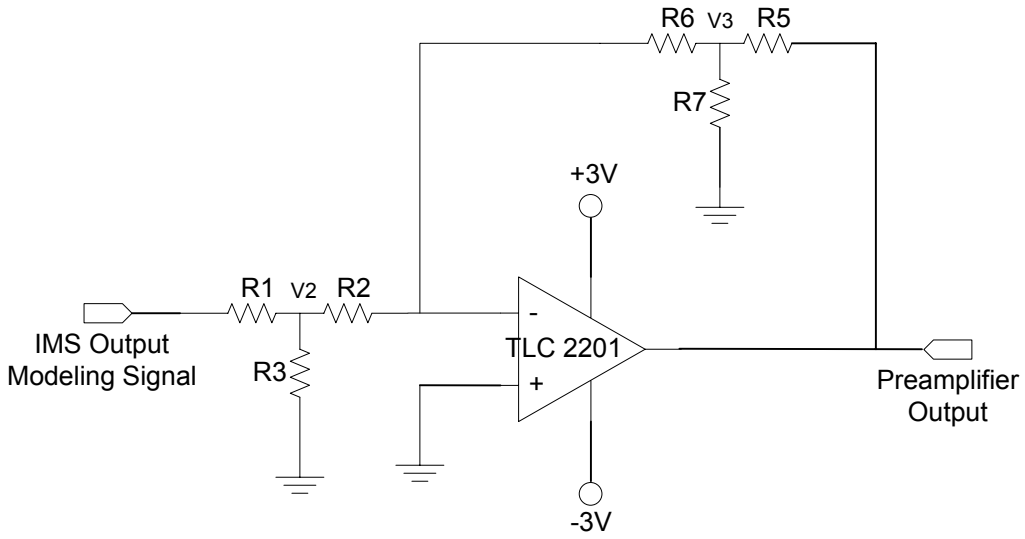


Figure 3.1 Preamplifier circuit with resistive T-network used to model IMS output currents

Gain calculations for preamplifier with input resistive T-network model:

Using Kirchoff's current law (KCL) at node V_2, the equations are:

$$\frac{V_2}{R_3}+\frac{V_2}{R_2}=\frac{V_I-V_2}{R_1} \qquad \text{..... (3.1)}$$

$$\frac{V_2}{R_1}+\frac{V_2}{R_2}+\frac{V_2}{R_3}=\frac{V_I}{R_1} \qquad \text{..... (3.2)}$$

$$V_2\left(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}\right)=\frac{V_I}{R_1} \qquad \text{..... (3.3)}$$

$$V_2=V_I\left(\frac{R_2R_3}{R_1R_2+R_2R_3+R_3R_1}\right) \qquad \text{..... (3.4)}$$

Using KCL at node V_3, the equations are:

$$0 - V_3 = \frac{V_2}{R_2}(R_6) \quad \text{..... (3.5)}$$

$$\frac{V_3}{R_6} = -\frac{V_2}{R_2} \quad \text{..... (3.6)}$$

and following equation can also be obtained at node V_3

$$-\frac{V_3}{R_6} = \frac{V_3}{R_7} + \frac{V_3 - V_{OUT}}{R_5} \quad \text{..... (3.7)}$$

$$\frac{V_{OUT}}{R_5} = \frac{V_3}{R_5} + \frac{V_3}{R_6} + \frac{V_3}{R_7} \quad \text{..... (3.8)}$$

$$V_{OUT} = V_3\left(\frac{R_5R_6 + R_6R_7 + R_7R_5}{R_6R_7}\right) \quad \text{..... (3.9)}$$

Substituting equation (2) in equation (3) will give the following equations:

$$V_{OUT} = -V_2\left(\frac{R_6}{R_2}\right)\left(\frac{R_5R_6 + R_6R_7 + R_7R_5}{R_6R_7}\right) \quad \text{..... (3.10)}$$

$$V_{OUT} = -V_2\left(\frac{R_5R_6 + R_6R_7 + R_7R_5}{R_2R_7}\right) \quad \text{..... (3.11)}$$

Substituting equation (1) in equation (4) will give the following relation:

$$V_{OUT} = -V_I\left(\frac{R_2R_3}{R_1R_2 + R_2R_3 + R_3R_1}\right)\left(\frac{R_5R_6 + R_6R_7 + R_7R_5}{R_2R_7}\right) \quad \text{..... (3.12)}$$

$$V_{OUT} = -V_I\left(\frac{R_3}{R_7}\right)\left(\frac{R_5R_6 + R_6R_7 + R_7R_5}{R_1R_2 + R_2R_3 + R_3R_1}\right) \quad \text{..... (3.13)}$$

$$\frac{V_{OUT}}{V_I} = -\left(\frac{R_3}{R_7}\right)\left(\frac{R_5R_6 + R_6R_7 + R_7R_5}{R_1R_2 + R_2R_3 + R_3R_1}\right) \quad \text{..... (3.14)}$$

The preamplifier for the real time IMS has been shown in figure 3.2 and the derivation equations using current as an input signal to the circuit follows.

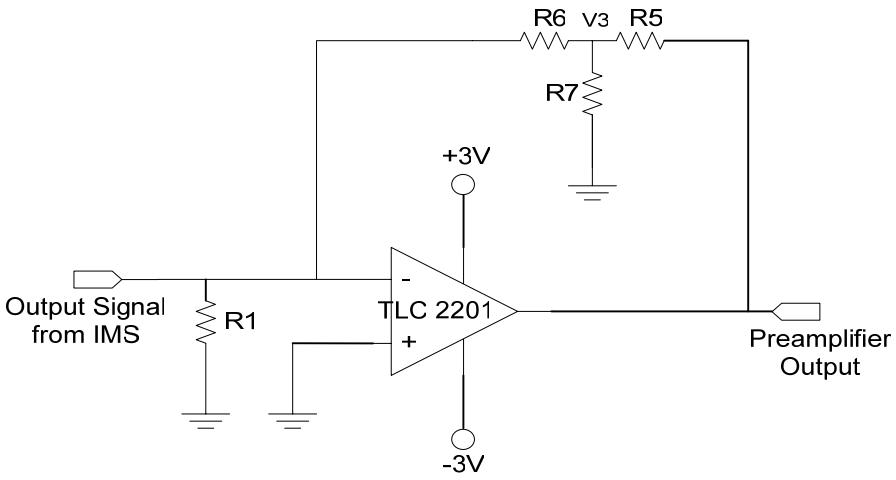


Figure 3.2 Preamplifier circuit for the real time IMS output signals

R_1 is a very big resistor, which has been used to ensure that the negative terminal of the op-amp does not float when there is no signal from IMS. Analyzing output voltage of preamplifier with the input current of I_{IMS}:

Using KCL at node V_3, the equation is:

$$-\frac{V_3}{R_6} = I \qquad \text{….. (3.15)}$$

$$V_3 = -I(R_6) \qquad \text{….. (3.16)}$$

Similarly, following equations can also be obtained at V_3,

$$\frac{V_3}{R_7} + \frac{V_3 - V_{OUT}}{R_5} = -\frac{V_3}{R_6} \qquad \text{….. (3.17)}$$

$$-\frac{V_{OUT}}{R_5} = -\frac{V_3}{R_5} - \frac{V_3}{R_6} - \frac{V_3}{R_7} \qquad \text{….. (3.18)}$$

$$\frac{V_{OUT}}{R_5} = V_3\left(\frac{R_5R_6 + R_6R_7 + R_7R_5}{R_5R_6R_7}\right) \quad \text{….. (3.19)}$$

$$V_{OUT} = V_3\left(\frac{R_5R_6 + R_6R_7 + R_7R_5}{R_6R_7}\right) \quad \text{….. (3.20)}$$

Substituting equation (6) in equation (8) will give the following relation:

$$V_{OUT} = -I\left(\frac{R_5R_6 + R_6R_7 + R_7R_5}{R_7}\right) \quad \text{….. (3.21)}$$

It is normal for an op-amp to have offset, practically. This appears as a DC component in the output of the circuit though it is not present in the input. The off-set in the circuit is due to the miss matches in various components in the op-amp circuit, internally. It isn't practical to manufacture an op-amp without any mismatches. In order to model this offset

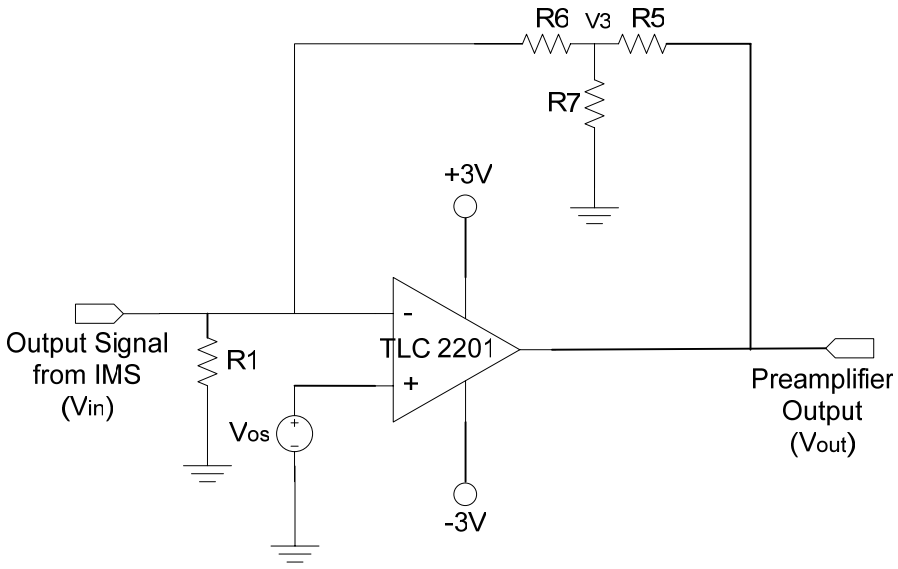


Figure 3.3 Modeling of offset in the preamplifier circuit

in the preamplifier circuit, we have introduced a DC voltage of V_{OS} at the positive terminal of the op-amp. This type of referring offset in the output to the input is generally called input referred offset. The analysis of the offset gives an idea of variation in the output signal due to the input referred offset of the op-amp (though it is not actually due the input terminals). Figure 3.3 represents the input referred offset of the preamplifier circuit and the analysis of the circuit is as follows:

Using KCL at node V_3, the equation is:

$$-\frac{V_3 - V_{OS}}{R_6} = I \qquad \text{….. (3.22)}$$

$$V_3 = V_{OS} - I(R_6) \qquad \text{….. (3.23)}$$

Similarly, following equations can also be obtained at V_3:

$$\frac{V_3}{R_7} + \frac{V_3 - V_{OUT}}{R_5} = \frac{V_{OS} - V_3}{R_6} \qquad \text{….. (3.24)}$$

$$-\frac{V_{OUT}}{R_5} = \frac{V_{OS}}{R_6} - \frac{V_3}{R_5} - \frac{V_3}{R_6} - \frac{V_3}{R_7} \qquad \text{….. (3.25)}$$

$$\frac{V_{OUT}}{R_5} = V_3\left(\frac{R_5R_6 + R_6R_7 + R_7R_5}{R_5R_6R_7}\right) - \frac{V_{OS}}{R_6} \qquad \text{….. (3.26)}$$

$$V_{OUT} = \frac{V_3(R_5R_6 + R_6R_7 + R_7R_5) - V_{OS}(R_5R_7)}{R_6R_7} \qquad \text{….. (3.27)}$$

Substituting equation (9) in equation (10) will give the following relation:

$$V_{OUT} = \frac{(V_{OS} - I(R_6))(R_5R_6 + R_6R_7 + R_7R_5) - V_{OS}(R_5R_7)}{R_6R_7} \qquad \text{….. (3.28)}$$

$$V_{OUT} = -I\left(\frac{R_5R_6 + R_6R_7 + R_7R_5}{R_7}\right) + V_{OS}\left(\frac{R_5 + R_7}{R_7}\right) \qquad \text{….. (3.29)}$$

Assuming that R_5 is much bigger than R_7, the relation reduces to:

$$V_{OUT} = -I\left(\frac{R_5R_6 + R_6R_7 + R_7R_5}{R_7}\right) + V_{OS}\left(\frac{R_5}{R_7}\right) \quad \text{..... (3.30)}$$

2. Simulation Results of the Preamplifier

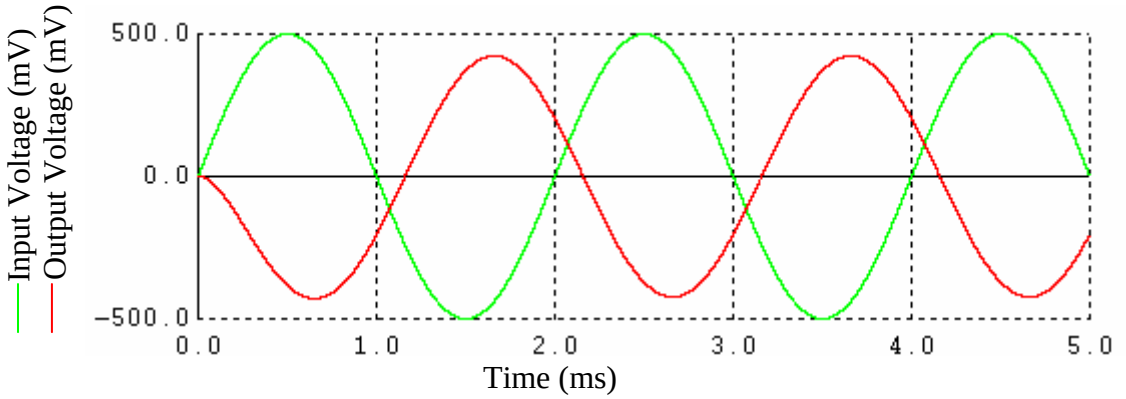


Figure 3.4 Simulation of transient analysis of the preamplifier circuit with a sine wave of 500Hz, 1V V_{PP} and 0V offset as input

Due to the inability to directly overlap the input current to the output voltage of the preamplifier, we have to match the input voltage that is used to model the input current to analyze the functionality of the preamplifier stage. Figure 3.4 shows the transient response of the preamplifier circuit in figure 3.1. The input signal applied was a sine wave with 1V V_{PP}, 0V offset and 500Hz. This simulation is similar to running a simulation with a 1nA of input current to the preamplifier from IMS. In this case 1V V_{PP} corresponds to 1nA I_{PP} from IMS. As in figure 3.4, the output of the preamplifier is about 170° out of phase to the input of the preamplifier.

Figure 3.5 shows the transient response of the preamplifier circuit in figure 3.1. The input signal applied was a sine wave with 2V V_{PP}, 0V offset and 500Hz. In this case the input voltage of 2V is similar to 2nA of input current to preamplifier stage from IMS. The output shows the similar transient response of the preamplifier in figure 3.1 but with increased amplitude than in figure 3.4.

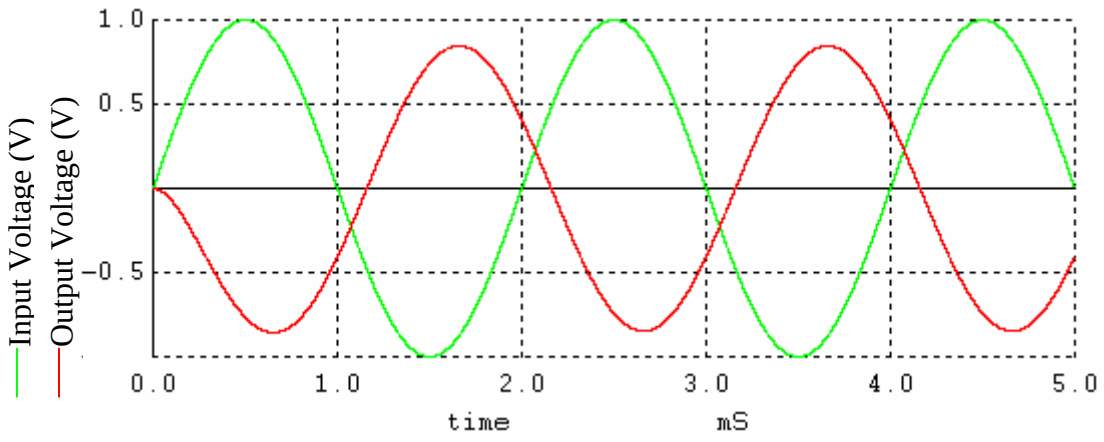


Figure 3.5 Simulation of transient analysis of the preamplifier circuit with a sine wave of 500Hz, 2V V_{PP} and 0V offset as input

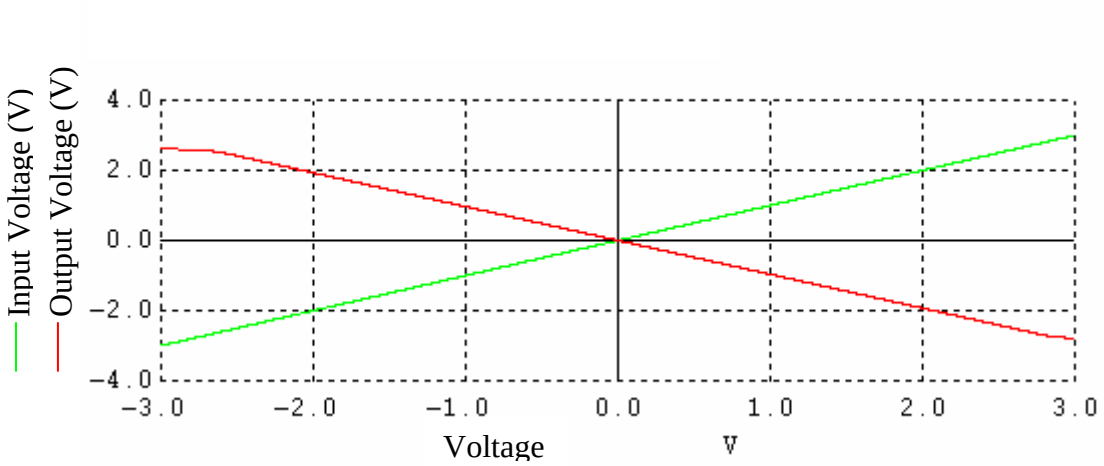


Figure 3.6 Simulation of DC analysis of the preamplifier circuit

Figure 3.6 shows the DC response of the preamplifier circuit. The variations in the output voltage were measured using a ramp signal at the input of the circuit. The response was linear but the almost 180° phase shift due to the inverting amplification can be noticed. Figure 3.7 shows the AC response of the preamplifier circuit using a SPICE simulation. The gain of the preamplifier starts to roll-off after 1kHz. The amplifier behaves as a low pass filter with some gain. Figure 3.8 shows the phase response of the

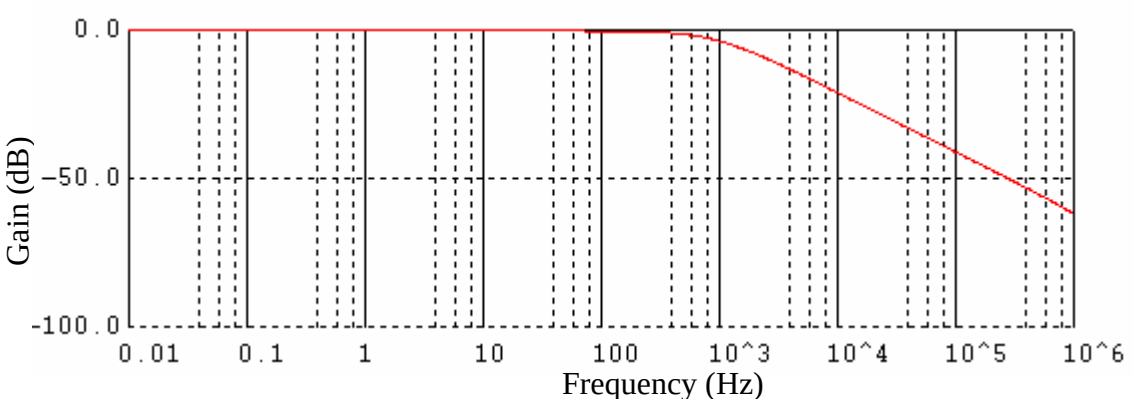


Figure 3.7 Simulation of AC analysis of the preamplifier circuit

preamplifier circuit. The phase shift of the preamplifier was about 180° when the gain was constant.

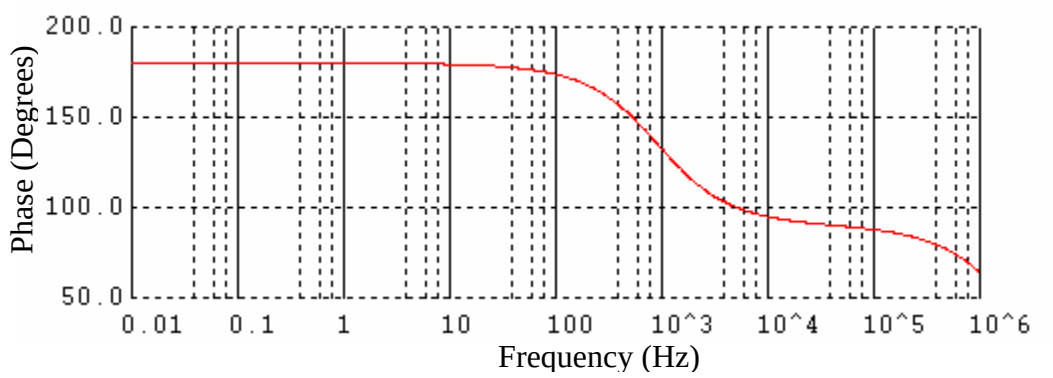


Figure 3.8 Simulation of AC (phase) analysis of the preamplifier circuit

3. On-bench Test Results of Preamplifier Circuit

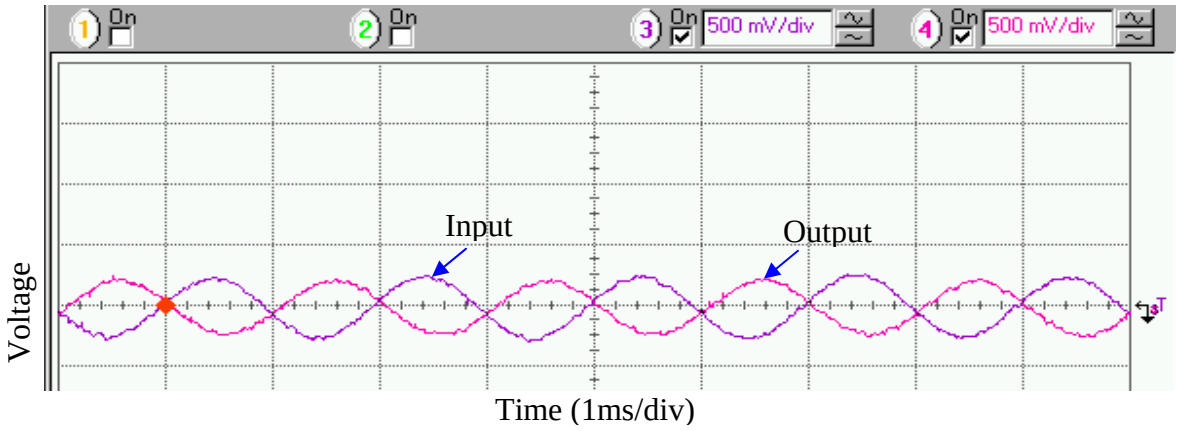


Figure 3.9 Test result of the preamplifier circuit with sine wave of 500Hz, 1V V_{PP}, and 0V off-set as input

Similar to the simulation results, the input current from the IMS is modeled using a voltage source and T-network resistors. Figure 3.9 shows the on-bench test results of the preamplifier circuit using a sine wave of 500Hz, 500mV V_{PP}, and 0V offset. 500mV V_{PP} of input voltage corresponds to 0.5nA of input current to the preamplifier stage from IMS. The results on-bench matches the results that were estimated using simulations. In

figure 3.10 the output was AC coupled to remove the offset due to miss-matches in the manufacturing of op-amp. Figure 3.11 shows the frequency response of the preamplifier. This response was tested manually by varying the frequency of the input signal.

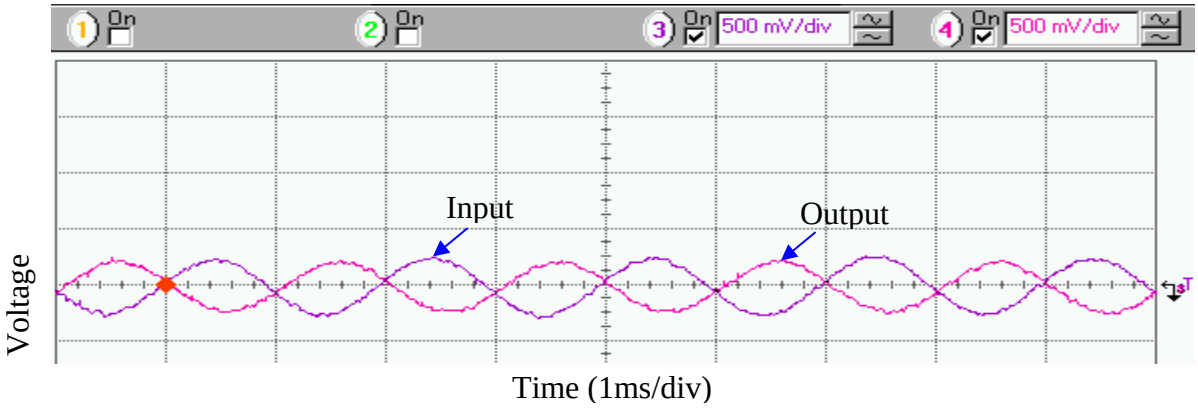


Figure 3.10 Test result of the preamplifier circuit with AC coupling and a sine wave of 500Hz, 500mV V_{PP} and 0V offset as input

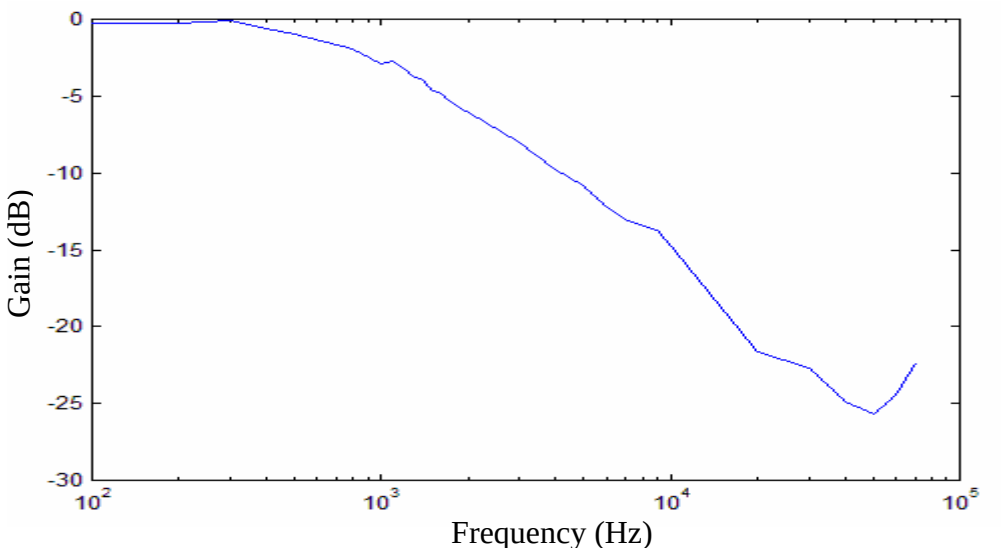


Figure 3.11 Gain Vs frequency plot from the test results of the preamplifier circuit with a sine wave of 500Hz, 1V V_{PP} and 0V offset as an input

4. Test results with IMS

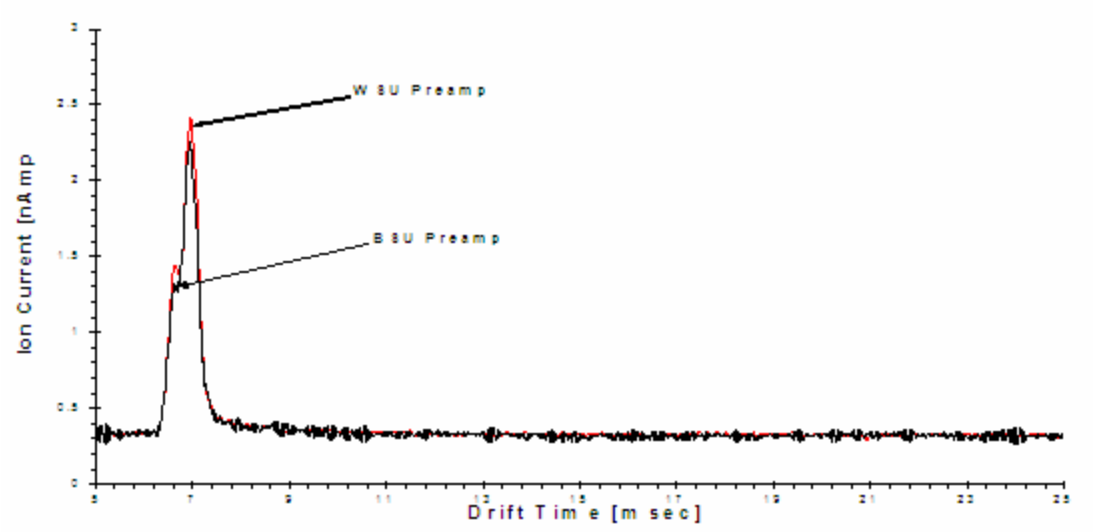


Figure 3.12 Comparison between BSU's preamplifier (Black) and WSU's preamplifier (Red) when RIP was formed in WSU's IMS [11]

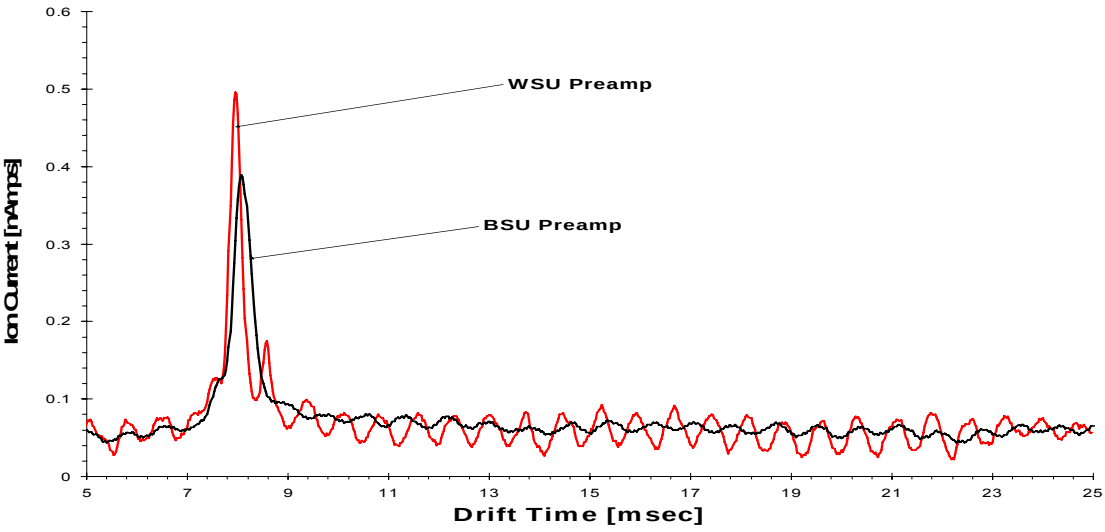


Figure 3.13 Comparison between BSU's preamplifier (Black) and WSU's preamplifier (Red) when the RIP was formed in BSU's IMS [11]

Figure 3.12 shows the comparison between BSU's preamplifier and WSU's preamplifier when the RIP was formed in WSU's IMS. RIP's formed were almost identical except the amplitude of the RIP formed using BSU's preamplifier was less by 0.2nA on the graph. Figure 3.13 shows that the RIP from BSU's preamplifier was wider and shorter than RIP from WSU's preamplifier. This is due to the lesser bandwidth of the feedback signal in BSU's preamplifier.

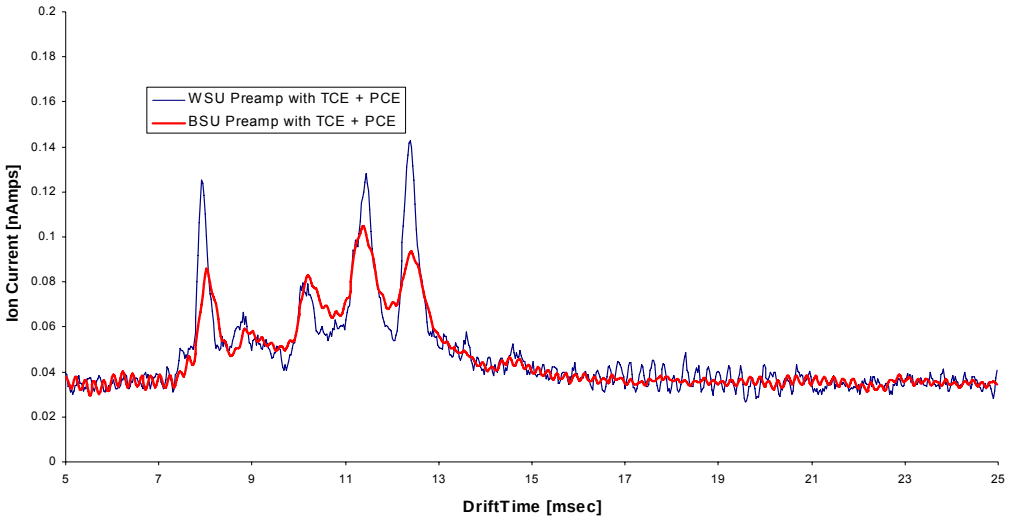


Figure 3.14 Comparison between BSU's preamplifier (Red) and WSU's preamplifier (Blue) when TCE and PCE were introduced into BSU's IMS [11]

Figure 3.14 gives the comparison between BSU's preamplifier and WSU's preamplifier when perchloroethene (PCE) and trichloroethene (TCE) compounds were introduced into BSU's IMS. As discussed before, the bandwidth effect on the smaller peaks is much more than on the larger peaks.

The bandwidth of the feedback signal can be increased for certain frequencies by introducing a capacitor across node V_3 and ground in figure 3.2. The modified schematic of the preamplifier circuit can be seen in figure 3.15. The capacitor in the feedback will

cause second order effects in the bandwidth. Some of the simulation results using SPICE can be seen from figure 3.16 to figure 3.18.

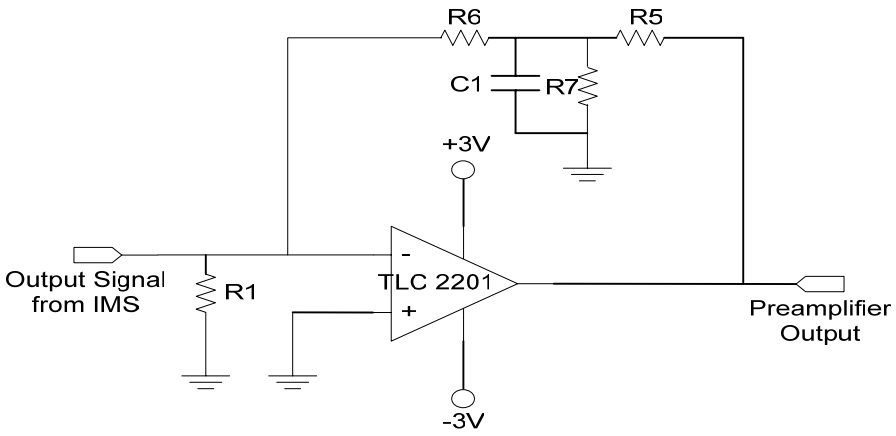


Figure 3.15 Schematic of the preamplifier after introducing a capacitor in the feedback

Figure 3.16 shows the transient response of the preamplifier circuit in figure 3.15. The capacitance should be chosen carefully in order to keep the circuit stable. If lower capacitance is chosen than the required, then there will not be much effect on the second order circuit. If higher capacitance is chosen than the required, then the circuit will not be

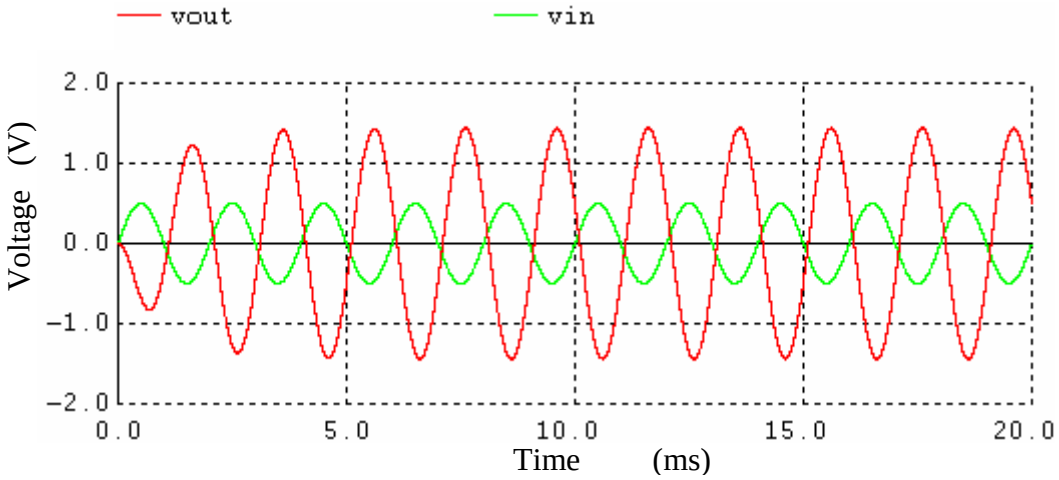


Figure 3.16 Simulation of transient analysis of the preamplifier circuit with the capacitor in the feedback

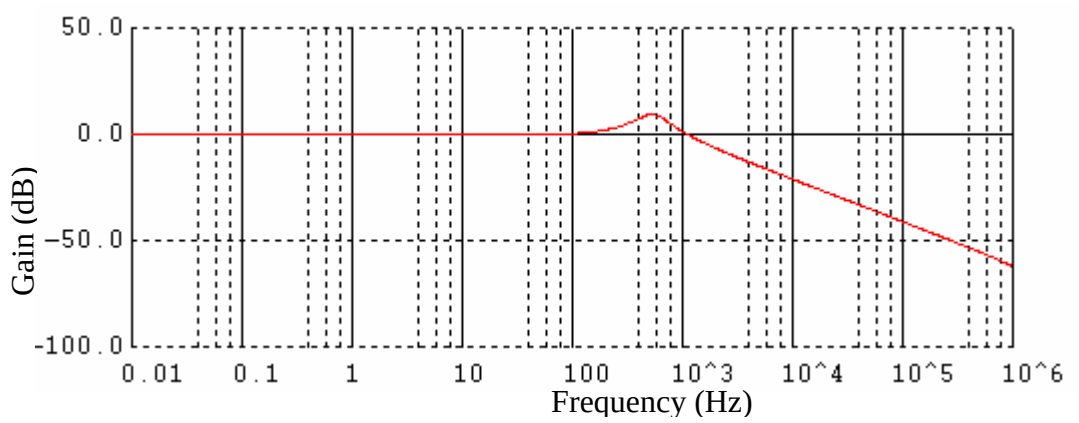


Figure 3.17 Simulation of AC analysis of the preamplifier circuit with the capacitor in the feedback

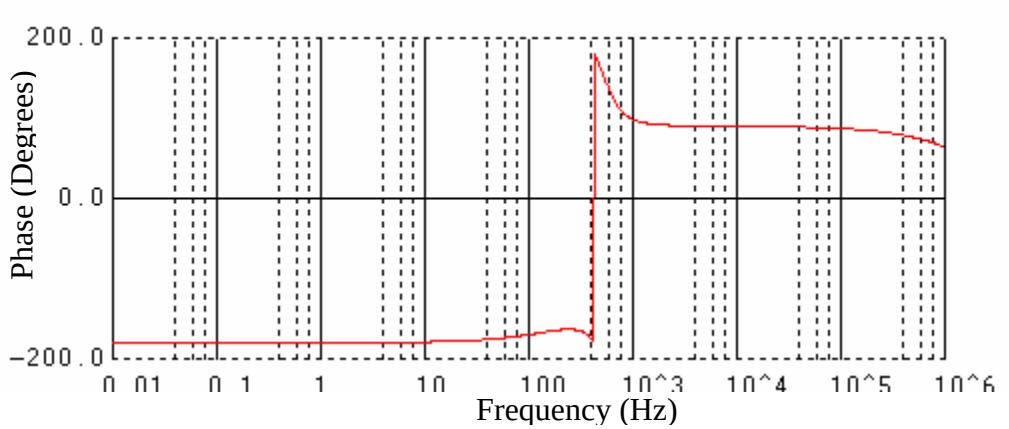


Figure 3.18 Simulation of AC (phase) analysis of the preamplifier circuit with capacitor in the feedback

stable and ringing can be seen in the output of the preamplifier. For the simulations the capacitance used was 0.5uF. Figure 3.17 shows the AC response of the preamplifier in figure 3.15. We can see that at 3dB-frequency of the preamplifier the gain is zero instead of -3dB of preamplifier in figure 3.1. From the phase response we can see that the there is a phase shift of 180° at 200Hz. This doesn't really affect the performance of the preamplifier because the final output will be inverted. This can be fixed using FPGA.

CHAPTER FOUR: DELTA-SIGMA MODULATOR (ADC)

As introduced in chapter II, delta-sigma modulator circuit is used as a digital interface between preamplifier and the FPGA. The term delta-sigma (ΔΣ) modulator is used to describe a system (analog or digital) which transforms its input, regardless of being a continuous or finely-quantized, to a coarsely-quantized output possessing a noise-shaped spectrum. To digitize a continuous time analog signal, two operations need to be performed: sampling the analog signal (commonly with constant sampling time period T) and quantizing its amplitude so that it assumes one of the finite numbers of the permitted values. The quantization process is usually uniform and any two quantized values differ by a fixed level spacing of Δ. The device used for quantization is called Quantizer or ideal ADC. The quantizer used in this case is a 1-bit quantizer. Regardless of the quantizer input, the output will have only two levels: low or high. The difference between the input characteristics and the approximate output is called the quantization error or (not perfectly correct) the quantization noise. Figure 4.1 shows the block diagram of the simplest analog ΔΣ modulator. The first order ΔΣ modulator is a first order loop system containing an integrator and a 1-bit ADC in the forward path, and a 1-bit DAC in the feedback path [8] [9].

1. Block Diagram and Theory of ΔΣ Modulator

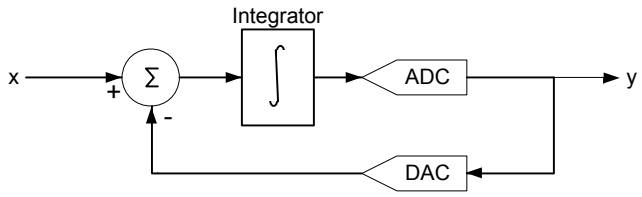


Figure 4.1 Block diagram of the simple first order ΔΣ modulator used as ADC [8] [9]

Now that the basic operation of the ΔΣ modulator has been illustrated, explaining the inner workings and determining why ΔΣ modulation is so beneficial for generating high-resolution data would be useful. Figure 4.2 shows the block diagram of a basic ΔΣ modulator. All the variables stated are in terms of the time, T, which is the inverse of the sampling frequency f_s and n, which is an integer. The 1-bit ADC is simply a comparator and a digital filter that converts an analog signal into either a high or low and samples it at high frequency. The 1-bit DAC uses the comparator output to ascertain if $+V_{ref}$ or $-V_{ref}$ is added to the input. As the advantages of the ΔΣ modulation are not perceptible, a simple derivation of the output, $y(nT)$, is used to elucidate its typical advantages [5]. The output of the integrator, $u(nT)$, can be described as

$u(nT)$ = integrator's previous input + integrator's previous output

$$= [x(nT-T)-q(nT-T)]+u(nT-T) \qquad \text{….. (4.1)}$$

where $T = \frac{1}{f_s}$ = (sampling frequency)$^{-1}$,

n is an integer value [10].

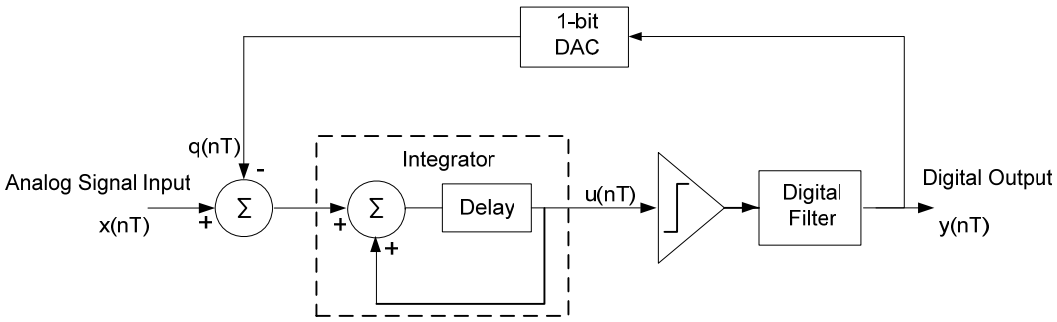


Figure 4.2 Block diagram of the basic first order ΔΣ modulator [8] [9] [10]

Where, $x(nT-T)-q(nT-T)$ is equal to the integrator's previous input, and $u(nT-T)$ is its previous output. The quantization error associated with the 1-bit ADC can be defined as the difference between its output and input such that [10]

$$Q_e(nT) = y(nT) - u(nT) \qquad \text{..... (4.2)}$$

Substituting equation 4.2 in equation 4.1, the output of the modulator is

$$y(nT) = [Q_e(nT) + x(nT-T)] - [q(nT-T) - u(nT-T)] \qquad \text{..... (4.3)}$$

Assuming the 1-bit DAC to be ideal, we can write

$$y(nT) = q(nT) \qquad \text{..... (4.4)}$$

Plugging in equations 4.4 and 4.2 in equation 4.3, we get

$$y(nT) = [Q_e(nT) + x(nT-T)] - [q(nT-T) - u(nT-T)] \qquad \text{..... (4.5)}$$

$$y(nT) = x(nT-T) + Q_e(nT) - Q_e(nT-T) \qquad \text{..... (4.6)}$$

From equation 4.6, we can observe that the output of the sigma delta modulator consists of a quantized value of the input signal delayed by one sample period and a difference of quantization error between present and preceding values. So, to a first order, quantization noise cancels itself [10].

2. Analysis of the ΔΣ modulator in Frequency Domain

The frequency domain analysis will further clarify this crucial fact. Figure 4.3 shows a model of first order ΔΣ modulator in the s-domain. The integrator is represented with its ideal transfer function of $\frac{1}{s}$. The 1-bit ADC can be represented with a simple error source, $Q_e(s)$. If the 1-bit DAC is assumed to be ideal, following equations can be written:

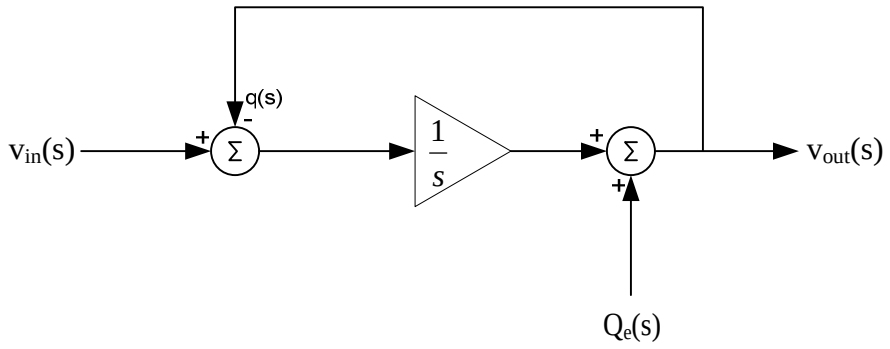


Figure 4.3 Block diagram of the basic first order ΔΣ modulator in s-domain [9] [10]

The output of the modulator can be written as

$$V_{out}(s) = Q_e(s) + \frac{1}{s}[V_{in}(s) - V_{out}(s)] \qquad \text{….. (4.7)}$$

$$V_{out}(s) = Q_e(s)(\frac{s}{s+1}) + V_{in}(s)(\frac{1}{s+1}) \qquad \text{….. (4.8)}$$

The modulator behaves as a low-pass filter for the input signal and as a high-pass filter for the quantization noise. If we observe the frequency response of the ΔΣ modulator, shown in figure 4.4, we see that in the region of input signal, the signal has

high gain while the effect of noise is minimized. At higher frequencies beyond the bandwidth of the input signal, quantization noise takes over. This high-pass characteristic of pushing the noise out of the bandwidth of the input signal is called Noise Shaping [9] [10].

By oversampling, the noise bandwidth is distributed over a wider bandwidth as shown in figure 4.6. If a digital low pass filter is applied to the modulator output, much of the quantization noise is removed without affecting the wanted signal. ΔΣ modulator shapes the quantization noise so that most of it lies above the pass band of the digital output filter. So, a high-resolution analog to digital conversion can be obtained with a low resolution ADC [9] [10].

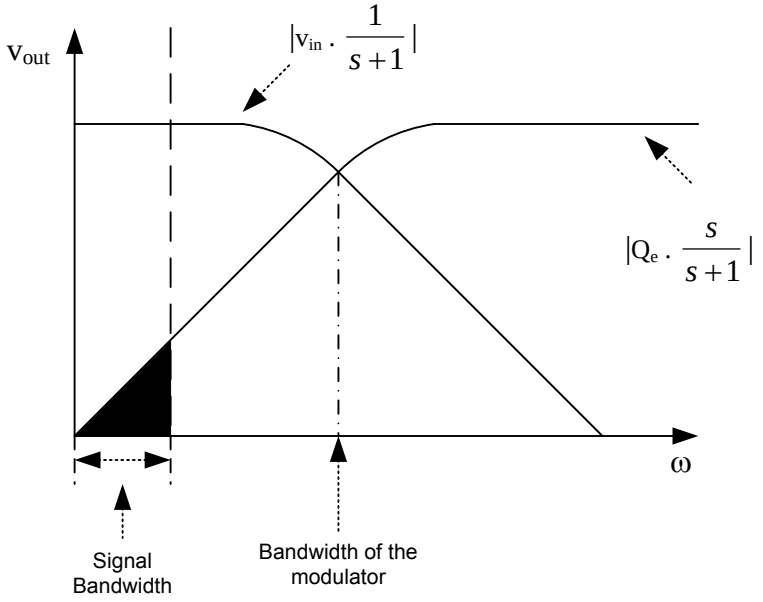


Figure 4.4 Frequency response of the first-order ΔΣ modulator [9] [10]

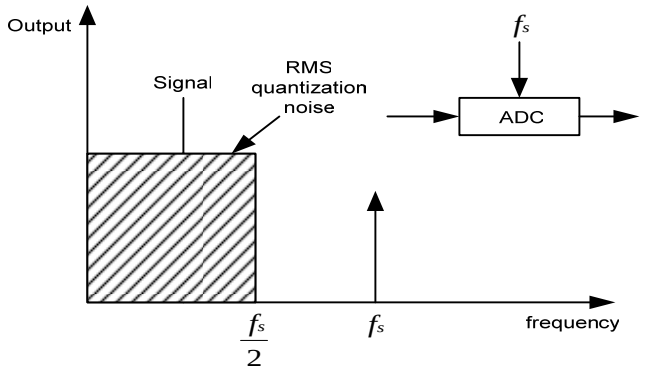


Figure 4.5 RMS quantization noise in a typical ADC with sampling frequency f_s [9] [10]

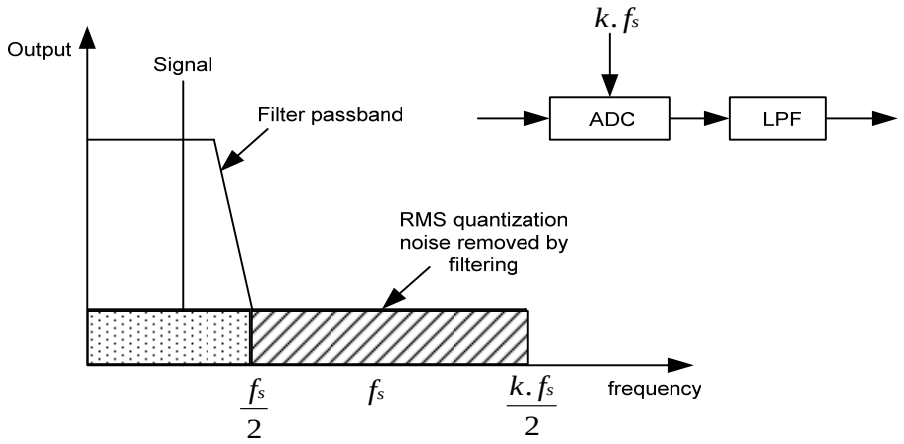


Figure 4.6 RMS quantization noise in an oversampled ADC with sampling frequency of $k.f_s$ [9] [10]

Figure 4.5 shows the quantization noise of the typical Nyquist data converter. The quantization noise is concentrated in the band of interest. Usually, the sampling frequency in Nyquist converters is double is signal frequency. Figure 4.6 shows the distribution of quantization noise in an oversampled converter. The quantization noise in the signal bandwidth in oversampled data converters is much less in the Nyquist data converters.

CHAPTER FIVE: NOISE ANALYSIS OF THE FIRST ORDER ΔΣ MODULATOR

Analyzing the noise in the system is one of the most important aspects. The affects of noise in on data conversion could change the functionality of the system as whole. The SNR of the system, ideally, was calculated using the derivations of the quantization noise in chapter IV. Figure 5.1 shows a continuous time implementation of a first order noise shaping modulator, which is simple to implement and easy to test on the bench. It consists of an op-amp, a comparator, capacitors and resistors.

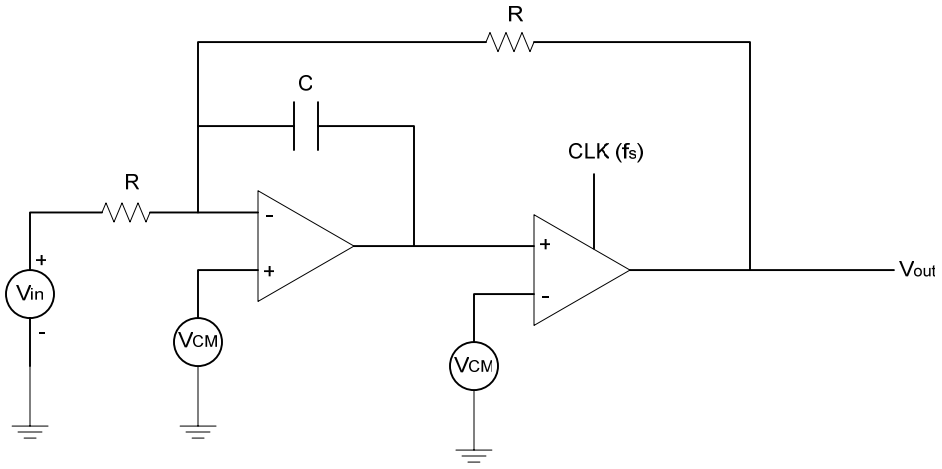


Figure 5.1 Analog implementation of a continuous time first order noise shaping modulator [9] [10]

Spice simulations are used to demonstrate the operation of this modulator. The sampling frequency is assumed to be 10MHz and the input signal used is a 10kHz sinusoidal wave with peak amplitude of 2.0V and centered on V_{CM}. VDD=4.5V and V_{CM} = 2.25V. Ideal spice models were used for the op-amp and comparator in the simulations.

Figure 5.2 shows the spice simulation result with the input and output signals of the modulator. We can clearly see that the average of the output of modulator tracks the input. When the input is at its maximum amplitude, the output of the modulator stays high (logic one) for the most part. As the input is at its minimum amplitude, the output of the modulator stays low (logic zero) for the most part. When the input signal level is moving through the common mode voltage, the modulator output bounces between VDD and ground, so that the average value matches the input value.

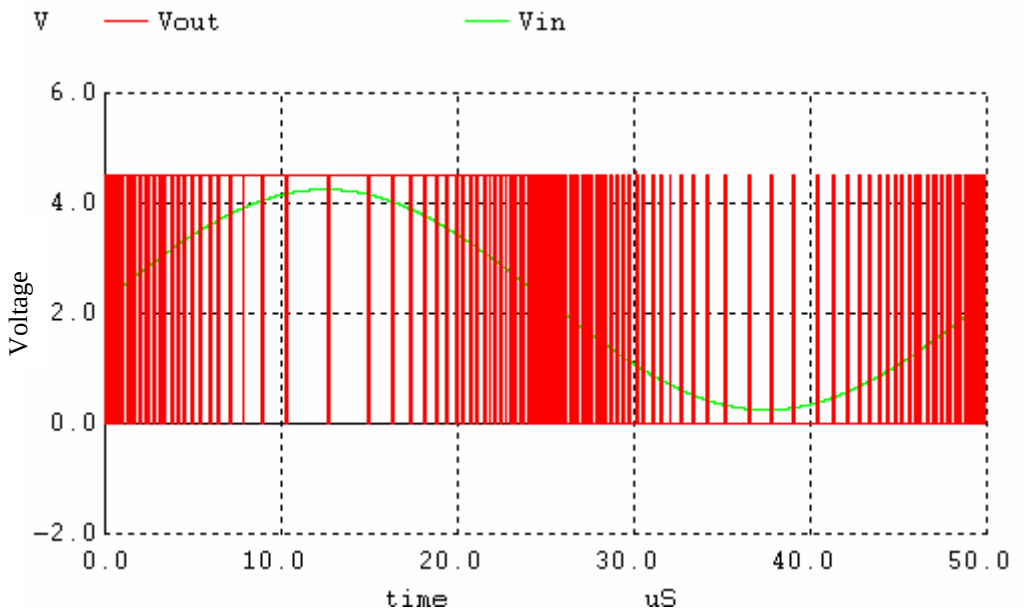


Figure 5.2 Spice simulation of the first order noise shaping modulator in figure 5.1

This 1-bit output of the modulator can be connected to a digital averaging filter to get a higher resolution output. The output of the filter would be a digital word representing the analog input voltage.

1. Modulation Noise in a First Order Noise Shaping Modulator

Modulation noise in a first order noise shaping modulator is theoretically explained. From equation 4.5, the output of the noise shaping modulator in the time domain is [9] [10]

$$y(nT) = x(nT - T) + Q_e(nT) - Q_e(nT - T) \quad \text{..... (5.1)}$$

Modulation noise is the differentiated quantization noise. In the z-domain, the block diagram of the noise shaping modulator can be represented as shown in figure 5.3

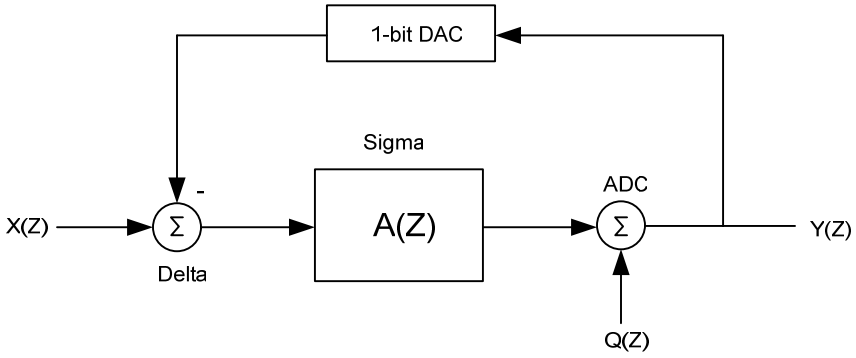


Figure 5.3 Z-domain representation of the noise shaping modulator

So, the output of the modulator is related to the input as shown in [9] [10]

$$Y(z) = \frac{A(z)}{1 + A(z)} \cdot X(z) + \frac{1}{1 + A(z)} \cdot Q(z) \quad \text{..... (5.2)}$$

Assuming A(z) = z^{-1}, this can be re-written as

$$Y(z) = (z^{-1})X(z) + (1 - z^{-1})E(z) \quad \text{..... (5.3)}$$

The product of the noise transfer function and modulation noise can be written as

$$NTF(z)E(z) = (1 - z^{-1})E(z) \quad \text{..... (5.4)}$$

The noise voltage spectral density is given by

$$V_{Qe}(f) = \frac{V_{LSB}}{\sqrt{12 f_s}} \qquad \text{..... (5.5)}$$

So, in the frequency domain, equation 8.2 can be written as

$$NTF(f).V_{Qe}(f) = (1 - e^{-j2\pi \frac{f}{f_s}})(\frac{V_{LSB}}{\sqrt{12 f_s}}) \qquad \text{..... (5.6)}$$

The power spectral density, PSD of the modulator's Modulation Noise can be written as

$$|NTF(f)|^2 . |V_{Qe}(f)|^2 = (\frac{V^2{}_{LSB}}{12 f_s}).2(1 - \cos 2\pi \frac{f}{f_s}).\frac{V^2}{Hz} \qquad \text{..... (5.7)}$$

Figure 5.4 shows the theoretical PSD from the above equation with [9] [10]

$V_{LSB} = 4.5V$ [1-bit ADC/DAC in the modulator]

$f_s = 10MHz$,

$f_n = f_s/2 = 5MHz$.

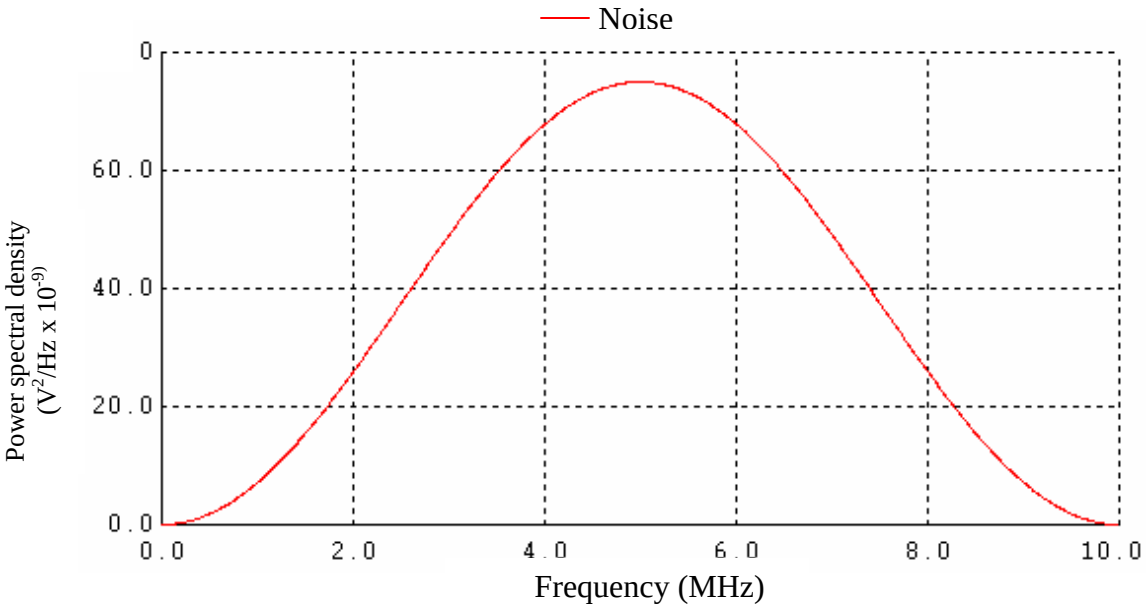


Figure 5.4 Theoretical modulation noise for a first order noise shaping modulator

Figure 5.4 shows that the modulation noise is significant. But by restricting the bandwidth of the modulation noise, we can considerably reduce the RMS quantization noise. The modulation noise spectrum of the first order noise shaping modulator in figure 5.1 can be viewed in SPICE. A slow moving voltage ramp is given as the input to the modulator. The difference between the input and output of the modulator is the modulation noise. Figure 5.5 show the slow ramp input signal and corresponding output of the noise shaping modulator. Figure 5.6 shows the modulation noise of the noise shaping modulator in figure 5.1.

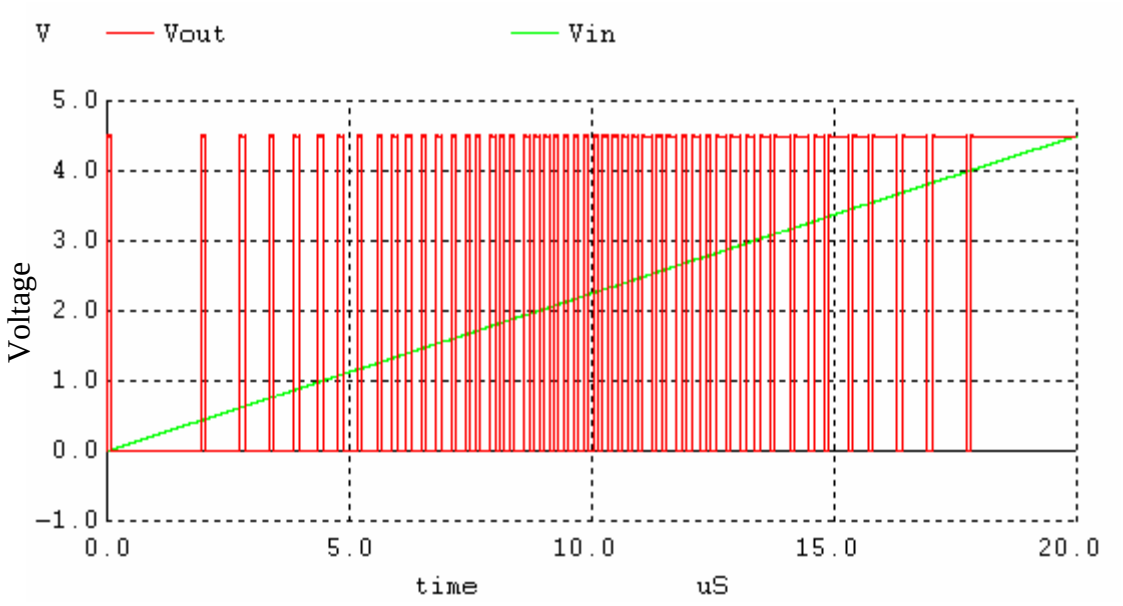


Figure 5.5 Slow ramp input signal to the modulator and its corresponding output

The PSD of the modulation noise can be obtained by squaring the magnitude of modulation noise and dividing the result with the resolution of the Fourier transform used. Figure 5.7 shows the PSD of the modulation noise. The shape of the modulation noise spectrum is comparable to the theoretical noise spectrum in figure 5.4

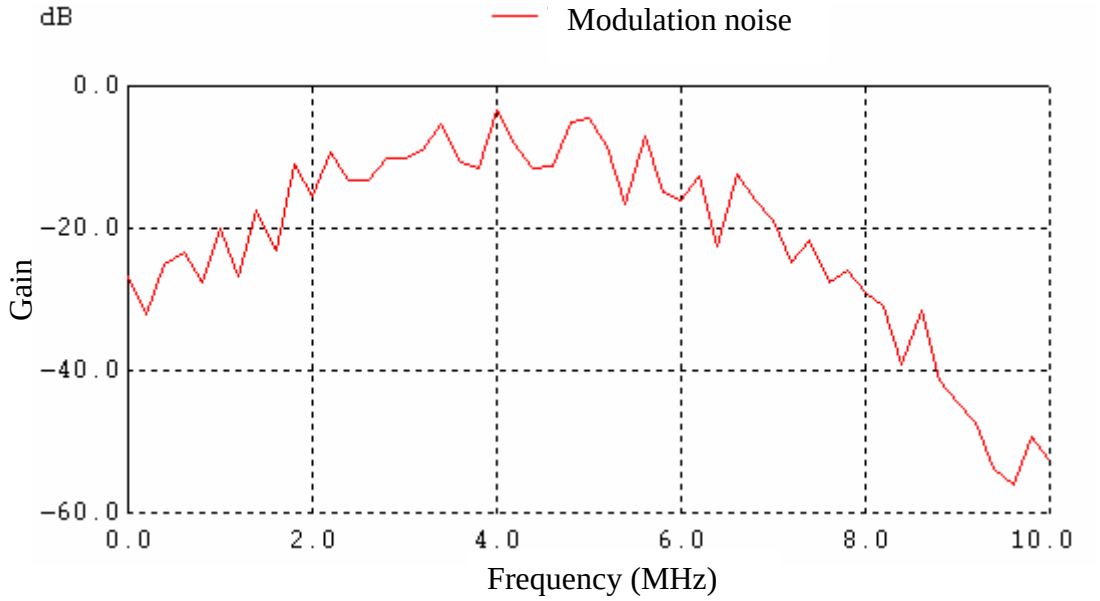


Figure 5.6 Modulation noise for a slow ramp input to the modulator

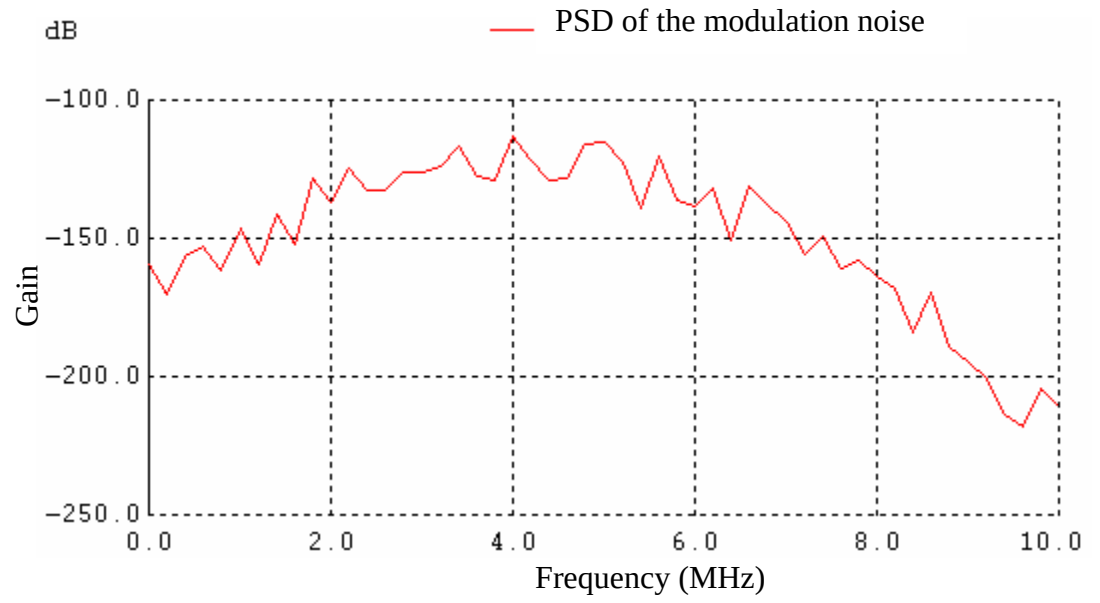


Figure 5.7 PSD of the modulation noise for a slow ramp input signal to the modulator

2. Ideal SNR of a First Order Noise Shaping Modulator

The RMS (Root Mean Square) quantization noise can be reduced by using simple averaging of ADCs outputs. If K samples are averaged, the sampling frequency is effectively increased by K times. The RMS quantization can be written as [10]

$$V_{QeRMS} = \frac{1}{\sqrt{K}}.\frac{V_{LSB}}{\sqrt{12}} \quad \text{….. (5.8)}$$

The ideal SNR (Signal to Noise Ratio) in this case is

$$SNR_{ideal} = 20.\log\frac{V_p/\sqrt{2}}{V_{Qe,RMS}} \quad \text{….. (5.9)}$$

$$SNR_{ideal} = 6.02N + 1.76 + 10LogK \quad \text{….. (5.10)}$$

So, every doubling in the oversampling ratio results in a 0.5 bit increase in resolution.

Consider the case of a first-order noise shaping modulator with K of its output samples averaged. Assuming $f \le f_n$ and the output of the modulator is passed through a perfect low pass filter, equation 5.3 can be rewritten as [10]

$$|NTF(f)|.|V_{Qe}(f)| = \frac{V_{LSB}}{\sqrt{12 f_s}}.2\sin(\pi.\frac{f}{f_s}).\frac{V}{\sqrt{Hz}} \quad \text{….. (5.11)}$$

The RMS quantization noise introduced in a bandwidth B can be calculated as

$$V^2_{Qe,RMS} = 2\int_0^B V^2{}_{Qe}(f).df \quad \text{….. (5.12)}$$

$$V^2_{Qe,RMS} = 2\int_0^B |NTF(f)|^2 . |V_{Qe}(f)|^2 .df \quad \text{….. (5.13)}$$

$$V^2_{Qe,RMS} = 2\frac{V^2{}_{LSB}}{12 f_s}.\int_0^B 4.\sin^2(\pi\frac{f}{f_s}).df \quad \text{….. (5.14)}$$

The maximum bandwidth of the input signal can be written as

$$B = \frac{f_s}{2K} \quad \text{..... (5.15)}$$

where K= oversampling ratio, which is the number of output samples averaged.

Using this in equation 5.5, we can write [10]

$$V_{Qe,RMS} = \frac{V_{LSB}}{\sqrt{12}} \cdot \frac{\Pi}{\sqrt{3}} \cdot \frac{1}{K^{3/2}} \quad \text{..... (5.16)}$$

Using equations 5.9 and 5.16, the ideal data converter SNR using the first-order NS modulator can be written as [10]

$$SNR_{ideal} = 6.02N + 1.76 - 20.Log\Pi + 20.LogK^{3/2} \quad \text{..... (5.17)}$$

$$SNR_{ideal} = 6.02N + 1.76 - 5.17 + 30.LogK \quad \text{..... (5.18)}$$

From this equation, we can see that every doubling in oversampling ratio results in 1.5bits increase in the resolution which corresponds to a 9dB increase in SNR_{ideal}. So for this noise shaping modulator with a 1-bit ADC, the final resolution (after digital filter) of the resulting data converter is N_{inc}+1 bits, where N_{inc} is given as [10]

$$N_{inc} = \frac{30\log K - 5.17}{6.02} \quad \text{..... (5.19)}$$

$$SNR_{ideal} = 6.02(N + N_{inc}) + 1.76 \quad \text{..... (5.20)}$$

The current peaks from the collector plate of the IMS occur in a time period of 0.5ms to 1ms. The worst-case minimum time period is supposed to be 0.2ms. So, we have a low frequency input signal to the modulator. The modulator's resolution is greatly dependent on the number of samples taken in a given time, KT_s. Digital filtering can be

done by passing the output of the modulator to a single accumulate and dump circuit or a counter. The output of the modulator can be band limited to f_s/K [10].

CHAPTER SIX: IMPLEMENTATION AND RESULTS OF SENSING CIRCUIT

1. Implementation of ΔΣ modulator

The Figure 6.1 shows schematic of the first order ΔΣ modulator implemented in this project work. When compared to Figure 5.1 we can see that the clocked comparator is implemented using an op-amp and a D flip-flop (DFF). By using discrete components to build the modulator, we can precisely set the values of the resistors and capacitors.

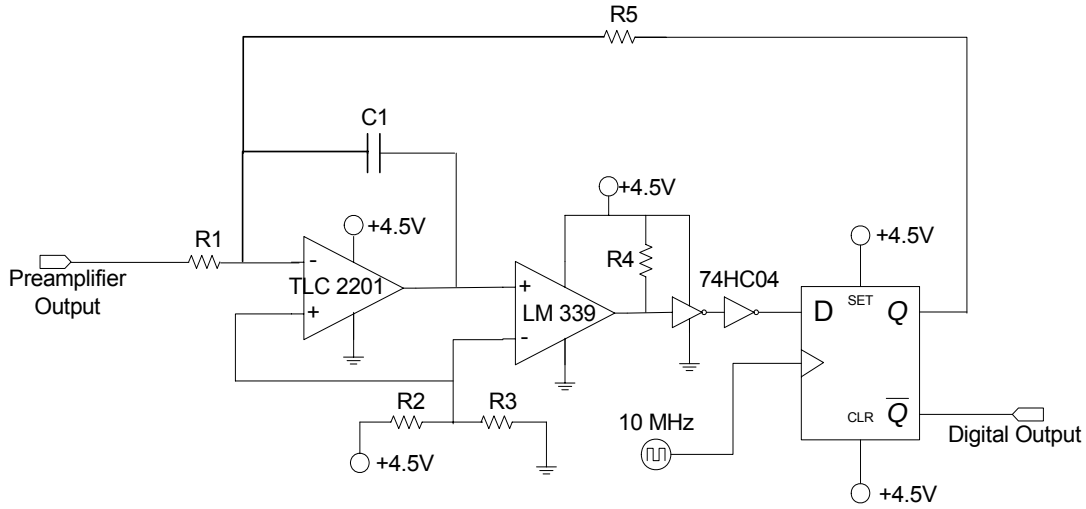


Figure 6.1 Schematic of the first order ΔΣ modulator implementation for sensing circuit

The TLC2201 is a precision, low-noise op-amp. It is used as an integrator with the non-inverting input tied to a reference voltage (2.25V here). The integrator accumulates the difference between the input and feedback signals. This is compared with the reference voltage using the LM339 comparator. The DFF is used to clock the

comparator output. So, the LM339 comparator combined with the DFF forms a clocked comparator. The output of the modulator tracks the average of the input. The average fed back signal would also ideally be the same as the input signal.

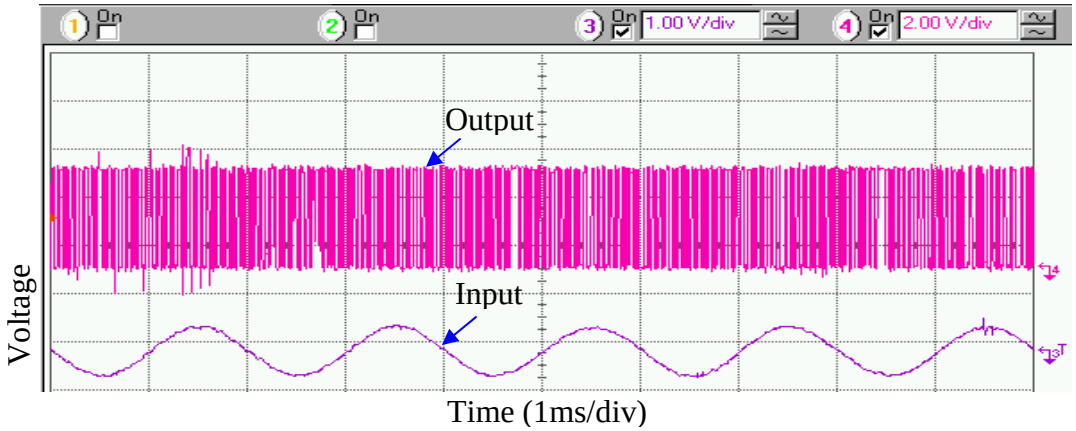


Figure 6.2 On-bench test result of the ΔΣ modulator digital output signal with sine wave of 500Hz, 1V V_{PP}, and 0V off-set as input

Figure 6.2 shows the digital output signal of the ΔΣ modulator with a sine wave of 500Hz, 1V V_{PP}, and 0V off-set as input. To verify the working of the ΔΣ modulator, we can use an analog low pass filter at the digital output of the ΔΣ modulator to reconstruct the analog input signal. Figure 6.4 shows the reconstructed analog input of digital output from ΔΣ modulator.

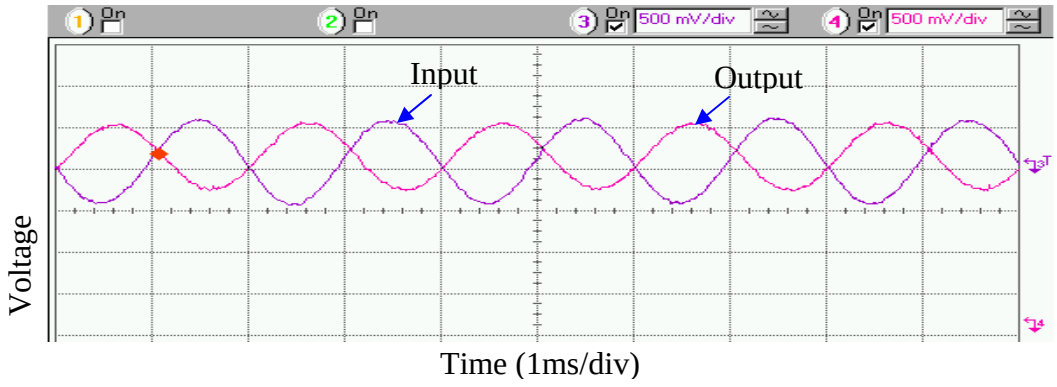


Figure 6.3 On-bench test result of the ΔΣ modulator digital output signal though an analog low pass filter with sine wave of 500Hz, 1V V_{PP}, and 0V off-set as input

2. Coupling Capacitor

Since we have some DC off-set from the preamplifier stage of the sensing circuit, the delta-sigma modulator may not give good analog to digital conversion of the sensed signal. In order to remove the DC off-set caused by the preamplifier a capacitor is introduced in between the preamplifier stage and the delta-sigma modulator, which is also called coupling capacitor. The value of the capacitor that has to be used in the circuit can be calculated. The way we are using the coupling capacitor is similar to the high pass analog filter, assuming delta-sigma modulator as a load for the preamplifier stage.

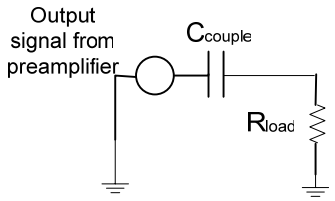


Figure 6.4 Modeling of how the coupling capacitor, with load resistance, acts as high pass filter

Following explains mathematically how the value of the capacitor is selected for coupling purpose. Since the input is a low frequency signal, the capacitor value should be chosen carefully to not get attenuated by the high pass filter. So, the coupling capacitance value should be much higher to make the high pass filter curve as steeper as possible. In Figure 6.5 both the f_{3dB} of input signal and the cutoff frequency of the modeled high pass filter should be matched to obtain the maximum signal. So,

$$f_{3dB} \leq f_{in} \qquad \text{….. (6.1)}$$

$$f_{3dB} = \frac{1}{2\pi RC} \qquad \text{….. (6.2)}$$

Substituting equation (6.2) in (6.1),

$$f_{in} \geq \frac{1}{2\pi RC} \qquad \text{….. (6.3)}$$

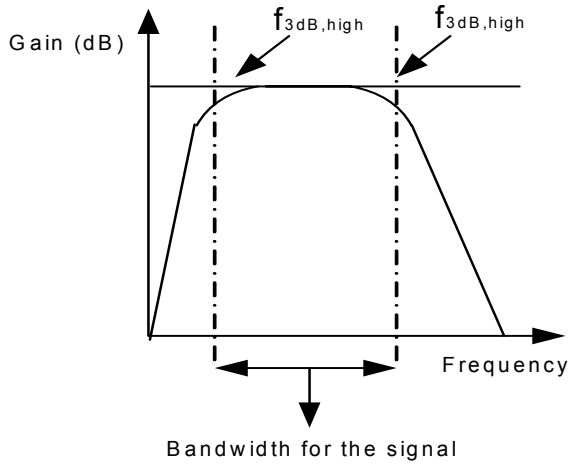


Figure 6.5 Bandwidth limitations of the sensing circuit with coupling capacitor

Assuming input signal frequency as 1 kHz and the load resistor as 10kΩ,

$$1kHz \geq \frac{1}{2\pi RC} \qquad \text{….. (6.4)}$$

$$C \geq 15nF$$

The capacitor, which was used in the test, was about 1uF.

3. Implementation of the Sensing Circuit

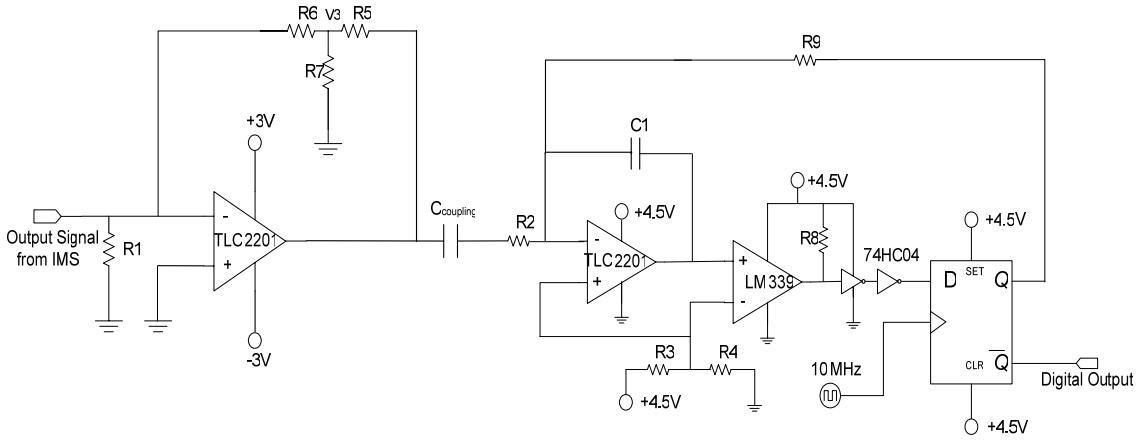


Figure 6.6 Complete schematic of the sensing circuit with coupling capacitor

The Figure 6.7 shows the printed circuit board layout of the sensing circuit shown in Figure 6.6. The component packaging style is chosen as dual-in-line packaging (DIP) for the ease of soldering to the PCB. Decoupling capacitors were used on the power supply routing to smoothen out the signal.

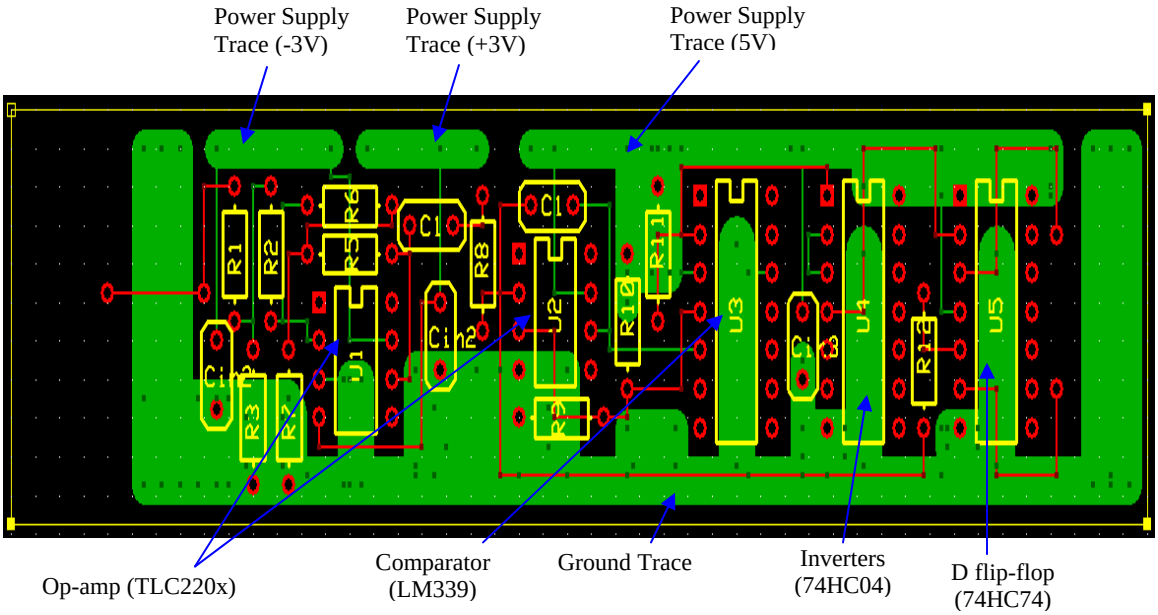


Figure 6.7 PCB layout of the sensing circuit

Figure 6.8 shows the test setup and the assembled PCB of the sensing circuit connected to the faraday plate of Boise state university's (BSU's) IMS. As we can see in Figure 6.8, the total circuit was powered with three sets of batteries. Figure 6.8 also shows the connections for the input signal, coaxial cable for clock, digital output to the FPGA, and the output through the analog low pass filter of the sensing circuit. Figure 6.9 shows the detailed view of the sensing circuit PCB.

The output through the analog low pass filter can be seen in Figure 6.10 and the zoomed view of the RIP has been shown in Figure 6.11. Figure 6.10 shows an inverted

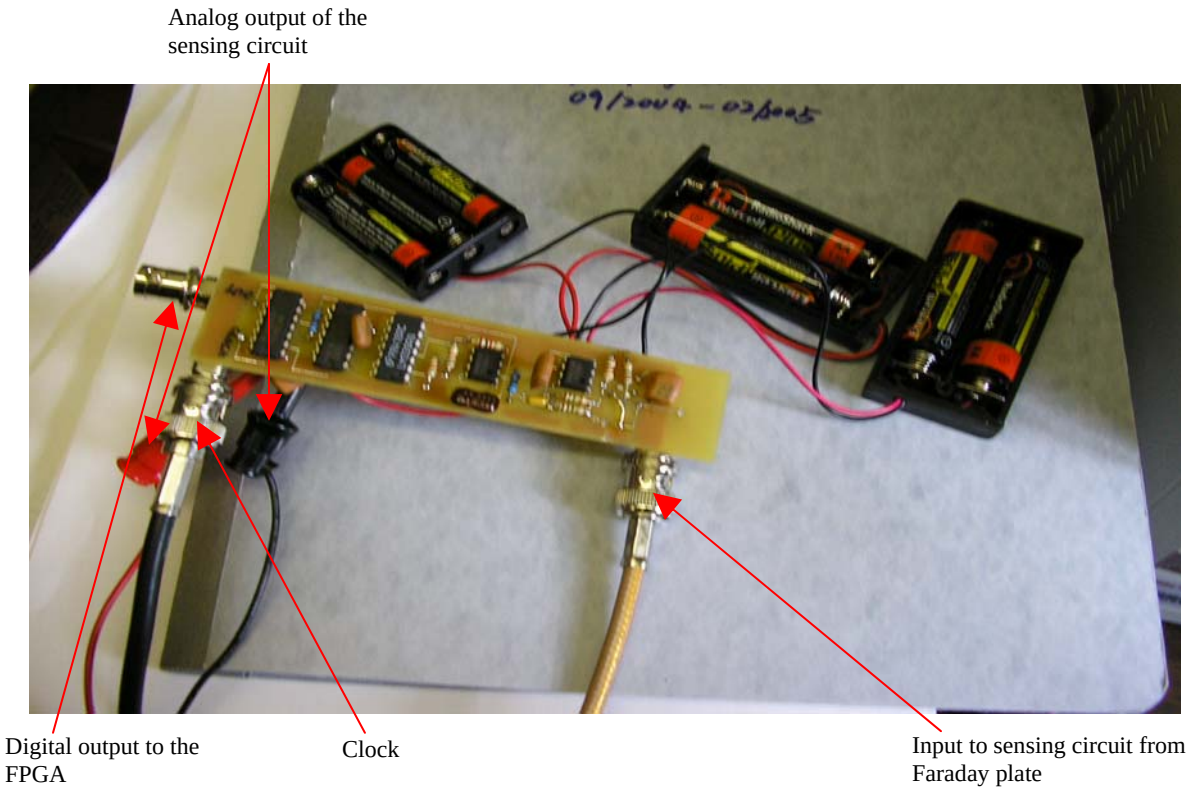


Figure 6.8 Test setup for the sensing circuit connected to the BSU's IMS [11]

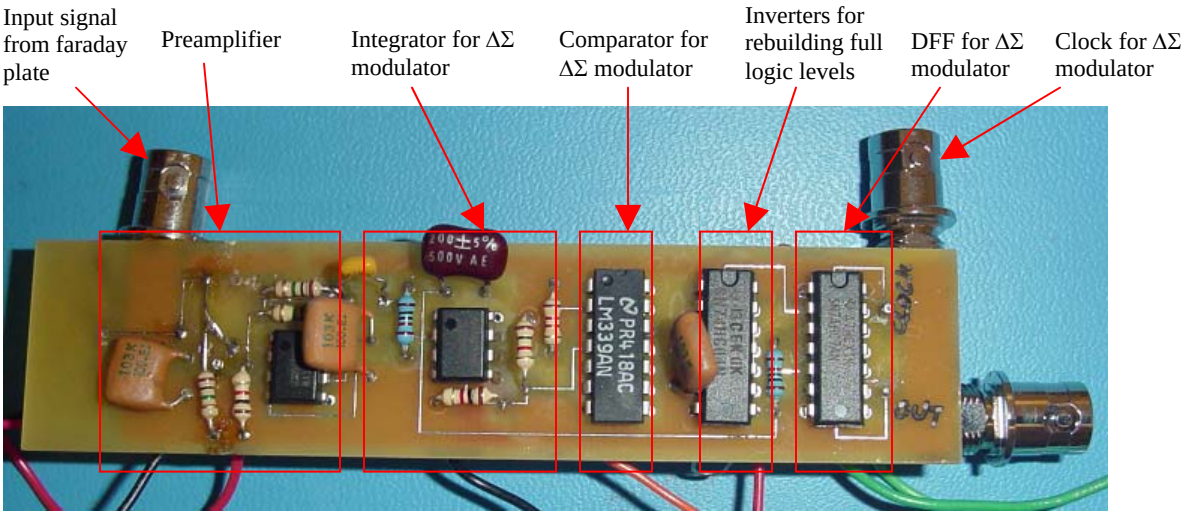


Figure 6.9 Zoomed view of sensing circuit PCB

RIP because the preamplifier is an inverting amplifier and the ΔΣ modulator isn't inverting the signal. So, the final output from the sensing circuit will be inverted. The amplitude measured on the oscilloscope was about 220mV, V_{PP}. This amplitude of the voltage corresponds to the amplitude of the current coming to the sensing circuit from the faraday plate of IMS.

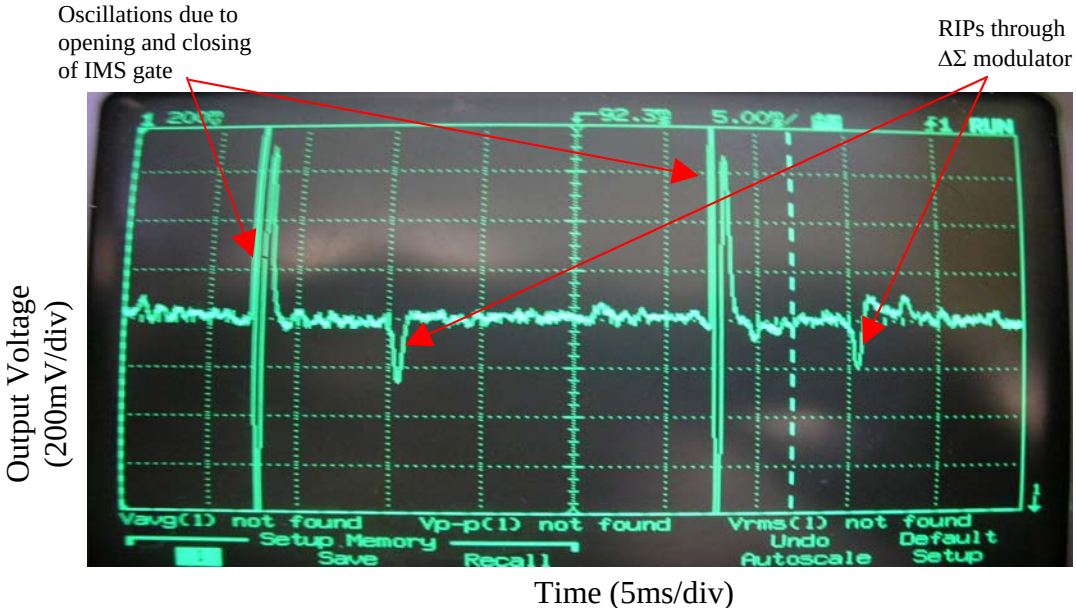


Figure 6.10 RIP from the BSU's IMS acquired after 64 averages using an oscilloscope [11]

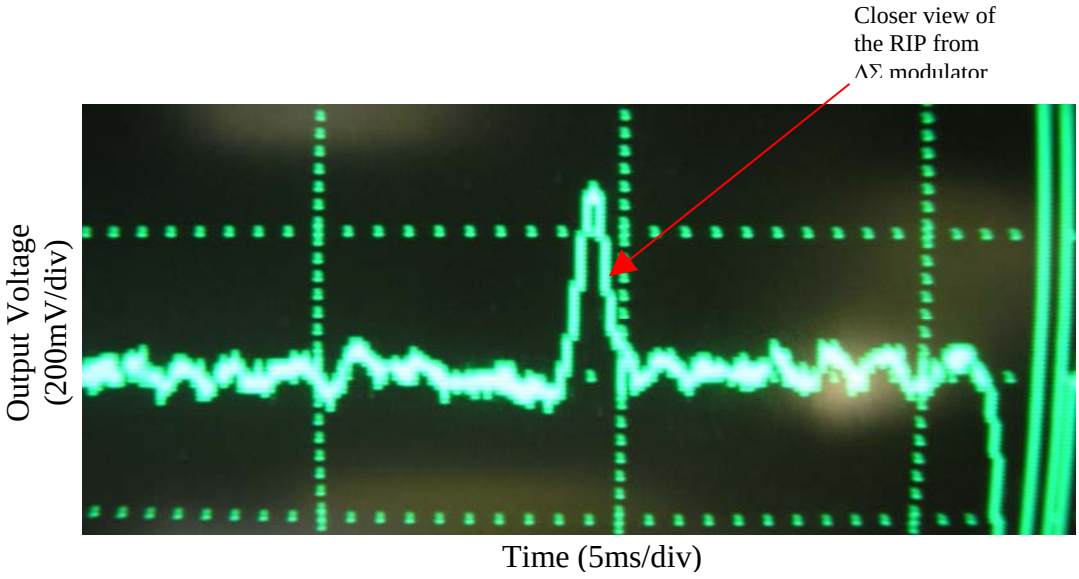


Figure 6.11 Closer (inverted) view of the RIP [11]

CHAPTER SEVEN: CONCLUSIONS, DRAWBACKS AND FUTURE WORK

Conclusions of the sensing circuit design are as follows:

- A prototype of the preamplifier circuit has been successfully built and tested to detect output currents from the IMS in the range of 0.1-3nA.
- Changing the loop gain of the preamplifier can program the detection of different current ranges. Else, the output voltage will saturate (maximum positive power supply is 3V).
- The bandwidth of the preamplifier was designed to be 1KHz, theoretically, and was about 800Hz, practically.
- The preamplifier for the IMS has been successfully built and tested with the IMS from Washington State University.
- In ΔΣ modulator circuit, the reference voltage (2.25V) appears as an offset voltage on the output. So, the base line for calculating the amplitude of the output voltage from the ΔΣ modulator circuit will be 2.25V.
- Both the preamplifier stage and the delta-sigma modulator have been integrated and tested to complete the basic prototype design for the sensing circuit.
- The sensing circuit has been integrated with the FPGA to test the correspondence of the digital output to the analog input from the IMS.

Future Work for this project:

- The circuit should be shielded for the protection from noises due to external devices in the surroundings.
- Whole sensing circuit can be re-fabricated using a 4-layer with both-side soldering and surface mount components for lesser noise and smaller area of PCB.
- Bigger fields of VDD and ground must me used for reducing noise effects. Separate grounds must be used for analog and digital circuitry in order to minimize the return currents from digital to analog circuits. Both the grounds should be connected with a thin path of metal.
- Decoupling bank of two capacitors (1nF and 10pF) should be used on all the VDD pins of different devices to minimize the noise effects.
- The bandwidth of the signal should be increased to sharpen the RIP from the preamplifier. This configuration should be tested with the IMS to ensure proper functionality.
- Regulators should be integrated with the sensing circuit for different power supplies we are using in preamplifier and ΔΣ modulator or change the power supply for the preamplifier circuit to 5V for reducing the number of regulators.
- Whole sensing circuit can be developed into an integrated circuit (IC) to minimize the area and enhance the performance.

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[9] R. Jacob Baker, CMOS Circuit Design, Layout and Simulation, first and second editions, John Wiley and Sons publishers, ISBN-81-203-1682-7 and ISBN-0-471-70055-X.

[10] R. Jacob Baker, CMOS MIXED-SIGNAL CIRCUIT DESIGN, John Wiley and Sons Publishers, ISBN-0-471-27256-6.

[11] Test of IMS and related electronics, Trip to WSU from 06/05/05 to 06/09/05.

APPENDIX

SPICE MODELS AND NETLIST

APPENDIX: SPICE MODELS AND NETLIST

1. Netlist for preamplifier stage

```
*** Preamplifier Circuit ****

.control
destroy all
run
set units=degrees
plot vout vin
*plot ph(vout)
*plot db(vout)
.endc

.tran 100n 10m
*.DC vin -3 3 1m
*.ac dec 100 .01 1G

Vdd1   Vdd1   0      DC     3
vdd2   vdd2   0      DC     -3
Vin    vin    0      DC     0      AC     sin 0 1 500

R1     Vin    V2     1meg
R2     V2     Vm     100k
R3     V2     0      1k
R5     V3     vout   1meg
R6     vm     V3     100k
R7     V3     0      1k
R8     vout   0      10k

Xamp   0      Vm     vdd1   Vdd2   Vout   TLC2201

* TLC2201 OPERATIONAL AMPLIFIER "MACROMODEL" SUBCIRCUIT
* CREATED USING PARTS RELEASE 4.03 ON 08/06/90 AT 15:18
* REV (N/A)     SUPPLY VOLTAGE: 5V
* CONNECTIONS:   NON-INVERTING INPUT
*              | INVERTING INPUT
*              | | POSITIVE POWER SUPPLY
```

```
*              | | | NEGATIVE POWER SUPPLY
*              | | | | OUTPUT
*              | | | | |
.SUBCKT TLC2201  1 2 3 4 5
*
 C1   11 12 11.00E-12
 C2    6  7 50.00E-12
 DC    5 53 DX
 DE   54  5 DX
 DLP  90 91 DX
 DLN  92 90 DX
 DP    4  3 DX
 EGND 99  0 POLY(2) (3,0) (4,0) 0 .5 .5
 FB 7 99 POLY(5) VB VC VE VLP VLN 0 537.9E3 -50E3 50E3 50E3 -50E3
 GA    6  0 11 12 282.7E-6
 GCM 0  6 10 99 2.303E-9
 HLIM 90  0 VLIM 1K
 ISS   3 10 DC 125.0E-6
 J1   11  2 10 JX
 J2   12  1 10 JX
 R2    6  9 100.0E3
 RD1  60 11 3.537E3
 RD2  60 12 3.537E3
 RO1   8  5 188
 RO2   7 99 187
 RP  3 4 5.71E3
 RSS  10 99 1.600E6
 VAD  60 4 -.5
 VB    9  0 DC 0
 VC 3 53 DC .928
 VE   54  4 DC .728
 VLIM  7  8 DC 0
 VLP  91  0 DC 2.800
 VLN   0 92 DC 2.800
.MODEL DX D(IS=800.0E-18)
.MODEL JX PJF(IS=500.0E-15 BETA=1.279E-3 VTO=-.177)
.ENDS
.end
```

2. Netlist for ΔΣ modulator stage

Simulation netlist for figures 5.2, 5.5, 5.6, and 5.7

```
.tran 2n 10u 0 2n UIC

* SPICE command scripts
.control
destroy all
run
plot Vout Vin
let Vqev=Vout-Vin
*plot Vqev
linearize Vqev
spec 0 10MEG 100k Vqev
let Vqedb=db(Vqev)
plot Vqedb ylimit -80 0
let m=mag(Vqev)
let Vqepsd=db(m*m/100k)
plot Vqepsd
.endc

*Input power and references
VDD VDD 0 DC 4.5
Vtrip Vtrip 0 DC 2.25
VCM VCM 0 DC 2.25

*Input Signal
Vin    Vin   0 DC 0 Pulse 0 4.5 0 10u

*Clock Signals
Vphi1  phi1  0 DC 0  Pulse 0 4.5  0  200p  200p  50n 101.25n
R1 vinm vin 10meg
R2 vinm vout1 10meg
R3 phi2 0 1MEG

*Use a VCVS for the op-amp
Eopamp Voutop 0 VCM Vinm 100MEG

*Setup switched capacitors and load
CF Voutop Vinm 200p
```

```
*clocked comparator implementation

XSH VDD     Vtrip   Voutop          Outsh   phi1    SAMPHOLD
S6 VDD Vout  Vcm   Outsh switmod


S7 Vout  0      Outsh Vcm   switmod

.model switmod SW RON=0.1

* Ideal Sample and Hold subcircuit
.SUBCKT             SAMPHOLD  VDD   Vtrip   Vin     Vout    CLOCK
Ein     Vinbuf 0        Vin     Vinbuf 100MEG
S1      Vinbuf  VinS   VTRIP CLOCK         switmod
Cs1     VinS    0       1e-10
S2      VinS    Vout1  CLOCK        VTRIP switmod
Cout1   Vout1  0       1e-16
Eout    Vout    0       Vout1  0       1
.model switmod SW
.ends

Mn      vout1   vout    0       0       cmosn L=2u W=3u
Mp      vout1   vout    vdd     vdd     cmosp L=2u W=9u

* Level 2 model nchan model for CN20
.MODEL CMOSN NMOS LEVEL=2 PHI=0.600000 TOX=4.3500E-08 XJ=0.200000U
TPG=1
+ VTO=0.8756 DELTA=8.5650E+00 LD=2.3950E-07 KP=4.5494E-05
+ UO=573.1 UEXP=1.5920E-01 UCRIT=5.9160E+04 RSH=1.0310E+01
+ GAMMA=0.4179 NSUB=3.3160E+15 NFS=8.1800E+12 VMAX=6.0280E+04
+ LAMBDA=2.9330E-02 CGDO=2.8518E-10 CGSO=2.8518E-10
+ CGBO=4.0921E-10 CJ=1.0375E-04 MJ=0.6604 CJSW=2.1694E-10
+ MJSW=0.178543 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -4.0460E-07

* Level 2 model pchan model for CN20
.MODEL CMOSP PMOS LEVEL=2 PHI=0.600000 TOX=4.3500E-08 XJ=0.200000U
TPG=-1
+ VTO=-0.8889 DELTA=4.8720E+00 LD=2.9230E-07 KP=1.5035E-05
+ UO=189.4 UEXP=2.7910E-01 UCRIT=9.5670E+04 RSH=1.8180E+01
+ GAMMA=0.7327 NSUB=1.0190E+16 NFS=6.1500E+12 VMAX=9.9990E+05
```

```
+ LAMBDA=4.2290E-02 CGDO=3.4805E-10 CGSO=3.4805E-10
+ CGBO=4.0305E-10 CJ=3.2456E-04 MJ=0.6044 CJSW=2.5430E-10
+ MJSW=0.244194 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -3.6560E-07
```

Simulation netlist for figure 5.4:

```
.tran 100k 32MEG UIC
* SPICE command scripts
.control
destroy all
run
plot noise xlimit 0 35E6
.endc

*set up frequency on the x-axis
Itime f 0 DC -1
Ctime f 0 1 IC=0
Rtime f 0 100G

*plot equation 32.10
Bnoise noise 0 V=((1.5^2)/(6*32E6))*(1-cos(2*pi*v(f)/32E6))
Rnoise noise 0 100G

.end
```