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Sensitivity Analysis of Medium Frequency Transformer Designs for Solid State Transformers

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***Abstract*—This paper discusses the technical challenges and trade-offs tied to design of medium frequency transformers for medium-voltage high-power applications and emerging solid state transformers. A dedicated design optimization algorithm is used to generate the set of all feasible transformer designs for the given electric requirements, originating from a modular DC-DC solid state transformer, and taking into account different geometry ratios, materials and operating frequencies. All possible design choice variations are compared in terms of maximum achievable efficiency, gravimetric and volumetric power density, identifying design limits for a given set of input parameters. Impact of modularity and choice of operating frequency directly related to selected semiconductors, reveal interesting trends that can aid overall solid state transformer design optimization.**

***Index Terms*—MFT, power electronics, design, optimization**

NOMENCLATURE

A_p	MFT area product
AWG	Litz wire strand AWG
B_m	Peak flux density
B_{sat}	Saturation flux density
C_r	Series resonant tank capacitance
Δ	Penetration ratio
I_{in}	Nominal current at SRC cell input
I_{out}	Nominal current at SRC cell output
I_{max}	Rated semiconductor current
I_{off}	Semiconductor turn-off current
J	Current density
K_f	Excitation waveform coefficient
K_u	Window utilization coefficient
K_{pd}	PD test voltage front multiplier
K_s	Dielectric distance safety coefficient
K,α,β	Steinmetz coefficients
L_m	MFT magnetization inductance
L_σ	MFT leakage inductance
L_r	Total series resonant tank inductance
M	Number of parallel connected SRC cells
N	Number of series connected SRC cells
P_n	MFT nominal power
P_{tot}	Total ISOP converter rated power
R_σ	MFT total series resistance
Q	SRC quality factor
V_b	Semiconductor rated blocking voltage
V_{MVDC}	Voltage at MVDC side of the ISOP converter
V_{LVDC}	Voltage at LVDC side of the ISOP converter
V_{in}	Voltage at the input of the SRC cell
V_{out}	Voltage at the output of the SRC cell
d_{wic}	Minimum i^{th} winding to core dielectric distance
d_{wiwj}	Minimum i^{th} to j^{th} winding dielectric distance
f_{sw}	Switching frequency
f_0	Resonant frequency
n	MFT primary to secondary turns ratio
u	Semiconductor blocking voltage utilization factor
μ_r	Relative magnetic permeability
ρ	Specific density
λ	Thermal conductivity

The initial version of this paper has been presented at IPEC 2018 in Niigata and has been substantially extended.

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I. INTRODUCTION

Novel high-power medium-voltage converter technologies offering galvanic insulation are needed to support the development of the emerging medium voltage DC (MVDC) grids and further improve performances in various other applications such as traction [1]. With the recent advancements in the power semiconductor industry, resulting in faster and more efficient switches with extended voltage and current capabilities, these converters, often referred to as solid state transformers (SSTs) or power electronic transformers (PETs), have become increasingly attractive.

Due to the limited blocking voltage capabilities of the existing power semiconductors, most of the proposed solutions from the literature employ some sort of an input series output parallel (ISOP) structure, featuring multiple identical converter cells, to allow the connection to MV, as displayed in Fig. 1a. The most popular ISOP converter structures are based on multiple stages of either series resonant converter (SRC) or dual active bridge (DAB) topologies, as shown in Fig. 1b and Fig. 1c, respectively. As can be seen, besides the power semiconductor modules, the central component of any such switched-mode DC-DC power supply topology is the medium frequency transformer (MFT), providing both the galvanic insulation and input-output voltage matching.

In contrast to traditional line frequency transformers (LFTs), normally operating at low grid frequency with sinusoidal voltage and current excitation, MFTs operate on higher switching frequencies with square voltage and, in general, non-sinusoidal current waveforms characteristic for the given power electronic converter topology. This has implications on MFT losses and dielectric withstand requirements. Moreover, correct design of electric parameters is essential for proper operation of these converters and therefore imposes strict requirements on the accuracy of the corresponding models [2].

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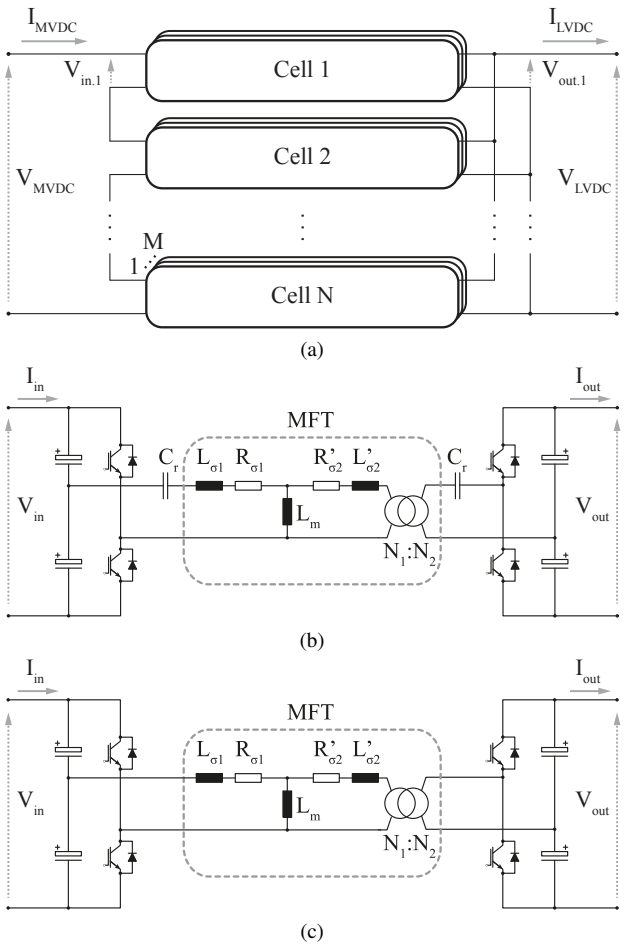

Fig. 1. (a) ISOP connection of DC-DC converter topologies commonly used within SSTs: (a) SRC converter (b) DAB converter

The main motivation for operating a transformer at high frequency is the potential for decrease in size, according to approximate relation (1) [3].

$$A_p \approx \frac{P_n}{K_f K_u B_m J f_{sw}} \tag{1}$$

This has many positive implications: easier integration, less material utilization, lower investment cost and environmental footprint etc.

These technologies have already been deployed in low-voltage low-power applications with great success, achieving the expected power densities. However, the increased dielectric withstand and power processing requirements, characteristic for aimed MV applications, affect the maximum achievable scaling. Size decrease implies decreased cooling surfaces resulting in higher temperature gradients unless additional cooling effort is introduced [4]. Depending on the application requirements, different design choices have direct impact on MFT characteristics.

Moreover, different DC-DC converter topologies impose different requirements for MFT electrical parameters and operation conditions. The analysis presented in this paper focuses on different implications on the MFT design for a SRC based ISOP DC-DC converter structure, as displayed in Fig. 1. Note that the conclusions are transferable to any AC or DC input-output combination of the ISOP structure, as the AC input or output would only imply the addition of active front-end or inverter stage to the SRC cell shown in Fig. 1b without significantly influencing the MFT specifications. The only difference being the type of experienced dielectric stress: high voltage DC with superimposed high frequency AC PWM in case of DC-DC/AC SST and low frequency high voltage AC with superimposed high frequency AC PWM in case of AC-DC/AC SST.

The research interest in the area has intensified recently, both in academic and industrial domain, dealing with modeling and overall design optimization of the MFT [5]–[9] and specific design challenges such as insulation coordination [10] or multi-winding design [11]. Several MFT prototype examples have been presented: litz wire / solid / metglas / 25 kW / 2 kHz [5], litz wire / nanocrystalline and ferrite / 166 kW/20 kHz [6], litz wire / nanocrystalline and ferrite /50 kW / 5 kHz [7], litz wire / ferrite / 100 kW / 10 kHz [8], litz wire / nanocrystalline / 240 kW / 10 kHz [10], litz wire / nanocrystalline / 100 kW / 15 − 22 kHz [11]. Even though these MFT prototypes have all been custom made for various technical requirements, it is possible to identify the most popular materials and design choices. These form the base design space for this study.

Compared to the mentioned state of the art, dealing with various challenges of the MFT design for defined requirements, this work looks into the MFT design optimization from the aspect of the whole converter. Design degrees of freedom of the ISOP converter, as shown in Fig. 1a, and their impact on the resulting MFT specifications are analyzed. While an analysis, attempting to find the optimal number of cascaded cells of the AC-DC ISOP converter from the aspect of the MVAC input active rectifier stage has been performed in [12], this paper tackles a similar problem from a DC-DC converter cell point of view. Considering the most relevant materials and design choices reoccurring in the literature, the MFT design is optimized in function of the ISOP converter modularity. A comparative analysis of various design choices is performed in terms of efficiency and power density, providing an overview of the dominant solutions and insight into the overall optimal design choice coordination.

An MFT is a complex system with coupled multi-physics which makes understanding the effects of certain design changes rather abstract and difficult to grasp. This work discusses in detail the trends and different design outcomes in both qualitative and quantitative sense. Impact of different parameters is analyzed in a structured and intuitive manner thus exposing different design trade-offs, potential gains and expectation limitations.

This paper is organized as follows: Section II presents the design of a SRC based ISOP converter structure, as shown in Fig. 1, describing the design degrees of freedom and their impact on the MFT requirements. A qualitative scaling analysis of the MFT design is presented in Section III, revealing the design trade-offs for the resulting different MFT ratings. Section IV introduces a methodology that allows to quantify the potential improvements of the MFT design in terms of size and efficiency, using a sophisticated model-

based design-optimization algorithm and identifies the optimal design alternatives. Section VI provides a discussion and summary of the main findings.

II. Converter Design

A. Selection of the number of cells

Depending on the electrical ratings, nominal power and input-output voltages, the number of DC-DC converter cells connected in ISOP configuration (N), as shown in Fig. 1, represents a design choice related to voltage class of selected semiconductors. Moreover, each of the cells can as well be realized as a parallel connection of multiple cells (M), depending on the current ratings of selected semiconductors. All of the cells are equally sharing the high voltage at MV side, high current at the low voltage side and power, according to (2), (3) and (4), respectively.

$$V_{in} = \frac{V_{MVDC}}{N} \quad \text{and} \quad V_{out} = V_{LVDC} \tag{2}$$

$$I_{in} = \frac{I_{MVDC}}{M} \quad \text{and} \quad I_{out} = \frac{I_{LVDC}}{NM} \tag{3}$$

$$P_n = \frac{P_{tot}}{NM} \tag{4}$$

The feasible alternatives are limited by the voltage and current ratings of the available semiconductors. The maximum blocking voltage of the selected semiconductor devices on the primary side (V_b) and current ratings of the semiconductors on the secondary side (I_{max}) must satisfy the relation (5).

$$V_b > \frac{V_{MVDC}}{uN} \quad \text{and} \quad I_{max} > \frac{I_{LVDC}}{NM} \tag{5}$$

Various design alternatives, depending on the selected semiconductor blocking voltages are summarized in Table I. This table considers the standard ratings of the contemporary semiconductor devices readily available on the market as well as the projection for the emerging future semiconductors with extended blocking voltage capabilities, such as the $10\,\mathrm{kV}$ SiC, marked in gray, and mostly available as engineering samples.

TABLE I: Number of Cascaded DC-DC Converter Cells Depending on Selected Semiconductor Blocking Voltage for $V_{MVDC} = 10\,\mathrm{kV}$ and Maximum Switching Frequency

V_b [kV]	N	V_{in} [kV]	u [p.u.]	f_{sw} [kHz]
1.7	11	0.91	0.53	25 (50)
3.3	6	1.67	0.51	10
4.5	4	2.5	0.56	5
6.5	3	3.33	0.51	1
10	2	5	0.5	/
20	1	10	0.5	/

u is the semiconductor blocking voltage utilization factor, normally up to 50%-60% [13]. Marked in gray are the emerging SiC based semiconductors with extended blocking voltage capabilities (not yet fully commercially available). Shown in brackets are the SiC modules already available on the market.

As can be seen, there exist various design alternatives, utilizing different number of DC-DC converter cells with differently rated semiconductors to share the high input voltages and output currents. Each of these solutions imposes different electrical ratings on the DC-DC converter cell resulting in different sizing of the passive components.

B. Cell Design

The design of the resonant tank of the SRC, as shown in Fig. 1b, can be performed based on the desired operating mode and selected quality factor (Q). Using the first harmonic approximation, the equivalent nominal-load resistance refereed to the primary side of the transformer can be calculated according to (6).

$$R_{ac1} = \frac{2n^2 V_{out}^2}{\pi^2 P_n} \tag{6}$$

The reference values for the series resonant capacitance and inductance can be calculated with (7) and (8), respectively

$$C_r = \frac{1}{2\pi f_0} \frac{1}{QR_{ac1}} \tag{7}$$

$$L_r = \frac{1}{2\pi f_0} QR_{ac1} \tag{8}$$

where

$$f_0 = 1.2 f_{sw} \tag{9}$$

is the desired resonant frequency. It is set 20% above the switching frequency to achieve sub-resonant operation, where the turn-off current of the primary side switches is limited to relatively small MFT magnetizing current, whereas the secondary side diode current is reduced to zero, thus eliminating reverse recovery losses. Quality factor is set to 0.1 to ensure a resonant tank characteristic that will result in a large zero voltage switching (ZVS) region within the sub-resonant frequency range, hence ensuring the soft turn-on of the active switches at the intended operating point.

The reference magnetizing inductance of the resonant tank is designed to limit the maximum magnetizing current to the desired active switch turn-off current (I_{off}) according to equation (10).

$$L_m = \frac{V_{out} n}{8 f_{sw} I_{off}} \tag{10}$$

Combining (2), (3),(4), (6), (8), (9) and (10), the reference parameters of the MFT within each SRC cell, leakage and magnetizing inductance refered to the primary side, can be expressed in function of the total converter ratings and the number of cells with (11) and (12), respectively.

$$L_r = \frac{Q}{1.2\pi^3} \frac{MV_{MVDC}^2}{N f_{sw} P_{tot}} \tag{11}$$

$$L_m = \frac{1}{8 I_{off}} \frac{V_{MVDC}}{N f_{sw}} \tag{12}$$

The last two equations show the influence of both design variables, operation frequency and modularity, on the reference leakage and magnetization inductance of the MFT, imposed by the converter.

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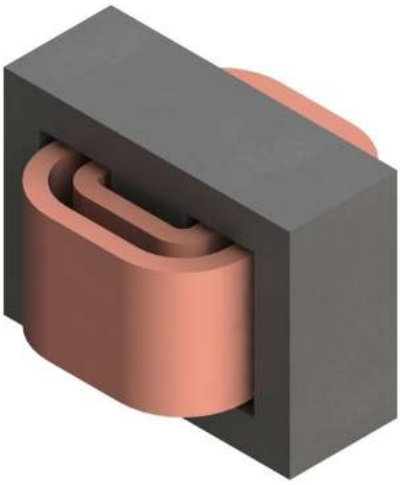
TABLE II: MFT Scaling Laws For Constant Material Utilisation - Magnetic Flux And Current Density

Variable	**Formula**	**Proportion**	**Simplified Generic Shell MFT Structure**
Cooling Surface	$S_c = C_1 l^2$	k^2	
Volume and Mass	$M = \gamma V = C_2 l^3$	k^3	
Current	$I = J S_{Cu}$	k^2	
Induced Voltage	$U = C_3 f_{sw} B_m S_{Fe}$	$f_{sw} k^2$	
Apparent Power	$P = UI$	$f_{sw} k^4$	
DC Resistance	$R_{DC} = N\rho l / S_{Cu}$	$1/k$	
Copper Losses	$P_{Cu} = F(f_{sw}) R_{DC} I^2$	$F(f_{sw}) k^3$	
Core Losses	$P_{Fe} = K f_{sw}^a B_m^b V$	$f_{sw}^a k^3$	
Temperature Rise	$\Delta\theta = (P_{Cu} + P_{Fe})/(\alpha S_c)$	$k(F(f_{sw}) + f_{sw}^a)$	
Relative Losses	$P_r = (P_{Cu} + P_{Fe})/P$	$(F(f_{sw}) + f_{sw}^a)/(k f_{sw})$	
Relative Cost	$\epsilon = M/P$	$1/(k f_{sw})$	

Where: l, k - spatial dimensions, C_i - proportionality constants, γ - MFT density, $F(f_{sw})$ - skin and proximity effect correction factor

III. Qualitative Analysis of MFT Design Trade-Offs

The approximate relation (1) provides a very simplified estimation of the transformer size, in function of electric requirements and selected design alternatives, suitable for fast design. However, it does not show the effects on the MFT internal characteristics such as temperature gradients and relative cost. A more comprehensive step-by-step qualitative analysis of the scaling laws of each variable characterizing the MFT in mechanical and electric sense, under the assumption of equal material utilization in terms of current and flux densities, is described in Table II.

Starting from basic relations such as calculation of arbitrary MFT surfaces, volume and weight, it is possible to derive the scaling laws for more complex characteristics which are not so intuitively obvious, such as temperature rise, relative losses and relative cost. As can be seen, the relative cost is reverse proportional to both size and frequency. Therefore, from the material quantity and cost point of view, high power MFTs appear more attractive than their smaller counterparts.

However, it can be seen that the temperature rise is proportional to the linear spatial dimension and the sum of the additional winding ($F(f_{sw})$) and core (f_{sw}^a) loss correction factors associated to high frequency effects. Consequently, the temperature gradients increase with the increase of transformer size (processing power), as well as the frequency. Depending on the type of insulation, additional insulation reinforcement may as well substantially increase the thermal resistances towards the ambient (e.g. solid type insulation). Therefore, the frequency, power processing and voltage domain where the described scaling can be preserved without additional cooling effort is limited.

On the other hand, relative losses decrease reversely proportional to size increase, indicating that higher power rated transformers should yield better efficiency. The frequency dependency is a function of winding ($F(f_{sw})$) and core (f_{sw}^a) loss frequency correction factors. The frequency exponent of core materials, $a > 1$, and therefore the relative core losses increase with the frequency increase in the amount depending on the material properties. Skin and proximity correction factor ($F(f_{sw})$) is negligible for low frequencies ($\Delta < 1$), but increases exponentially at higher frequencies ($\Delta > 1$) [5]. Therefore, relative winding losses have a minimum at some frequency where penetration ratio is around one. Consequently, depending on the core material properties, and loss distribution between the core and the windings, the total relative losses are a convex function of frequency either having a minimum point or an increasing trend in the entire frequency range, depending on the initial gradient.

There are many coupled effects that influence the scaling of the MFT, making it a rather difficult task to map the domain of possible designs or fairly assess the design improvement potential of each design choice on its own.

IV. Quantitative Analysis of MFT Design Trade-Offs

This section provides a method of analyzing the MFT design trade-offs in an integral manner, using a sophisticated MFT design tool. The focus of the analysis is on the influence of the ISOP converter modularity on the maximum achievable MFT characteristics for various design choice alternatives. The electric specifications of the ISOP converter, chosen for the case study, are summarized in Table III.

TABLE III: Total Converter Electric Specifications

P_{tot}	V_{MVDC}	V_{LVDC}
500 kW	10 kV	750 V

TABLE IV: Core Material Characteristics at 100 °C [6], [14], [15]

Core Material	B_{sat} [T]	K [kW/m^3]	α	β	ρ [kg/m^3]	λ [W/mK]
Si-Ferrite N87	0.39	$1.6{\cdot}10^{-3}$	1.42	2.16	4850	4
Nanocrys-talline	1.17	$3.6{\cdot}10^{-5}$	1.64	2.10	7330	1.5 (8)

Two different thermal conductance values, in normal and parallel direction to nanocrystalline sheets are considered to properly take into account the anisotropy of the nanocrystalline cores

TABLE V: Dielectric Material Characteristics [10]

Material	V_d [kV/mm]	k_s	ρ[kg/m^3]	λ[W/mK]
Air	3	4	0	/
Epoxy	45	3	500	0.25

k_s is a dielectric safety margin multiplicative factor

A. Scope Of The Analysis

The considered design is a litz wire, natural air convection cooled shell type MFT with enhanced cooling at the top and bottom surfaces of the core, as shown in Fig. 3b. While the main transformer structure is fixed, two different core materials and insulation strategies, typically reoccurring in the literature, are analyzed.

The considered core materials are Si-Ferrite N87 and nanocrystaline, as the most common materials of choice for MFT prototypes documented in the literature, depending on the switching frequency range. The assumed material characteristics, used in the study are summarized in Table IV.

ISOP connection requires for each MFT to be insulated for full working voltage of 10 kV. This requirement, combined with the high frequency stress with high dV/dt makes the proper MFT insulation coordination a rather challenging problem. Two different insulation strategies are considered: air insulation (litz wire winding in the air [8]) and solid insulation (litz wire winding cast in epoxy resin in the air [10]). Considered dielectric characteristics of the mentioned materials are summarized in Table V.

Proper MV MFT insulation coordination is not a straightforward task and it depends on many different details (e.g. local electric field grading) which are not easy to take into account at the optimization stage. However, for design comparison purposes, without the loss of generality, it can be claimed that, depending on the chosen insulation material, higher blocking voltage requirements (V_i) will yield larger dielectric distances (d_i), proportional to the corresponding dielectric strength (V_b) according to

$$d_i \approx k_s k_{pd} \frac{V_i}{V_b} \tag{13}$$

where k_{pd} is a PD test standard voltage front multiplier from IEC 60664-1 international standard and ($k_s > 1$) is a multiplicative safety margin factor that takes into account the imperfections, degradation and pollution in non-laboratory conditions (it is down to a designer to decide). Especially high safety margin values must be taken into account for any design with air due to the possibly high dust or moisture content causing local field anomalies that can lead to Partial Discharge (PD).

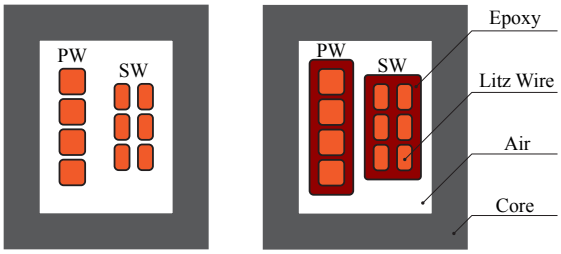


Fig. 2. Two considered insulation concepts: (a) Square litz wire windings without any added external insulation besides the strand enamel and outer silk binder, held in place with a coil former; (b) Square litz wire windings separately cast in epoxy resin, mechanically held by the the strength of the cast itself

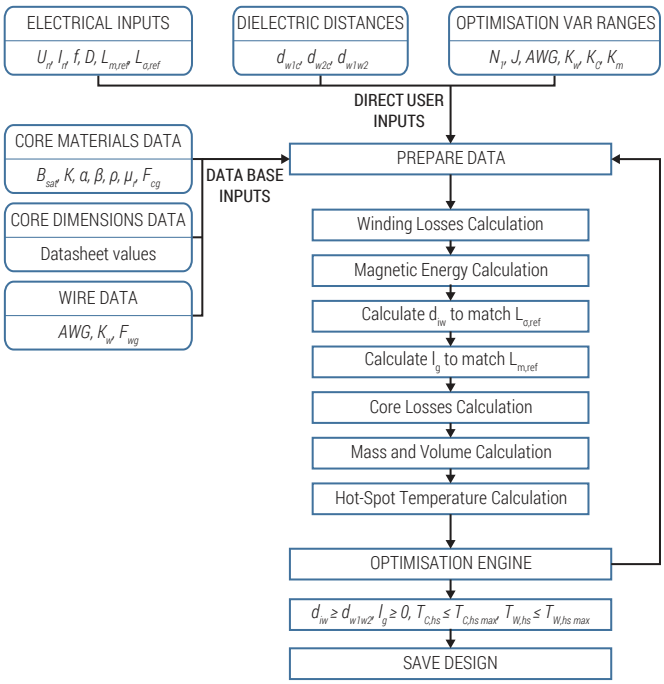
Air insulated design assumes litz wire windings without any added external insulation besides the strand enamel and outer silk binder, as shown in Fig. 2a. In order to maximize the cooling efficiency, they are mechanically held by a specially designed coil former (not visible in Fig. 2a) that allows natural air convection from almost entire winding surface, as presented in [8]. The minimum air dielectric distances (clearances) are calculated according to (13). Similarly, solid insulated design assumes litz wire windings, each separately cast in epoxy resin to minimize the mechanical stress on the cast due to the thermal expansion of different parts [10], mechanically held by the the strength of the cast itself, as displayed in Fig. 2b. Even though the minimum width of the epoxy coating is calculated for full voltage according (13), additional small air clearances are assumed to maximize the natural air convective cooling and allow for easy assembly.

Note that despite being an interesting design alternative, oil based designs have not been considered in this study as they in general require additional expansion vessels and radiators [11] or some other type of external heat exchanger [16] which make a fair design comparison very difficult, unless these are properly taken into account as well.

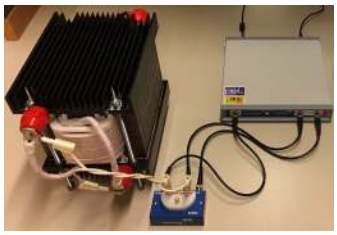
All of the aforementioned design alternatives are systematically analyzed using a sophisticated MFT design optimization tool.

B. Method of Analysis

A model based brute force MFT design optimization algorithm, capable of generating sets of all feasible MFT designs for given electric and dielectric specifications, as illustrated in Fig. 3, has been presented and experimentally verified in detail on a 100 kW, 10 kHz, 2 kV, N87 Si-ferrite core MFT prototype [8] confirming the high accuracy of the utilized improved models and flexibility of the overall proposed methodology. For the purposes of this analysis, the mentioned methodology



(a)



(b)

(c)

Fig. 3. (a) A brute-force model-based MFT design optimization algorithm [17]; (b) Measurement of the optimal MFT prototype electric parameters using Bode 100 vector network analyzer [2]; (c) Thermal camera image of the MFT prototype at full load steady state operation [4]

is used to map various design choice influences and trade-offs.

All geometry ratios and relative field densities, as described by Fig. 4 and Table VI, are considered as optimization variables whose each variation fully defines one MFT design. The maximum allowed hot-spot temperatures of the windings and the core are selected as 150 °C and 100 °C, respectively, corresponding to the selected material properties.

As described in more detail in [8], [17], the algorithm takes the available data-sheet inputs, electrical and dielectric references and optimization variables ranges. The ”prepare data” function generates the optimization space where each optimization variable vector variation corresponds to a fully defined single design. Winding losses and magnetic energy are calculated using [2], [18]. Dielectric distance between the windings is calculated to match the reference leakage inductance based on the magnetic energy calculation. Air gap is calculated to match the magnetization inductance reference. Core losses [19], mass and volume calculation is performed and finally the hot-spot temperatures are generated utilizing a sophisticated thermal network model [4]. Each design that

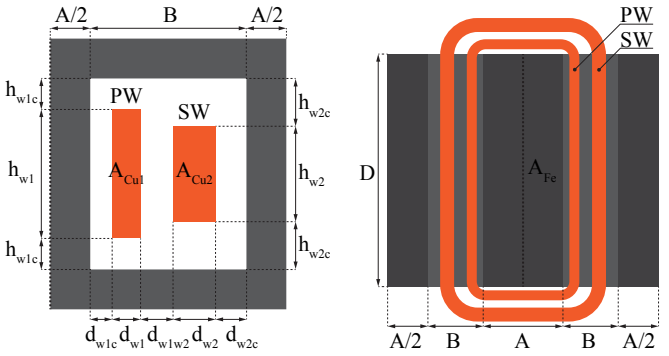


Fig. 4. Definition of generalized MFT geometry for parametric optimization: a) vertical cross section, where A_{Cui} denote the geometric winding cross-section area (copper and inter winding, turn-to-turn, insulation), whereas the total winding to winding (d_{w1w2}) and winding to core (d_{wic} and h_{wic}) distances include the solid insulation around the winding (in case of solid insulated) and air spacing; b) horizontal cross section, where A_{Fe} denotes the geometric core cross-section area

TABLE VI: Definition of Optimisation Varable Ranges For Parametric Optimisation According to Generalized MFT Geometry Definition in Fig. 4

Optimization Variable	Definition	Range	Unit
PW number of turns	N_1	$1-50$	/
PW Current Density	$J_{m1}=\frac{I_n}{A_{Cu1}}$	$0.5-6$	$\frac{\mathrm{A}}{\mathrm{mm}^2}$
SW Current Density	$J_{m2}=\frac{I_n}{A_{Cu2}}$	$0.5-6$	$\frac{\mathrm{A}}{\mathrm{mm}^2}$
Magnetic Induction	$K_m=\frac{B_m}{B_{sat}}$	$0.2-0.9$	p.u.
PW Geometric Ratio	$K_{w1}=\frac{d_{w1}}{h_{w1}}$	$0.05-0.5$	p.u.
SW Geometric Ratio	$K_{w2}=\frac{d_{w2}}{h_{w2}}$	$0.05-0.5$	p.u.
Core Geometric Ratio	$K_c=\frac{A}{D}$	$0.05-0.5$	p.u.
American Wire Gouge	AWG	32	/

PW and SW refer to primary and secondary windings, respectively

passes the feasibility check is saved into a design database. Similar to branch and bound strategy, the ”optimization engine” function utilizes certain heuristics to detect and avoid unnecessary waste of processing power on large infeasible design sets, thus increasing the execution speed and allowing the generation of more dense and higher quality design populations.

For each possible number of cascaded DC-DC converter cells (N) from Table I, core and insulation material combination, maximum feasible MFT design sets are generated for a family of frequencies in range from 0.5 kHz to 50 kHz in a logarithmic scale, as shown in Fig. 5. A comprehensive comparative analysis of these results is presented next, outlining the main effects and trade-offs while taking into account both the readily available power semiconductor modules on the market and exploring the potential benefit of the emerging future devices with extended blocking voltage and operating frequency range, as given in Table I.

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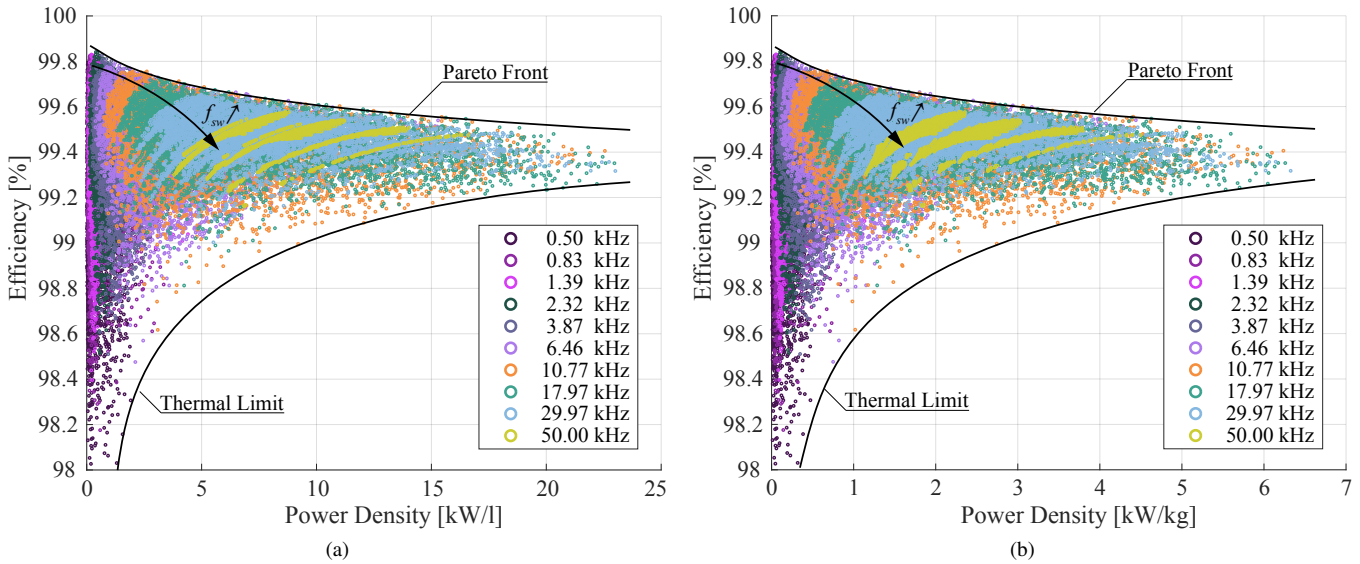

Fig. 5. Efficiency versus volumetric (a) and gravimetric (b) power density plots of all mathematically feasible MFT designs generated with design optimization algorithm for $N = 11$, $M = 1$, Si-Ferrite, Solid (around 12 million designs, uniformly down-sampled to 66000 for faster rendering). Designs are organized in color groups based on operating frequency. The MFT volume is defined as the minimum box which can be put around the active part of the transformer, core and the windings, as recommended metric for design comparison [20].

V. MFT Design Analysis

An example of the maximum feasible MFT design set, generated with the algorithm for $N = 11$, $M = 1$, Si-Ferrite, solid insulated MFT, is displayed in efficiency versus volumetric and gravimetric power density plots, as given in Fig. 5. These plots reveal the trend related to the influence of frequency increase on the disposition of the feasible MFT designs. The upper boundary of the feasibility sets represents the Pareto front corresponding to the trade-off between the efficiency and power density. On the other hand, the lower boundary is set by the thermal limitations, showing how, at the set boundary, a smaller design must have a higher efficiency in order to compensate for the decrease of the cooling surfaces and remain within the defined temperature limitations.

It can as well be seen how the feasible design sets at different frequencies reach the maximum achievable efficiency point at different power densities. The loss density within the core and the windings is higher at higher frequencies and therefore the increase of efficiency cannot be achieved by mere increase of their respective cross-sections. Therefore, with the increase of frequency, where additional loss density associated to high frequency effects is higher, maximum efficiency points are lowered and shifted towards higher power densities. Analyzing only the efficiency versus power density trade-off for any frequency, all of the designs which have lower power density than this critical value are sub-optimal as further increase of power density would allow for an increase in efficiency as well.

Beside these direct conclusions, with some simple post-processing of these feasible MFT design sets, it is possible to expose all sorts of complex design trends featuring compound constraints.

A. Switching Frequency and Efficiency

It is especially interesting to analyze the potential increase in power density that can be achieved with the increase of operating frequency under specified minimum efficiency constraint. This trend can easily be identified by means of filtering the maximum MFT design feasibility sets from Fig. 5 by minimum allowed efficiency criteria and selection of designs with maximum power density for each frequency.

The family of curves, representing maximum achievable gravimetric and volumetric power densities versus operating frequency, for different minimum efficiency constraints, are presented in Fig. 6. It can be seen that it is not possible to achieve the scaling such as estimated with (1) for higher frequencies. For each minimum efficiency constraint, there exists a Pareto optimal frequency at which the maximum achievable MFT power density is at its apex. For higher frequencies, the additional frequency dependent losses start to dominate, thus preventing further scaling. Furthermore, it can be seen that, as the minimum efficiency constraint is tightened, the maximum achievable power densities decrease, as well as the feasible design set frequency range. It is also interesting to notice that Pareto optimal frequencies are lower for MFT designs with higher efficiency requirement.

B. Switching Frequency and Insulation Voltage

Taking into account the assumptions described in Section IV-A, it is possible to perform a simplified analysis of the influence of the required insulation level, by comparing feasible MFT design sets with different minimum dielectric distance constraints, corresponding to different insulation voltage requirements, according to (13). An example of the maximum achievable gravimetric and volumetric power density versus operating frequency plots for different insulation requirements

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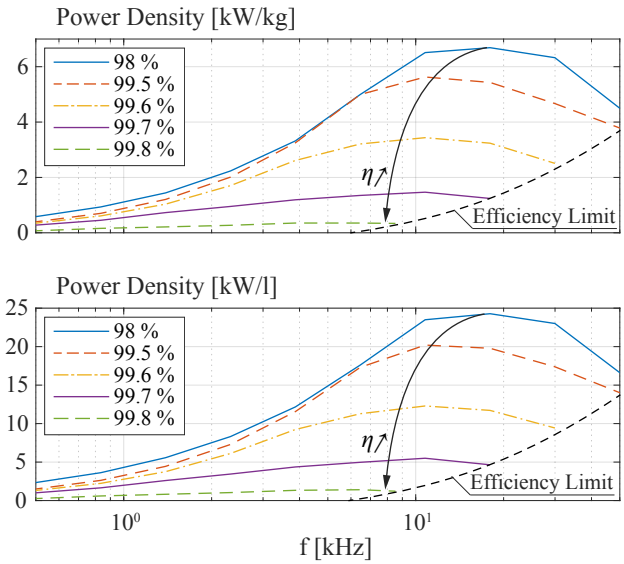

Fig. 6. Maximum achievable gravimetric (top) and volumetric (bottom) power density versus operating frequency plots for different minimum efficiency constraints for $N = 11$, $M = 1$, Si-Ferrite, solid insulated MFT

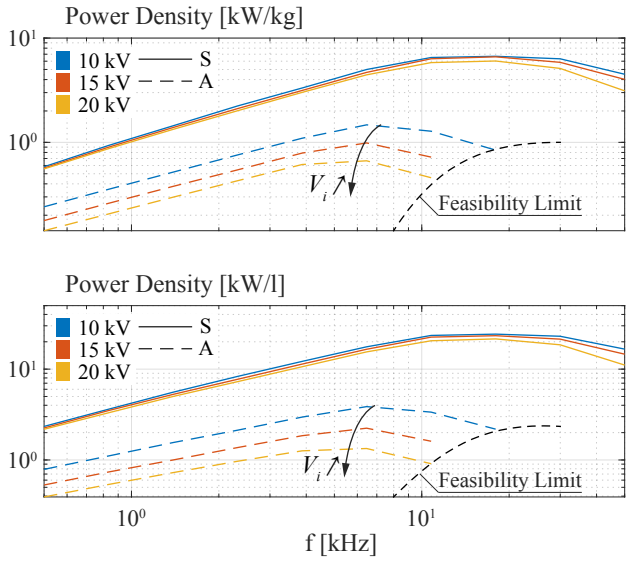

Fig. 7. Maximum achievable gravimetric (top) and volumetric (bottom) power density versus operating frequency plots for different insulation requirements for $N = 11$, $M = 1$, Si-Ferrite, solid (S) and air (A) insulated MFT

are displayed in Fig. 7, for $N = 11$, $M = 1$, Si-Ferrite MFT with both insulation alternatives. As can be seen, the maximum achievable power density is lower in case of the MFT design with higher insulation voltage. This is an expected result, as the higher insulation level requires larger dielectric distances and therefore more volume is occupied for this function.

Moreover, it can be seen that the air insulated design is much more sensitive to the increase of the insulation voltage compared to the solid insulated alternative. As given in Table V, epoxy resin has much better dielectric properties than air which lead to proportionally smaller increase in dielectric spacing, according to (13). Design optimization algorithm optimizes the active part of the transformer, windings and the core, whereas the minimum insulation distances must be respected for a chosen dielectric.

Consequently, dielectric properties of the insulation material determine the sensitivity of the volume and weight of the MFT design to the increase of insulation requirements. Air insulated designs will require large volume to accommodate MV applications, due to relatively poor dielectric properties of the air compared to epoxy, but they benefit from the inherent property of self healing and avoid relatively complex and expensive epoxy casting. While, air pollution and its varying properties are always a concern when it comes to air insulation, solid cast insulation suffers electrical, thermal and mechanical stress due to non equal expansion of various materials in contact which may, cause cracks over time. Moreover, any epoxy casting imperfections (e.g. bubbles) may cause sufficiently strong local field gradients that can cause PD and eventually annihilation of dielectric properties.

Provided that a reliable data base of various insulating materials is available, insulation coordination could as well be integrated into design optimization, thus allowing the selection of the most optimal alternative.

C. Optimal Number Of ISOP Connected Cells

As discussed earlier, some type of modular series connected structure is necessary on the MV side, depending on the selected power semiconductor module blocking voltages. Taking into account the variety of available semiconductor devices and projections for the future power modules with extended operation range, as listed in Table I, the number of ISOP connected DC-DC converter cells represents a design choice. Similar to operating frequency, this degree of freedom is analyzed from the aspect of potential MFT optimization. A maximum feasible design set is generated for all mentioned MFT design variations, for each possible number of ISOP cascaded cells from Table I, as given in Fig. 8.

It can be seen that the downward slope of Pareto-front, showing the trade-off between efficiency and power density, becomes steeper with the increase of the number of cascaded cells. Consequently, maximum achievable MFT efficiency, for a given power density, decreases with the increase of N. This result is in line with the qualitative analysis from Section III. Increase of N results in more DC-DC converter cells with lower power rating according to (4) and, as can be seen from Table II, relative losses are reverse proportional to MFT unit of size and indirectly to rated power.

It is interesting to notice how this trend is influenced by the insulation material. As can bee seen, the Pareto fronts of the air insulated designs are much more affected by the increase of N compared to solid insulated counterparts. This is due to the fact that the size of the active parts of the transformer, winding and core cross sections, decrease with the mentioned power decrease, whereas the dielectric distances must remain the same in order to accommodate full input voltage insulation of 10 kV regardless of N, as discussed in Section IV-A. Therefore, insulation occupies a higher relative portion of the MFT as the N increases. Higher relative dielectric distances cause larger relative mean lengths of the windings and magnetic

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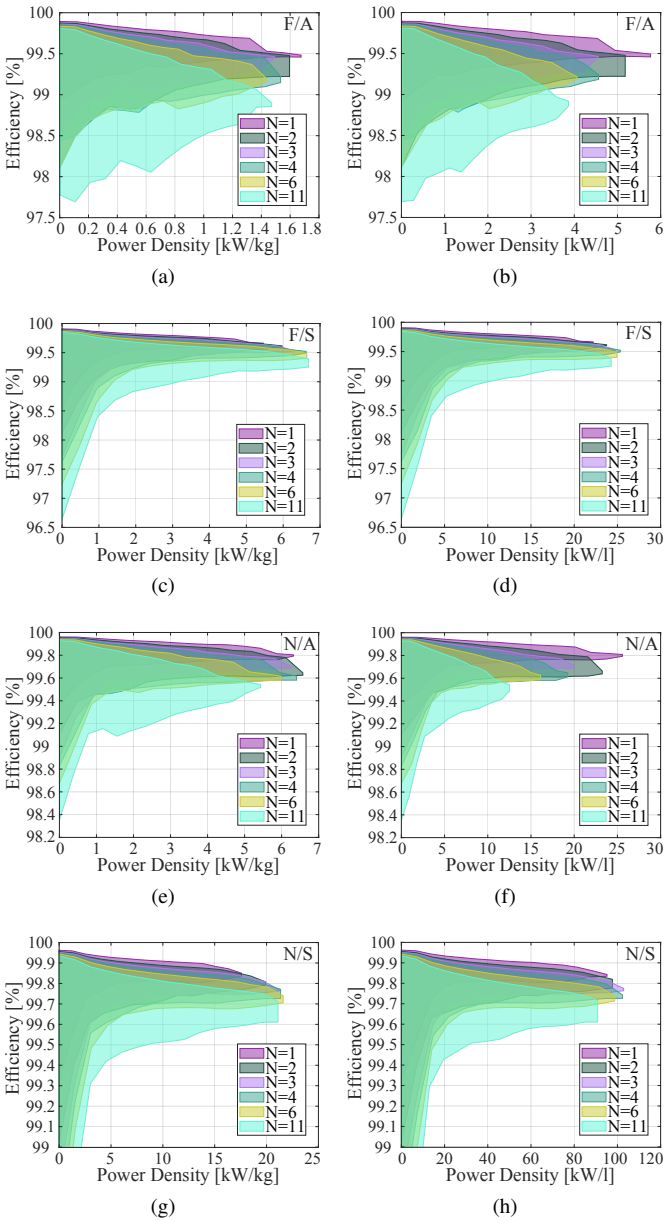

Fig. 8. Efficiency versus power density plots of maximum feasible MFT design sets, generated with the design optimization algorithm for each possible number of ISOP cascaded cells from Table I for all mentioned design variations: Si-Ferrite (F), Nanocrystaline (N), air (A) and solid cast (S) insulated. Each cell is realized as a single DC-DC converter ($M = 1$).

flux path, thus increasing the volume where core and winding losses are present resulting in decreased efficiency. This effect is much stronger for air insulated designs where minimum dielectric widths are significantly higher compared to those that can be achieved with solid insulation.

It can as well be seen how the thermal limit relaxes with the increase of N. This result is also in line with the qualitative analysis. As can be seen from Table II, temperature rise is proportional to the MFT unit of size and indirectly to rated power. In other words, lower power rated transformer units have larger relative cooling surfaces compared to the high power rated units, thus less efficient designs are thermally feasible.

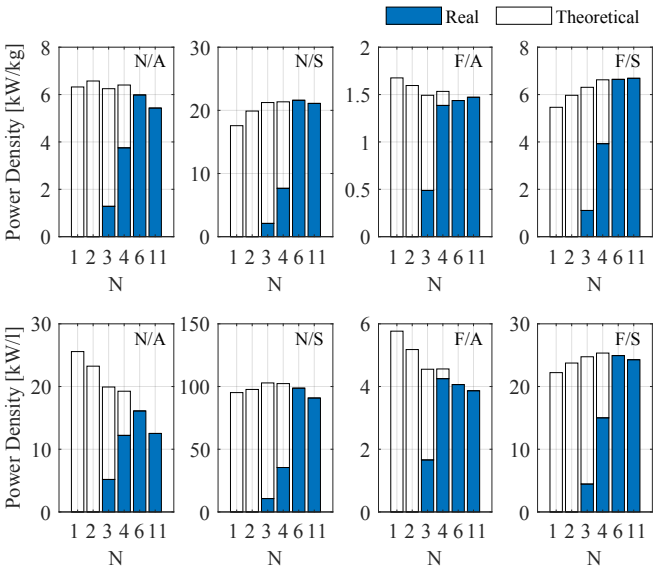

Fig. 9. Bar plots, of maximum achievable gravimetric and volumetric power density versus the number of cascaded ISOP connected cells, denoting the real (Si semiconductor based) and theoretically feasible (emerging SiC semiconductor based) solutions for all mentioned design variations: Si-Ferrite (F), Nanocrystaline (N), air (A) and solid cast (S) insulated. Each cell is realized as a single DC-DC converter ($M = 1$).

While Fig. 8 shows the "theoretical" maximum MFT design feasibility sets, where all of the switches from Table I are available and can switch in range of 0.5-50 kHz, it is interesting to highlight which of these solutions can be realized with already available, "real", power semiconductor modules taking into account their switching frequency limitations. Bar plots, of maximum achievable gravimetric and volumetric power density versus the number of cascaded ISOP connected cells are presented in Fig. 9, denoting the real and theoretically feasible solutions for all of the design choice variations.

As can be seen, there is a clear difference between the real and theoretical solutions, especially for realizations that utilize power semiconductors modules with high blocking voltage (low N). As given in Table I, higher blocking voltages yield lower maximum allowed switching frequencies due to semiconductor physics of available Si IGBTs. Therefore, the domain of practically feasible solutions is confined within this narrowed down frequency range. As the N increases, utilizing power semiconductor modules with lower blocking voltage that can switch faster, the suboptimality gap decreases.

As shown in Figs. 6 and 7, MFT designs with the given design combinations and requirements reach the highest power densities in frequency range approximately between 10 kHz and 20 kHz. Therefore, from the point of view of the MFT power density, all of the DC-DC converter cell realizations utilizing the switches that can switch 25 kHz and higher have zero optimality gap.

It can be observed that the maximum theoretically achievable volumetric power density of the MFT designs featuring air insulation significantly drops with the increase of N. Same as for efficiency, this can directly be explained by the fact that the necessary insulation occupies a higher relative portion of the MFT as the N increases, thus preventing the expected scaling.

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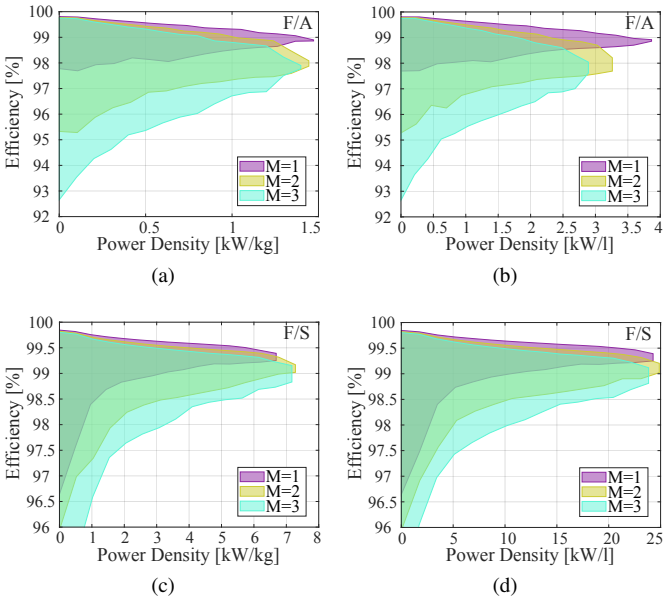

Fig. 10. Efficiency versus power density plots of maximum feasible MFT design sets, generated with the design optimization algorithm for different number of parallel connected DC-DC SRCs within a converter cell from Fig. 1a for the next design variations: Si-Ferrite (F), air (A) and solid cast (S) insulated where $N = 11$

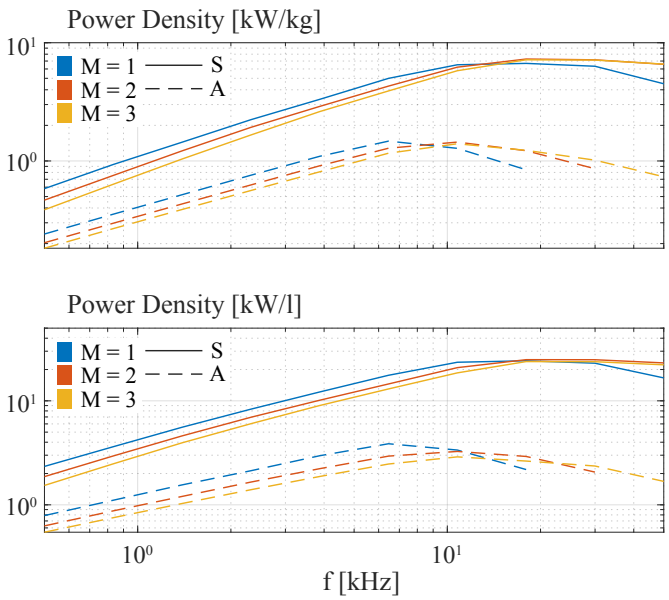

Fig. 11. Maximum achievable gravimetric (top) and volumetric (bottom) power density versus operating frequency plots for different number of parallel connected DC-DC SRCs within a cell for $N = 11$, Si-Ferrite, solid (S) and air (A) insulated MFT designs

On the other hand, for the solid insulated designs, maximum theoretical volumetric power densities are achieved at $(N = 3, 4)$. The volume occupied by the insulation is not as significant in this case, due to the high dielectric strength of the epoxy resin. However, epoxy coating increases the thermal resistances of the windings and therefore these designs converge to their theoretical optimum at higher N where relative cooling conditions are easier.

Moreover it is interesting to notice that, depending on the particular case, nanocrystalline designs achieve around 3-4 times higher power densities compared to Si-Ferrite based alternative. Moreover, solid insulation allows for increase in gravimetric power density in range of 3-4 times and in volumetric power density in range of 3-7 times. Note that only the active part of the MFT, windings, core and insulation, are considered for the volume and weight calculation, as recommended metric for design comparison [20]. Therefore, these differences would amount to lower values after the inclusion of coolers, bushings and other assembly components.

From the aspect of solutions that can be realized with readily available power semiconductor modules, it can be seen that a substantial volume and weight reduction can be achieved with higher modularity (N), utilizing faster power semiconductor modules with lower blocking voltage. Moreover, when it comes to gravimetric power density, the optimal solutions that can be achieved with the existing devices at higher N are either better or not significantly suboptimal compared to the absolute theoretical maximum. This statement holds for the volumetric densities as well, except for the air insulated designs, where relative increase of insulation volume prevents the scaling.

This result shows that, as far as the MFT is concerned, for the considered design choices and under the assumption of smart technology coordination and design optimization, the utilization of faster switching semiconductors does not enable any further substantial power density increase of the MFT (there are obvious benefits on the converter level). Different variations of design choices and lower modularity may become more attractive, but the overall potential power density gain reaches a saturation at some point.

D. Optimal Number Of Parallel Connected DC-DC Converters Within a Cell

Similar to cascaded ISOP connection of DC-DC converter cells, each of the cells can as well be realized as a parallel connection of M DC-DC SRC converters. This is an interesting concept from the efficiency point of view. In most of applications, the given converter would very rarely operate at full load for which it is optimized. Unfortunately, the switching losses and losses in the passive components do not decrease proportionally to the load which usually has a significant impact on efficiency at light load conditions. Similar to concepts deployed in electric vehicle chargers, this type of modular structure allows to turn off an arbitrary number of parallel SRC cells at light load conditions, instead of lossy freewheeling, thus increasing the overall converter efficiency. Therefore, an optimized operation can be achieved in all conditions.

Same as for the number of cascaded ISOP connected DC-DC converter cells, this type of modularity is analyzed from the aspect of potential MFT optimization. A maximum feasible design set is generated for all mentioned MFT design variations with Si-Ferrite core, for different number of parallel connected DC-DC SRCs within a converter cell from Fig. 1a, as displayed in Fig. 10.

Similar to the case of N, it can be seen that a price in MFT efficiency has to be paid for higher M modularity.

Note that, unlike N, M influences only the required rated power of the MFT, whereas input-output voltages remain the same and thus insulation requirements as well. As already discussed in Section V-C, the maximum achievable efficiency is lower for the lower power rated MFT designs, or higher M. However, due to better relative cooling conditions of lower power transformers, relaxing the thermal limit, high power densities can still be achieved in spite of decreased efficiency.

Maximum achievable gravimetric and volumetric power density versus operating frequency plots, for different number of parallel connected DC-DC SRCs within a cell, are presented in Fig. 11, for $N = 11$, Si-Ferrite, solid and air insulated MFT designs. While it can be seen that lower power rated MFT designs have inferior power density at lower frequencies, they maintain the scaling up to higher frequencies, achieving the highest power densities in some cases (e.g. for $M = 3$ and solid insulation). Easier cooling of lower power transformers makes designs on higher frequencies, where power loss density is higher, thermally feasible thus increasing the frequency range where MFT scales favorably.

The ultimate choice of M is a trade-off between how much the nominal converter efficiency can be compromised in favor of added flexibility, allowing for optimized (more efficient) operation at light load conditions. This choice should reflect the expected operating conditions in a way that minimizes the overall amortized losses.

VI. Conclusion

One of the main drivers for solid state transformers (SSTs) operation at medium frequency is the potential to substantially decrease the size of magnetic components. Various design choices on a converter level have a significant influence on the required MFT characteristics and therefore need to be analyzed together. In order to fully explore the potential of this concept, an MFT design optimization is required to properly take into account all of the effects associated to medium-frequency high-power operation at MV.

Design optimization of an MFT is a complex task featuring coupled multi-physics and a multitude of different application specific constraints - e.g. electrical parameters, efficiency, temperature rise, weight, volume, height, width etc. A large number of various design choices and materials makes proper classification or comparison of different designs very difficult. This work has considered a representative subset of possible technologies, which is by no means exhaustive and future work is still required.

Considering targeted technical specifications, it was shown that for the considered variations of MFT design choices and materials, the highest power densities are achieved in approximate frequency range from $10\,\mathrm{kHz}$ to $20\,\mathrm{kHz}$. While it might be possible to maintain the scaling up to slightly higher frequencies by implementing more efficient cooling, this would have an impact on efficiency, cost and system complexity. Further MFT scaling is tied to improvements from the material science - providing better transformer core and winding materials with better high frequency loss characteristic. Therefore, from the point of view of the MFT efficiency and power density, considering the available and technically reasonable core and winding design choices, the operation on higher frequencies does not bring any additional benefits. Furthermore, insulation requirements and the associated dielectric distances do not decrease with frequency increase (even need reinforcing), thus imposing severe constraints on maximum achievable power density.

Although the maximum achievable MFT power density reaches a saturation at mentioned frequencies, development of less lossy semiconductor modules capable of switching on much higher frequencies is very beneficial from the converter efficiency point of view. Furthermore, the availability of the emerging semiconductors with extended blocking voltage range will offer additional design alternatives which may prove optimal for certain applications.

Finally, besides intuitively clear conclusions that MFT power density can be improved using stronger dielectric materials for insulation and better core materials (for the given frequency range), it was shown that by properly exploiting modularity, it is possible to achieve designs within the frequency range of the existing semiconductors, featuring high MFT power densities comparable to the theoretical maximum. On the other hand, emerging wide-bandgap devices will certainly improve the converter part of efficiency.

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