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Sensor-Less Five-Level Packed U-Cell (PUC5) Inverter Operating in Stand-Alone and Grid-Connected Modes

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***Abstract*—In this paper a new mode of operation has been introduced for Packed U-Cell (PUC) inverter. A sensor-less voltage control based on redundant switching states is designed for the PUC5 inverter which is integrated into switching process. The sensor-less voltage control is in charge of fixing the DC capacitor voltage at half of the DC source value results in generating symmetric five-level voltage waveform at the output with low harmonic distortion. The sensor-less voltage regulator reduces the complexity of the control system which makes the proposed converter appealing for industrial applications. An external current controller has been applied for grid-connected application of the introduced sensor-less PUC5 to inject active and reactive power from inverter to the grid with arbitrary power factor while the PUC auxiliary DC bus is regulated only by sensor-less controller combined with new switching pattern. Experimental results obtained in stand-alone and grid-connected operating modes of proposed PUC5 inverter prove the fast response and good dynamic performance of the designed sensor-less voltage control in balancing the DC capacitor voltage at desired level.**

***Index Terms*—Multilevel Inverter, Packed U-Cell, Sensor-Less Voltage Regulator, PUC5, 5-Level Inverter, Power Quality.**

I. Introduction

High harmonic content of output voltage waveform in conventional two-level inverters is a matter of controversy. Nowadays, using more switches and DC sources in power electronics converters is a competitive field of research leads to generate more voltage levels at the output and consequently lower harmonic content, smaller size of the output filters, and lower manufacturing cost as well [1, 2]. Multilevel inverters are designed based on configuration of more switches and DC supplies to achieve the goal of generating various voltage levels at the output. Such inverters generate low harmonic waveforms; therefore they are most suitable for energy conversion applications to deliver efficient power to the loads from renewable energy sources like photovoltaic systems [3-6].

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The main problem of multilevel converters is having more independent DC supplies than the conventional two-level ones that make the use of bulky transformers and diode rectifiers inevitable. Besides, complicated voltage control strategies must be applied in case of using DC capacitors instead of DC sources [7-9].

Researchers have been introducing lots of multilevel inverter topologies also for low and medium power applications like connecting photovoltaic panels to the local grid as household consumption or street lightings to convert the DC voltage of the renewable energy resource to the proper AC waveform useable at load and grid sides. In such applications a single-phase transformer-less inverter with minimum number of DC sources is preferable [10-19]. Packed U-Cell (PUC) inverter has been first introduced by Al-Haddad et al to generate 7-level voltage while using only 6 active switches, one isolated DC sources and one capacitor as second source which its voltage should be controlled to fix at 1/3 of first DC source [20]. Although the mentioned topology has less number of components among other 7-level inverters, it has some major drawbacks including high switching frequency, asymmetric output voltage cycles and levels, requiring fast response and complicated controller with lot of feedback sensors, using large capacitor to regulate the voltage in variable situations and etc [18, 21, 22].

In this paper, the PUC topology is investigated to have simple controller and better performance, which led to proposing a new self-voltage-balancing sensor-less 5-level PUC inverter called sensor-less PUC5. The PUC5 inverter capacitor voltage would be fixed at half of the DC source amplitude using a self-voltage-balancing process which is integrated into the multicarrier pulse width modulation (PWM). Therefore there would be no necessity of using voltage or current sensors due to not using complicated controllers. Since the capacitor voltage is kept constant at desired level, the output voltage waveform would have symmetrical five levels with less harmonic distortion. The PUC5 topology and proposed technique is the subject of a US provisional patent application No.: 62/073387 which is explained and fully investigated in section II. In section III, grid-connected controller is described. Section IV includes some comparative study between multilevel inverters based on number of components. The experimental results including stand-alone and grid-connected modes are shown and discussed in section V to demonstrate the fast and good dynamic performance of proposed sensor-less self-voltage-

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balancing technique applied on PUC5 inverter in regulating the capacitor voltage at desired level and producing five-level output voltage in face of varying conditions.

II. Proposed PUC5 Inverter Topology and Self-Voltage-Balancing Switching Technique

Although the 7-level output waveform of the PUC is interesting due to generating maximum voltage levels while using minimum number of components, requiring complex controller and many sensors to provide state feedbacks for controller calculation as well as asymmetric voltage levels produced make it difficult to get wide spread acceptance by the industries and market.

A. PUC5 Inverter Configuration and Sensor-Less Voltage Balancing Investigation

The single-phase PUC inverter topology has been shown in Fig. 1. The complete associate switching states are listed in table I [20].

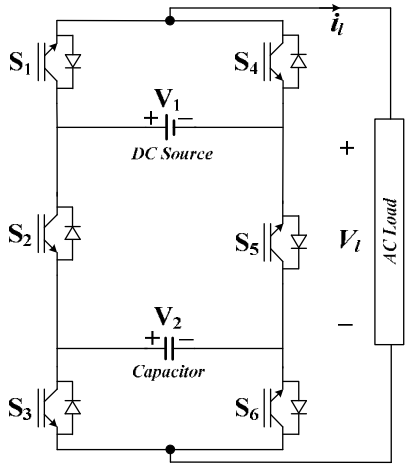

Fig. 1: PUC inverter topology

TABLE I
ALL POSSIBLE SWITCHING STATES OF PUC INVERTER

States	S_1	S_2	S_3	Output Voltage	V_l
1	1	0	0	V_1	+2E
2	1	0	1	V_1-V_2	+E
3	1	1	0	V_2	+E
4	1	1	1	0	0
5	0	0	0	0	0
6	0	0	1	-V_2	-E
7	0	1	0	V_2-V_1	-E
8	0	1	1	-V_1	-2E

It is clear that 8 existing switching states can provide different paths for current to flow through the system including DC sources and load. Taking into account that the output voltage levels numbers depend on DC sources amplitudes, using unequal DC sources result in having different level numbers in output voltage waveform. First, to have maximum number of levels at the output, V_2 amplitude must be 1/3 of V_1. Assuming $V_1=3V_2=3E$, seven levels would be generated as 0, ±E, ±2E, ±3E. 7-level PUC disadvantages were mentioned above which is mostly due to complex voltage balancing procedure, but considering table I more precisely, it is observed that the PUC inverter has the ability to operate as 5-level inverter by assuming $V_1=2V_2=2E$, therefore the output 5-level voltage waveform includes the levels 0, ±E, ±2E. In this case, the capacitor voltage (V_2) is kept constant at half of the DC source (V_1) amplitude. Noticing table I, six switching states are available to produce three levels including –E, 0 and +E that means there are some redundant switching states which may help to find different paths for flowing current through the load. The redundant switching states can deal with charging and discharging the capacitor in order to balance the voltage at the half of the DC source voltage.

To use the redundant switching states in proper design of the required PWM technique for PUC5 inverter, all switching states have been studied noticing the effects on capacitor voltage. Fig. 2 shows the paths made by switching states listed in table I.

Based on Fig. 2, it is clear that in states where the DC source and capacitor are connected in series with the load, the capacitor is charged (states 2 & 7). On the other hand, on some paths that the capacitor feeds the load alone, it is discharging (states 3 & 6). Eventually, for rest of the states, the capacitor voltage is remained unchanged because it is neither connected to DC source nor to the load. Table II indicates the charging and discharging states of the capacitor.

TABLE II
CAPACITOR VOLTAGE STATES

State	Capacitor Voltage
1	No Effect
2	Charging
3	Discharging
4	No Effect
5	No Effect
6	Discharging
7	Charging
8	No Effect

One of the main issues with 7-level PUC inverter in balancing the capacitor voltage is high switching frequency, complexity of the controller and using too many sensors as states variables feedbacks [21, 23]. Since the investigated PUC5 inverter has redundant switching states, the capacitor voltage balancing feature can be integrated into the modulation technique. Therefore the control strategy contains only the PWM switching technique without the necessity of using additional controller (linear or nonlinear or …) which necessitates complex function and more computation effort of the real time controller therefore makes it not simple to implement. It is expected that the voltage controller integrated into switching technique would have good dynamic performance and fast response due to simplicity and not using any feedback sensors.

The key point in table II is the fact that capacitor can be charged or discharged in each positive or negative half cycle. Therefore, in order to keep the capacitor voltage fixed, in designing of proposed switching technique, it has been decided to charge the capacitor in the positive half-cycle and then to discharge it in negative half cycle. Due to the output voltage waveform frequency which is 60 Hz and the selected switching frequency, the capacitor can be only charged to half of the DC source amplitude.

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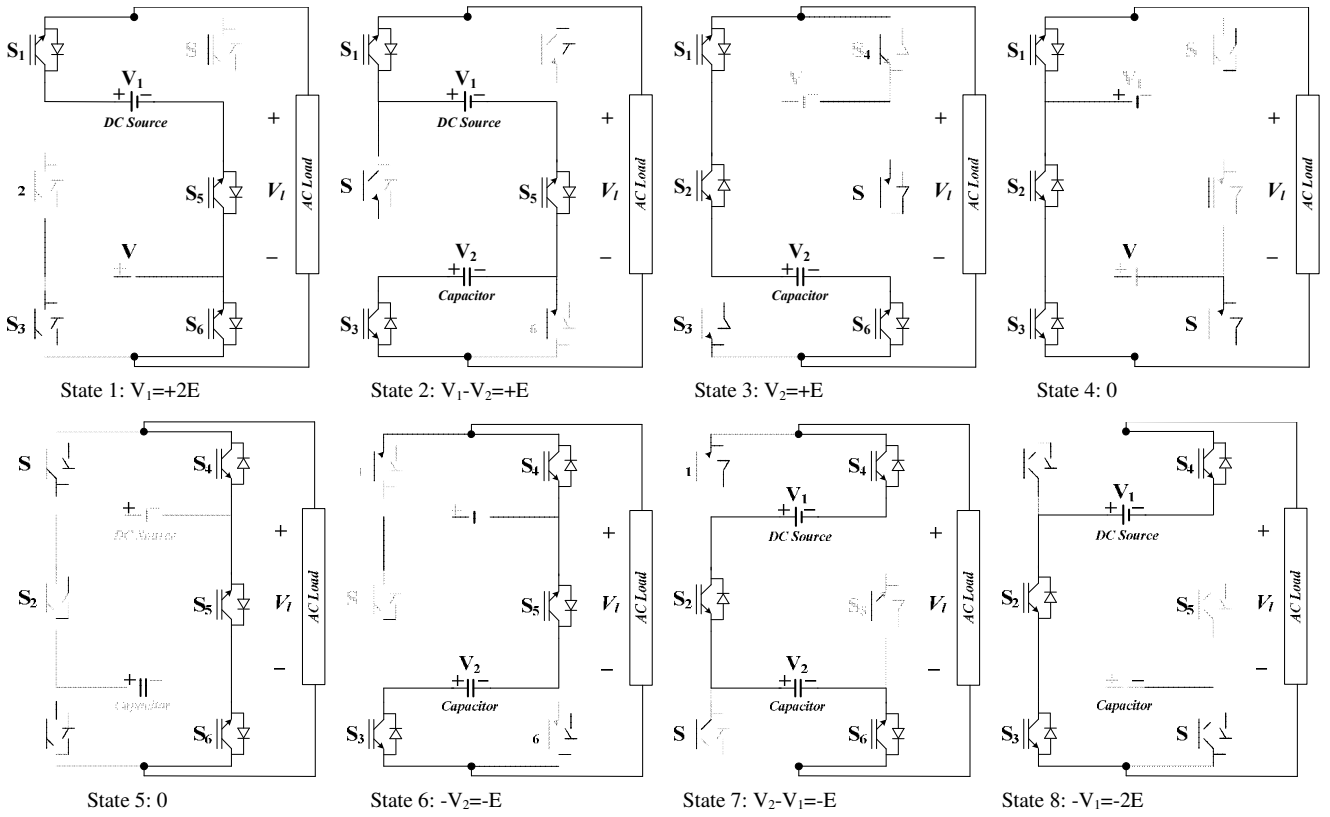

Fig. 2: switching states and conducting paths of PUC5 inverter

Regarding the charging states (2 and 7), it is clear that the capacitor is charged when it is connected in series with DC source and load, as well as the load voltage should be ±E. Thus the following equations can be written:

$$V_1 = V_2 + V_l \Rightarrow \begin{cases} 2E = V_2 + E \\ -2E = V_2 - E \end{cases} \Rightarrow |V_2| = E \qquad (1)$$

While the source voltage is fixed at 2E, the capacitor must be charged up to E to produce the proper output load voltage. Such condition as well as the charging (discharging) time forces the capacitor to charge up to half of source voltage value.

In order to have equivalent times of charging and discharging in one period, switching state 2 is chosen to connect the DC source to the capacitor and charge it up, while on the other hand, the capacitor will be discharged in negative half cycle in order to prevent the overcharged through the switching state 6 which connects the capacitor directly to the load. The mentioned procedure is independent of the switching frequency and output voltage frequency. The capacitor charging and discharging time only depends on load value. It has direct effect on capacitor size which should be considered in calculating the system parameters for specific application design. Larger loads need smaller capacitor in DC link and vice versa.

This self-voltage-balancing procedure can be mathematically proved based on capacitor energy relations. Fig. 3 shows one cycle of the typical output voltage and current waveforms of PUC5 inverter. V_E is a part of output voltage generated by the capacitor (+E or –E) whether connected to the load alone as discharging path or in series with DC source as charging process.

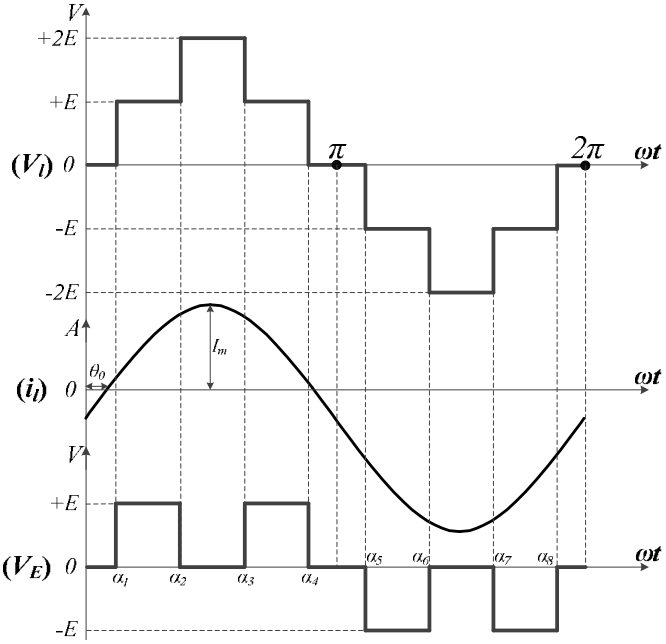

Fig. 3: typical output voltage and current waveform of a five-level inverter

The output voltage and current can be assumed as a following sine functions:

$$v_l(t) = V_m Sin(\omega t) \qquad (2)$$

$$i_l(t) = I_m Sin(\omega t - \theta_0) \qquad (3)$$

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Where, V_m and I_m are the maximum value of output voltage and current waveforms, respectively. As well, θ_0 is the phase difference between output voltage and current. Based on energy absorbing or delivering to the load by dc capacitor, the following equations can be written:

$$\begin{aligned} I &= \frac{dq}{dt} \\ \rightarrow dU &= V\, dq = V\, I\, dt \\ \rightarrow U &= \int V\, I\, dt \end{aligned} \tag{4}$$

Where, I, q, and U are current, electric charge, voltage and energy of the capacitor, respectively. Considering Fig. 3 and substituting equation (3) into (4), the capacitor energy delivered or absorbed in PUC5 inverter can be derived in periods of positive and negative half-cycle of the output voltage. It should be also mentioned that the capacitor voltage is a fixed value at E.

$$\begin{aligned} U^+ &= \int_0^{\pi} V_E I_m Sin(\omega t - \theta_0)\, d(\omega t) \\ &= I_m \int_0^{\pi} V_E Sin(\omega t - \theta_0)\, d(\omega t) \\ &= I_m \left[\begin{array}{l} \int_0^{\alpha_1} 0 \times Sin(\omega t - \theta_0)\, d(\omega t) \\ + \int_{\alpha_1}^{\alpha_2} E \times Sin(\omega t - \theta_0)\, d(\omega t) \\ + \int_{\alpha_2}^{\alpha_3} 0 \times Sin(\omega t - \theta_0)\, d(\omega t) \\ + \int_{\alpha_3}^{\alpha_4} E \times Sin(\omega t - \theta_0)\, d(\omega t) \\ + \int_{\alpha_4}^{\pi} 0 \times Sin(\omega t - \theta_0)\, d(\omega t) \end{array} \right] \\ &= -EI_m Cos(\omega t - \theta_0) \,|_{\alpha_1}^{\alpha_2} \; -EI_m Cos(\omega t - \theta_0) \,|_{\alpha_3}^{\alpha_4} \\ &= EI_m \left[\begin{array}{l} Cos(\alpha_1 - \theta_0) - Cos(\alpha_2 - \theta_0) \\ + Cos(\alpha_3 - \theta_0) - Cos(\alpha_4 - \theta_0) \end{array} \right] \end{aligned} \tag{5}$$

The same effort is done for calculating capacitor energy in negative half-cycle and the following equation would be obtained for U^-:

$$\begin{aligned} U^- &= \int_{\pi}^{2\pi} V_E I_m Sin(\omega t - \theta_0)\, d(\omega t) \\ &= I_m \int_{\pi}^{2\pi} V_E Sin(\omega t - \theta_0)\, d(\omega t) \\ &= EI_m Cos(\omega t - \theta_0) \,|_{\alpha_5}^{\alpha_6} \; + EI_m Cos(\omega t - \theta_0) \,|_{\alpha_7}^{\alpha_8} \\ &= EI_m \left[\begin{array}{l} Cos(\alpha_6 - \theta_0) - Cos(\alpha_5 - \theta_0) \\ + Cos(\alpha_8 - \theta_0) - Cos(\alpha_8 - \theta_0) \end{array} \right] \end{aligned} \tag{6}$$

Noticing the fact that two half cycles of the output voltage are symmetric, thus it can be assumed that:

$$\begin{cases} \alpha_5 = \pi + \alpha_1 \\ \alpha_6 = \pi + \alpha_2 \\ \alpha_7 = \pi + \alpha_3 \\ \alpha_8 = \pi + \alpha_4 \end{cases} \tag{7}$$

Then the energy amount in half cycles would be equal in value but opposite in sign:

$$U^- = -U^+ \tag{8}$$

This means that the capacitor energy in full cycle would be balanced and maintained constant which leads to keep the capacitor voltage at the desired level in all conditions since the reference waveform is periodical.

Higher switching frequency implies more switching pulses make the capacitor charging/discharging time smaller; consequently better voltage balancing performance. Since the sensor-less voltage balancing concept is based on the symmetry of the charging and discharging times it is therefore independent of the grid voltage distortion or unbalanced voltage conditions where the full cycle is reformed (eg the 3rd or 5th harmonic are present). In such conditions, both positive and negative half cycles are still identical and symmetrical results in self-voltage-balancing of the capacitor eventually.

B. Sensor-Less Voltage Controller Integrated Into Switching Technique

Five-level PWM scheme including four carriers' waves and the sinusoidal reference waveform is depicted in Fig. 4. The four carriers' waveforms (Cr_1, Cr_2, Cr_3, and Cr_4) are shifted vertically to modulate the reference waveform (V_{ref}) completely [15, 24]. The firing pulses associated with switching states 1, 2, 4, 5, 6 and 8 (listed in table I) are generated based on comparing V_{ref} with those carrier waves. Moreover, redundant switching states of 4 and 5 are used to reduce the switching frequency. If V_{ref} is positive, then state 4 will be used to produce the zero level at the output. On the other hand, if V_{ref} is negative, the output zero level voltage will be generated by state 5. The described algorithm is shown in Fig. 5 which can produce the five-level voltage waveform at the output with minimum switching frequency while fixing the

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capacitor voltage at the desired level without any feedback sensor.

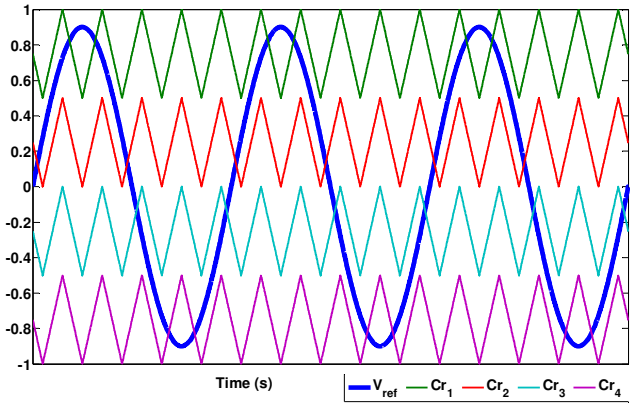

Fig. 4: five-level PWM scheme using four vertically shifted carrier waveforms

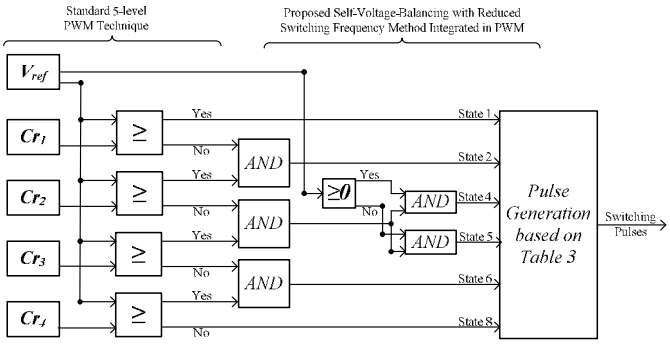

Fig. 5: proposed open-loop switching algorithm for self-voltage-balancing of PUC5 Inverter

As mentioned before, applying the proposed algorithm on PUC5 inverter generates 5-level voltage waveform at the output without using any voltage sensors and complex calculations in controller. The capacitor voltage would be constant even at start-up and also in load change conditions. The light algorithm makes the system much faster than previously implemented controller on PUC inverter as published in the literature. The proposed technique does not depend on system model (e.g. average modelling), feedback sensors, modulation index, switching frequency and grid frequency. It can operate the system starting from zero voltage up to arbitrary amplitude and also in DC source voltage variation situations.

III. Grid-Connected Mode Configuration and Controller

The grid-connected PUC5 inverter with associated controller is shown in Fig. 6 in which i_s is the injected current from inverter to the grid. The typical controller has been designed to control the amplitude and phase-shift of i_s results in delivering active power and exchanging reactive power desirably with the grid by PUC5 inverter. Even in this controller the DC capacitor voltage is not involved since proposed technique in previous section is in charge of balancing this voltage [25-27].

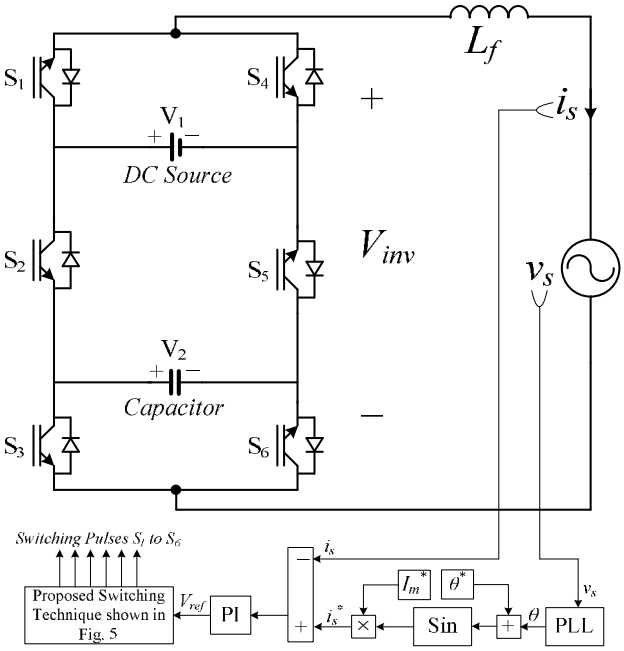

Fig. 6: Grid-connected PUC5 inverter with designed controller

In illustrated controller, AC source voltage (v_s) is measured and sent to the PLL to extract its phase angle. The grid voltage angle is then added to the desired phase shift denoted as θ^*. to exchange reactive power with the grid while injecting active power, power factor (PF) should be between 0 and 1 which can be determined by θ^*. If the unity power factor mode of operation is targeted, therefor $\theta^* = 0$ to ensure an injected grid current synchronized with v_s. For reactive power exchange the power factor should be less than 1. For instance, to have a PF = 0.5 then $\theta^* = 60°$ should be added to the measured voltage angle. The reference angle is sent to the Sin block to produce a unit sine wave containing desired phase shift. This unit sine wave is multiplied by desired value as maximum reference current (I_m^*) which can control the amount of power injected to the grid. The resulted function is assumed as reference current (i_s^*) that should be generated by the inverter. The actual current (i_s) is compared with reference current and the error signal is sent to a proportional-integral linear controller to minimize the steady state error. The PI controller output signal will be modulated by the proposed switching technique shown in Fig. 5 which is also responsible in balancing the PUC5 capacitor voltage at half of the DC source amplitude.

PUC5 inverter is expected to generate lower harmonic current waveform injecting to the grid compared to conventional single-phase full-bridge grid-connected inverters due to generating more voltage levels at the output.

IV. Comparative Study of Multilevel Inverter Based on Number of Components

Table III shows the components count in popular multilevel inverters as well as the proposed PUC5 inverter in case of producing single-phase 5-level output voltage waveform. It is prominent that the proposed converter with the sensor-less voltage balancing technique has the less components as well as its control complexity is very low.

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Extending to the n-level, table IV will be achieved. Component counts are calculated in term of voltage level (n). It should be mentioned that in more than 3-level inverters, no reliable control techniques have been reported for NPC since all of them have some limitations on load power factor and modulation index [28]. Although it has been compared in Table III, it is not listed in the Table IV for higher voltage levels. Moreover, the proposed PUC5 inverter is able to produce voltage levels using binary DC links so it would have the levels like 5, 10, 17, 26, ... [29-31].

The following chart in Fig. 7 demonstrates the low number of components used in PUC5 inverter rising by the voltage levels. It is observed that the number of components employed in PUC5 is slowly raised as a function of the produced voltage levels.

TABLE III
COMPONENTS COUNT FOR SINGLE-PHASE FIVE-LEVEL INVERTERS

Inverter Type	DC Source	Capacitor	Clamped Diode	Active Switch	Total Parts Count	Control Complexity
CHB	2	0	0	8	10	Low
NPC with voltage control	1	4	6	8	19	Very High
NPC without voltage control	4	0	6	8	18	Low
FC	1	3	0	8	12	High
Proposed PUC5	1	1	0	6	8	Very Low

TABLE IV
COMPONENTS COUNT FOR SINGLE-PHASE MULTILEVEL INVERTERS

Inverter Type	DC Source	Capacitor	Clamped Diode	Active Switch	Total Parts Count
CHB	$\frac{n-1}{2}$	*0*	*0*	*2(n-1)*	$\frac{5(n-1)}{2}$
NPC without voltage control	*n-2*	*0*	*2(n-2)*	*2(n-1)*	*5n-7*
FC	*1*	*n-2*	*0*	*2(n-1)*	*3(n-1)*
Proposed PUC5	*1*	$\sqrt{n-1}-1$	*0*	$2\sqrt{n-1}+2$	$3\sqrt{n-1}+2$

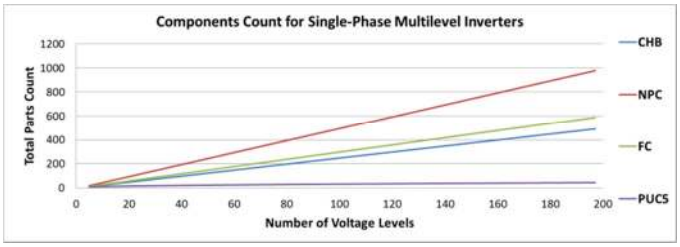

Fig. 7: components count chart in multilevel inverters

As a comparison only between 7-level PUC inverter and the proposed PUC5, it should be noted that the 7-level PUC needs a very complicated controller to produce desired voltage levels at the output which requires adjusting a lot of controller gains in practical works. Moreover, the controller design needs a lot of effort in modelling the system accurately and using many state variable feedbacks that increase the number of state variables and consequently voltage and current sensors. Moreover, It is highly dependent on the system parameters including load, connection line resistance and inductance, switching frequency, sampling time, DC source voltage amplitude, DC capacitor value, modulation index and output voltage frequency. It can show improper results containing a lot of spikes on the generated voltage waveform, which makes use of additional protection device inevitable. All in all, the 7-level PUC inverter needs more investigation and improvement to be useful in all conditions. On the other hand, the proposed 5-level functionality of the PUC inverter illustrates proper results in all stand-alone and grid-connected conditions without using additional feedback sensors to balance internal DC bus voltage. However, it should be mentioned that the sensor-less voltage balancing is only about the internal capacitor voltage control of the converter and it does not imply on any other external sensors such as shown in Fig. 6 to control the line current. Less complex controller combined with lower switching frequency are some advantages of the proposed PUC5 inverter with requiring less components count as well.

V. EXPERIMENTAL RESULTS

A prototype of PUC inverter has been built to validate the proposed PUC5 with self-voltage-balancing in both stand-alone and grid-connected modes. Six 1.2KV 40A SiC MOSFETs type SCT2080KE have been used as active switches. The proposed self-voltage balancing procedure integrated into switching technique and the designed grid-connected controller has been applied by dSpace 1103 as real-time controller and switching pulses are sent to the PUC5 switches. The tested system parameters are listed in table V.

TABLE V
EXPERIMENTAL SYSTEM PARAMETERS

Grid Voltage (v_s)	110 V rms
Grid Frequency	60 Hz
Grid Link Inductor (L_f)	4 mH
DC Source Voltage (V_1)	200 V
Switching Frequency	2 kHz
Stand-Alone mode RL Load	40 Ω, 20 mH
Stand-Alone mode Rectifier Load (DC Side R_{dc} and L_{dc})	40 Ω, 50 mH
DC Capacitor	2500 µF

A. Test 1: Stand-Alone Mode

The PUC5 inverter has been tested under various load conditions such as stand-alone mode as UPS application including change in load and in DC source. In this mode, the PUC5 inverter supplies an RL type of load.

At first, the start-up mode of the PUC5 inverter is shown in Fig. 8. The capacitor is charged up to half of DC source by proposed sensor-less voltage balancing approach and five-level output voltage is generated symmetrically. Results show that no pre-charged capacitor is needed in this topology with the implemented voltage control. Moreover, the zoomed figure shows that the capacitor voltage ripple is less than 5%. The FFT analysis of the 5-level inverter voltage waveform has been performed and its harmonic spectrum is shown in Fig. 8. It should be mentioned that the output voltage THD is about 10% without adding additional bulky harmonic filters. 2 kHz frequency of the PWM carriers is clear in this figure as the highest amplitude of the harmonic orders except the fundamental one.

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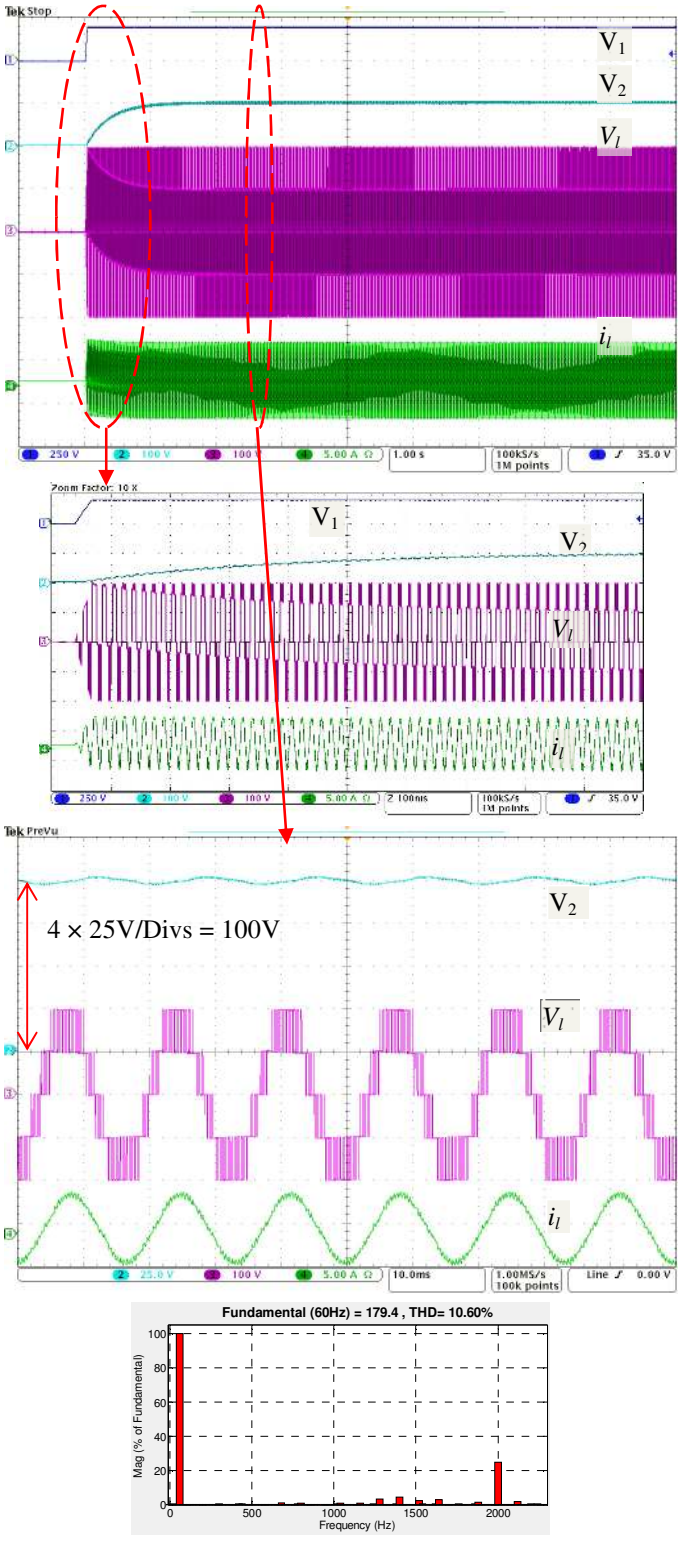

Fig. 8: start-up capacitor charging, 5-level voltage generating and FFT analysis

In another test, a nonlinear load consisting of a single-phase rectifier connected to R_{dc} and L_{dc} on its DC side is connected in parallel to the existing RL load and they are feed by PUC5 inverter. Results are illustrated in Fig. 9 that demonstrate the good dynamic performance of proposed technique in variable load conditions.

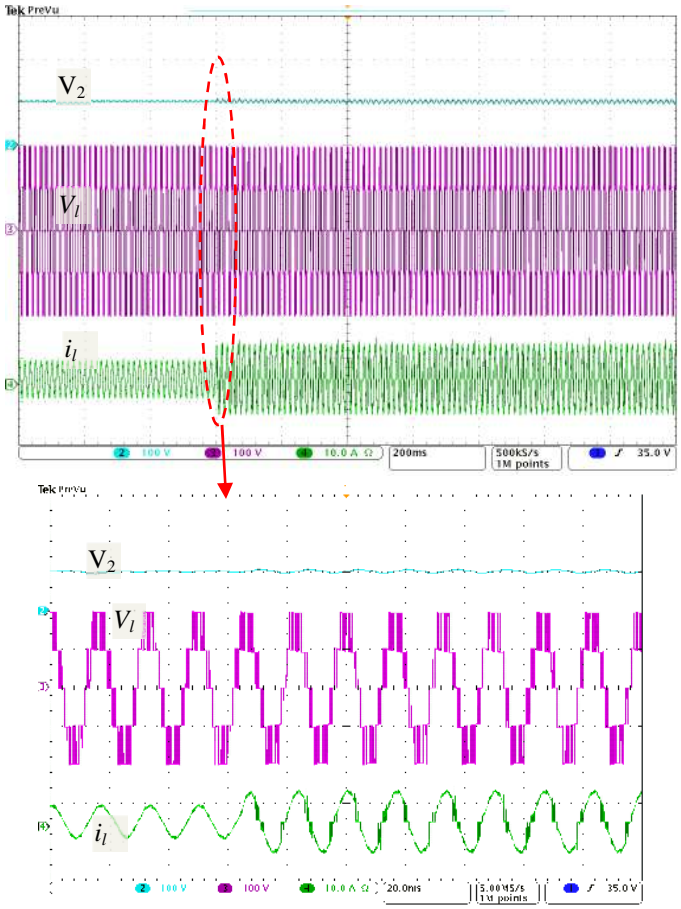

Fig 9: adding single-phase rectifier (as nonlinear load) paralleled with the RL load to the output of PUC5

Fig. 10 contains results when the DC source voltage is changing and capacitor voltage is tracking the reference value ($V_1/2$) properly by applying proposed sensor-less voltage regulator technique integrated into switching pattern.

Finally, in stand-alone mode, switches gate pulses as well as one cycle of output voltage are depicted in Fig. 11. It is clear that two upper switches are operating at grid frequency while their voltage rating as equal to DC source voltage (V_1). Although, four lower switches are fired with higher frequency than upper switches, the switching frequency is not that large compared to 2-level conventional inverters [32, 33]. Moreover, their voltage ratings are half of two upper switches that they have to withstand capacitor voltage which is $V_1/2$.

B. Test 2: Grid-Connected Mode

In this case, the PUC5 inverter is connected to a single-phase AC source as grid and the designed controller in section III is forcing the inverter to inject power to the grid with different power factor. At first, to show the fast response and proper dynamic performance of designed grid-connected controller as well as proposed sensor-less voltage balancing technique, $\theta^* = 0$ is selected and the current reference is changed during the test as illustrated in Fig. 12.

As it is obvious, the grid-connected PUC5 is operating in unity power factor and injecting active power to the grid. The grid-connected controller is working acceptably in making the current waveform in phase with ac voltage waveform.

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Moreover, the proposed sensor-less self-voltage-balancing method operates significantly perfect in regulating the capacitor voltage at desired level while encountering any kind of changes in the system and produces five-level voltage at the output of the inverter. Due to generating 5-level voltage waveform at the output of grid-connected PUC5 inverter, the injecting current through grid would have lower harmonic components without using any extra filters that enlarge the inverter package. Fig. 13 illustrates the current THD which is too much lower than the acceptable amount in standards.

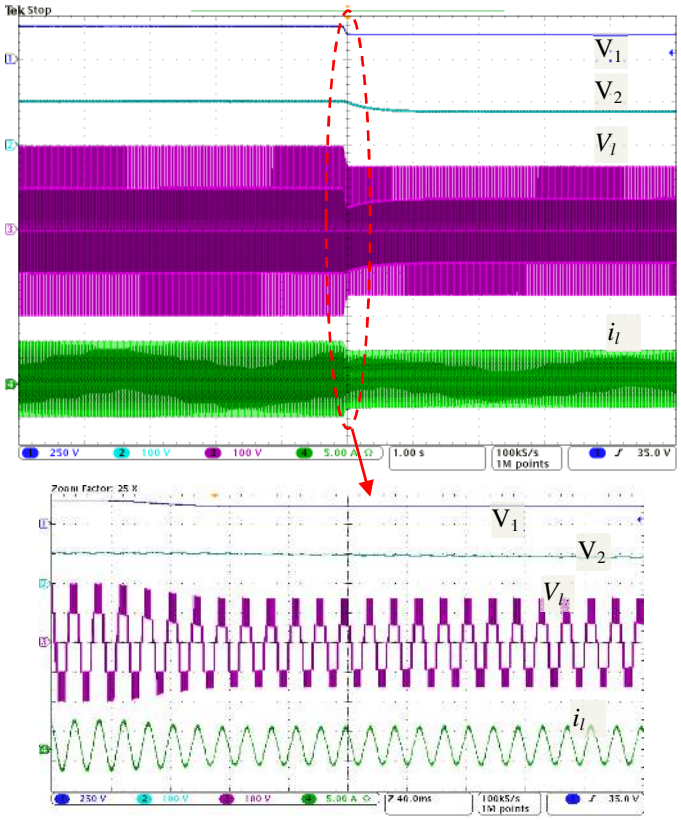

Fig. 10: DC source voltage changes and capacitor voltage is tracking the reference value

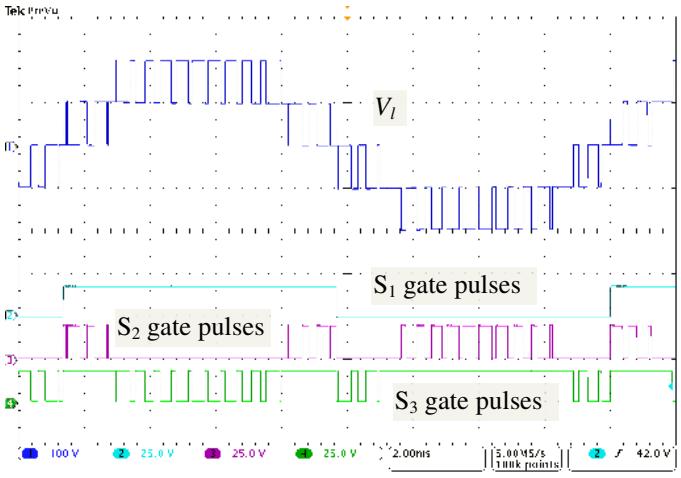

Fig. 11: switches gate pulses

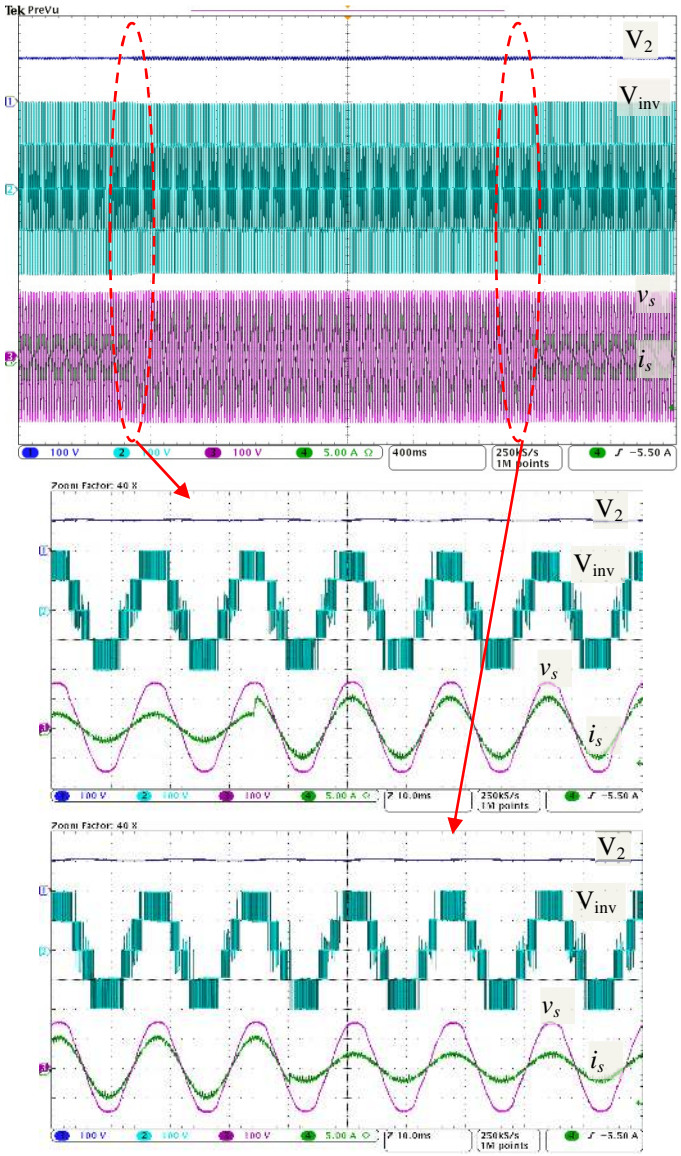

Fig. 12: grid-connected PUC5 with change in current reference amplitude

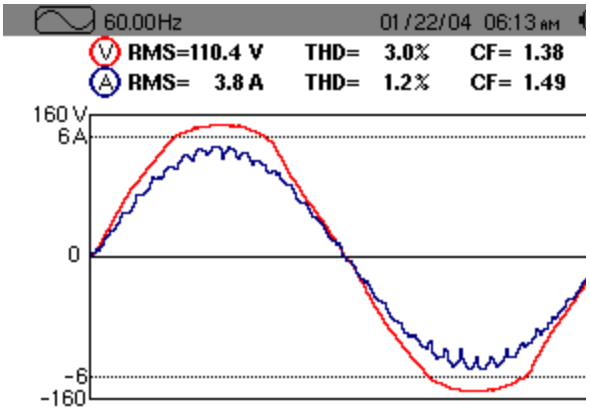

Fig. 13: THD, and Crest factor computation of injected grid current

Final tests have been performed to exchange reactive power with the grid while injecting reduced amount of active power. Therefore, two different PFs of 0.86 and 0.5 have been selected and associated displacement angles are 30° and 60°,

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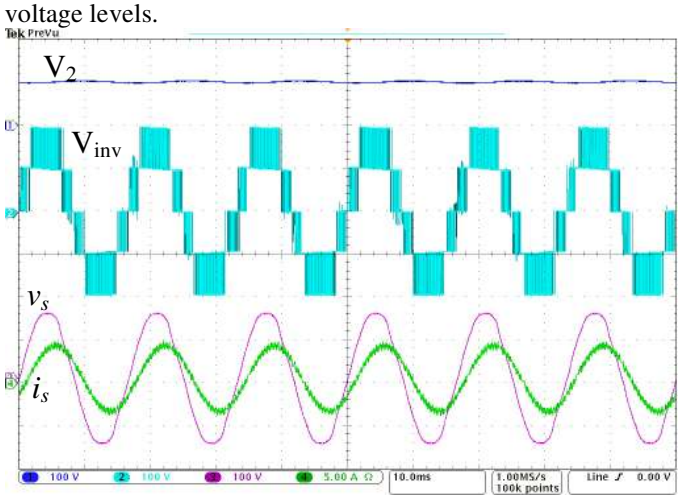
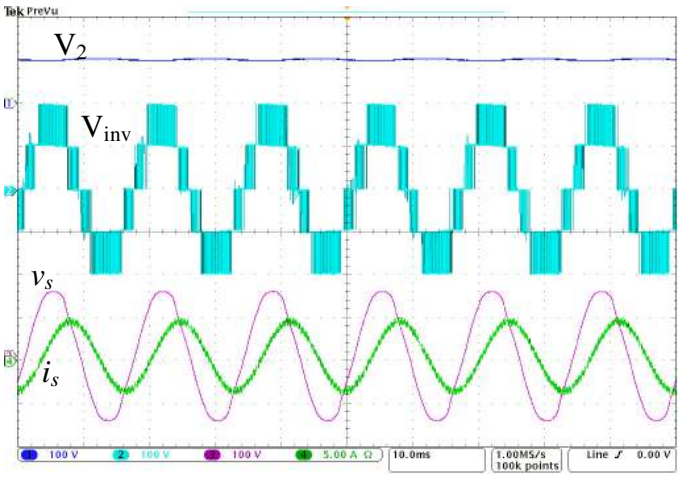
respectively as depicted in Fig 14 which shows the phase shift between grid voltage and current. In both cases (30° & 60° phase shift) the capacitor voltage is regulated at desired level, whereas inverter output waveform contains five identical voltage levels.



a)



b)

Fig. 14: PUC5 inverter operation at different power factors a) PF = 0.86, θ = 30° b) PF = 0.86, θ = 60°

7-level waveform has been replaced by 5-level operation containing equal harmonic contents while a significant simplicity has been obtained on the controller with PWM switching technique useful for various industrial applications. In the PUC5 converter, due to accurate voltage balancing process, the output voltage waveform shows a good symmetry in positive and negative half cycles that makes its THD smaller.

VI. Conclusion

The PUC5 inverter has been proposed in this paper while the capacitor voltage is balanced without involving any external controller and voltage feedback sensors. The proposed sensor-less voltage controller has been integrated into switching technique to work as open-loop system with reliable results. Moreover, another controller has been designed for the PUC5 inverter to work as unity power factor grid-connected inverter. Low harmonics components in both voltage and current waveforms generated by PUC5, no need to bulky output filters, reliable and good dynamic performance in variable conditions (including change in DC source, load, power amount injected to the grid), requiring no voltage/current sensor in stand-alone mode, low manufacturing costs and miniaturized package due to using less components and etc are interesting advantages of the introduced PUC5 topology which have been proved by experimental results in both stand-alone and grid-connected modes. The presented PUC5 inverter can be a challenging candidate for conventional photovoltaic application inverters.

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