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Faculty of Electrical Engineering
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Ph.D. Thesis

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Sensorless Control Strategies for Three - Phase PWM Rectifiers

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1. *INTRODUCTION*

Methods for limitation and elimination of disturbances and harmonic pollution in the power system have been widely investigated. This problem rapidly intensifies with the increasing amount of electronic equipment (computers, radio set, printers, TV sets etc.). This equipment, a nonlinear load, is a source of current harmonics, which produce increase of reactive power and power losses in transmission lines. The harmonics also cause electromagnetic interference and, sometimes, dangerous resonances. They have negative influence on the control and automatic equipment, protection systems, and other electrical loads, resulting in reduced reliability and availability. Moreover, nonlinear loads and non-sinusoidal currents produce non-sinusoidal voltage drops across the network impedance's, so that non-sinusoidal voltages appears at several points of the mains. It brings out overheating of line, transformers and generators due to the iron losses.

Reduction of harmonic content in line current to a few percent allows avoiding most of the mentioned problems. Restrictions on current and voltage harmonics maintained in many countries through IEEE 519-1992 in the USA and IEC 61000-3-2/IEC 61000-3-4 in Europe standards, are associated with the popular idea of **clean power**.

Many of harmonic reduction method exist. These technique based on passive components, mixing single and three-phase diode rectifiers, and power electronics techniques as: multipulse rectifiers, active filters and PWM rectifiers (Fig. 1.1). They can be generally divided as:

A) harmonic reduction of already installed non-linear load;

B) harmonic reduction through linear power electronics load installation;

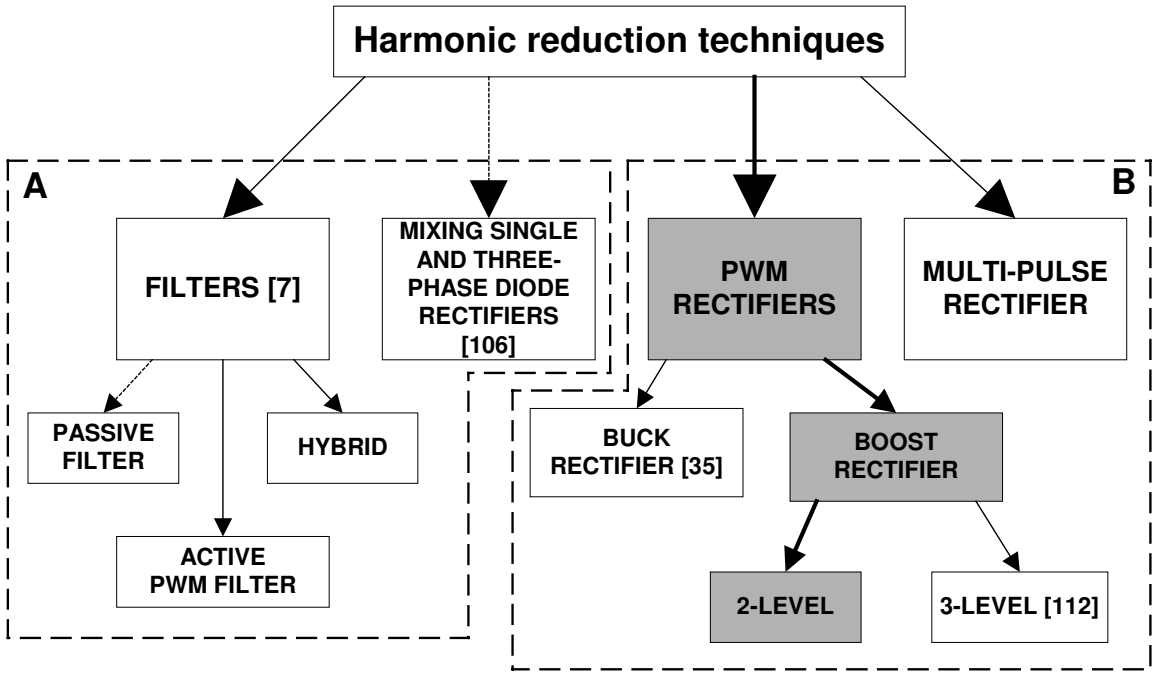

Fig.1.1 Most popular three-phase harmonic reduction techniques of current
A) Harmonic reduction of already installed non-linear load
B) Harmonic reduction through linear power electronics load installation

The traditional method of current harmonic reduction involves passive filters LC, parallel-connected to the grid. Filters are usually constructed as series-connected legs of capacitors and chokes. The number of legs depends on number of filtered harmonics (5^{th}, 7^{th}, 11^{th}, 13^{th}). The advantages of passive filters are simplicity and low cost [105]. The disadvantages are:

- each installation is designed for a particular application (size and placement of the filters elements, risk of resonance problems),
- high fundamental current resulting in extra power losses,
- filters are heavy and bulky.

In case of diode rectifier, the simpler way to harmonic reduction of current are additional series coils used in the input or output of rectifier (typical 1-5%).

The other technique, based on mixing single and three-phase non-linear loads, gives a reduced THD because the 5^{th} and 7^{th} harmonic current of a single-phase diode rectifier often are in counter-phase with the 5^{th} and 7^{th} harmonic current of a three-phase diode rectifier [106].

The other already power electronics techniques is use of multipulse rectifiers. Although easy to implement, possess several disadvantages such as: bulky and heavy transformer, increased voltage drop, and increased harmonic currents at non-symmetrical load or line voltages.

An alternative to the passive filter is use of the active PWM filter (*AF*), which displays better dynamics and controls the harmonic and fundamental currents. Active filters are mainly divided into two different types: the active shunt filter (current filtering) (Fig. 1.2) and the active series filter (voltage filtering) [7].

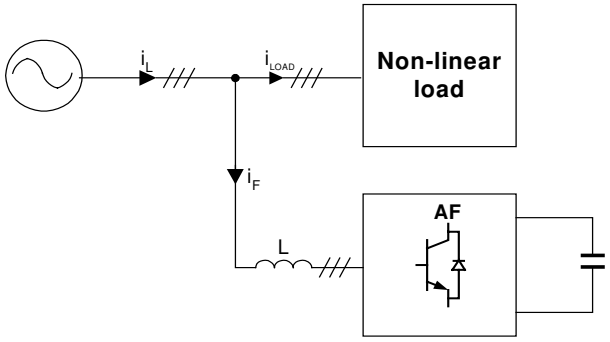

Fig. 1.2 Three-phase shunt active filter together with non-linear load.

The three-phase two-level shunt *AF* consist of six active switches and its topology is identical to the PWM inverter. *AF* represents a controlled current source i_F which added to the load current i_{Load} yields sinusoidal line current i_L (Fig. 1.2). *AF* provide:

- compensation of fundamental reactive components of load current,
- load symetrization (from grid point of view),
- harmonic compensation much better than in passive filters.

In spite of the excellent performance, *AF*s possess certain disadvantages as complex control, switching losses and *EMC* problems (switching noise is present in the line current and even in the line voltage). Therefore, for reduction of this effects, inclusion of a small low-pass passive filter between the line and the *AF* is necessary.

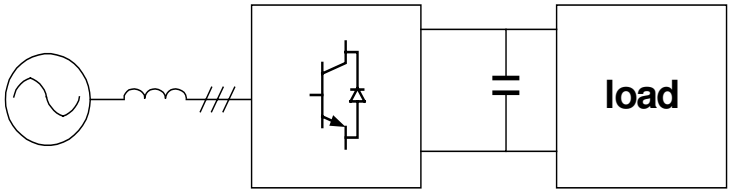

Fig.1.3 PWM rectifier

The other interesting reduction technique of current harmonic is a *PWM* (active) rectifier (Fig. 1.3). Two types of *PWM* converters, with a voltage source output (Fig. 1.4a) and a current source output (Fig. 1.4b) can be used. First of them called a *boost* rectifier (increases the voltage) works with fixed DC voltage polarity, and the second, called a *buck* rectifier (reduces the voltage) operates with fixed DC current flow.

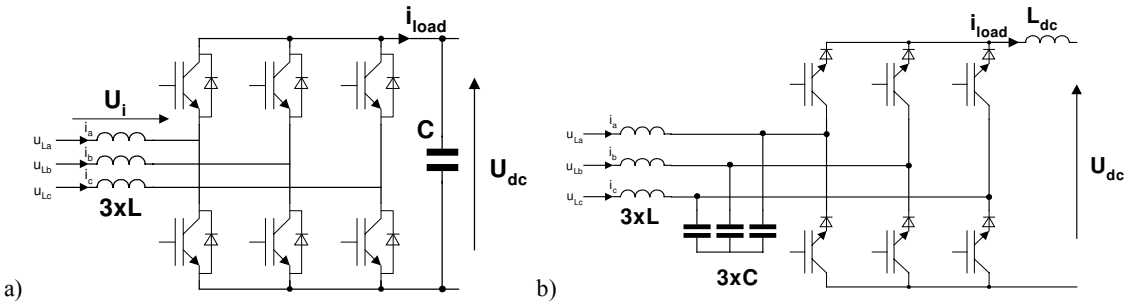

Fig. 1.4 Two basic topologies of PWM rectifier:
a) *boost* with voltage output b) *buck* with current output

Among the main features of PWM rectifier are:

- bi-directional power flow,
- nearly sinusoidal input current,
- regulation of input power factor to unity,
- low harmonic distortion of line current (*THD* below 5%),
- adjustment and stabilization of DC-link voltage (or current),
- reduced capacitor (or inductor) size due to the continues current.

Furthermore, it can be properly operated under line voltage distortion and notching, and line voltage frequency variations.

Similar to the *PWM* active filter, the PWM rectifier has a complex control structure, the efficiency is lower than the diode rectifier due to extra switching losses. A properly designed low-pass passive filter is needed in front of the *PWM* rectifier due to *EMI* concerns.

The last technique is most promising thanks to advances in power semiconductor devices (enhanced speed and performance, and high ratings) and digital signal

processors, which allow fast operation and cost reduction. It offers possibilities for implementation of sophisticated control algorithm.

This thesis is devoted to investigation of different control strategies for *boost* type of three-phase bridge PWM rectifiers. Appropriate control can provide both the rectifier performance improvements and reduction of passive components. Several control techniques for PWM rectifiers are known [16-23, 30-69]. A well-known method based on indirect active and reactive power control is based on current vector orientation with respect to the line voltage vector (Voltage Oriented Control - VOC) [30-69]. An other less known method based on instantaneous direct active and reactive power control is called Direct Power Control (DPC) [16, 20-23]. Both mentioned strategies do not produce sinusoidal current when the line voltage is distorted. Therefore, the following thesis can be formulated:

"using the control strategy based on virtual flux instead of the line voltage vector orientation provides lower harmonic distortion of line current and leads to line-voltage sensorless operation".

In order to prove the above thesis, the author used an analytical and simulation based approach, as well as experimental verification on the laboratory setup with a 5kVA IGBT converter.

The thesis consists of six chapters. Chapter 1 is an introduction. Chapter 2 is devoted to presentation of various topologies of rectifiers for ASD's. The mathematical model and operation description of PWM rectifier are also presented. General features of the sensorless operation focused on AC voltage-sensorless. Voltage and virtual flux estimation are summarized at the end of the chapter. Chapter 3 covers the existing solution of Direct Power Control and presents a new solution based on Virtual Flux estimation [17]. Theoretical principles of both methods are discussed. The steady state and dynamic behavior of VF-DPC are presented, illustrating the operation and performance of the proposed system as compared with a conventional DPC method. Both strategies are also investigated under unbalanced and distorted line voltages. It is shown that the VF-DPC exhibits several advantages, particularly it provides sinusoidal line current when the supply voltage is non-ideal. Test results show excellent

performance of the proposed system. Chapter 4 is focused on the Voltage Oriented and Virtual Flux Oriented Controls. Additionally, development and investigation of novel modulation techniques is described and discussed, with particular presentation of adaptive modulation. It provides a wide range of linearity, reduction of switching losses and good dynamics. Chapter 5 contains comparative study of discussed control methods. Finally Chapter 6 presents summary and general conclusions. The thesis is supplemented by nine Appendices among which are: conventional and instantaneous power theories [A.2], implementation of a space vector modulator [A.3], description of the simulation program [A.4] and the laboratory set-up [A.6].

In the author's opinion the following parts of the thesis represent his original achievements:

- development of a new line voltage estimator – (Section 2.5),
- elaboration of new Virtual Flux based Direct Power Control for PWM rectifiers – (Section 3.4),
- implementation and investigation of various closed-loop control strategies for PWM rectifiers: Virtual Flux – Based Direct Power Control (VF -DPC), Direct Power Control (DPC), Voltage Oriented Control (VOC), Virtual Flux Oriented Control (VFOC) – (Sections 3.6 and 4.5),
- development of a new Adaptive Space Vector Modulator for three-phase PWM converter, working in polar and cartesian coordinate system (Patent No. P340 113) – (Section 4.4.7),
- development of a simulation algorithm in SABER and control algorithm in C language for investigation of proposed solutions – (Appendix A.4),
- construction and practical verification of the experimental setup based on a mixed RISC/DSP (PowerPC 604/TMS320F240) digital controller – (Appendix A.6).

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References

Appendices

List of Symbols

Symbols (general)

x(t), x – instantaneous value
X^*, x^* - reference
$\overline{X}, \overline{x}$ - average value, average (continuous) part
$\widetilde{X}, \widetilde{x}$ - oscillating part
$\underline{x}$ - complex vector
$\underline{x}^*$ - conjugate complex vector
$|X|$ - magnitude (length) of function
$\Delta X, \Delta x$ - deviation

Symbols (special)

α - phase angle of reference vector
λ - power factor
φ - phase angle of current
ω - angular frequency
ψ - phase angle
ε - control phase angle

$cos\varphi$ - fundamental power factor
f – frequency
i(t), i – instantaneous current
j – imaginary unit
k_P, k_I – proportional control part, integral control part
p(t), p – instantaneous active power
q(t), q – instantaneous reactive power
t – instantaneous time
v(t), v - instantaneous voltage

$\underline{\Psi_L}$ – virtual line flux vector
$\Psi_{L\alpha}$ – virtual line flux vector components in the stationary α, β coordinates
$\Psi_{L\beta}$ – virtual line flux vector components in the stationary α, β coordinates
Ψ_{Ld} – virtual line flux vector components in the synchronous d, q coordinates
Ψ_{Lq} – virtual line flux vector components in the synchronous d, q coordinates

$\underline{u_L}$ – line voltage vector
$u_{L\alpha}$ – line voltage vector components in the stationary α, β coordinates
$u_{L\beta}$ – line voltage vector components in the stationary α, β coordinates
u_{Ld} – line voltage vector components in the synchronous d, q coordinates
u_{Lq} – line voltage vector components in the synchronous d, q coordinates

$\underline{i_L}$ – line current vector
$i_{L\alpha}$ – line current vector components in the stationary α, β coordinates
$i_{L\beta}$ – line current vector components in the stationary α, β coordinates

i_{Ld} – line current vector components in the synchronous d, q coordinates
i_{Lq} – line current vector components in the synchronous d, q coordinates

$\underline{u}_S$, $\underline{u}_{conv}$ – converter voltage vector
$u_{S\alpha}$ – converter voltage vector components in the stationary α, β coordinates
$u_{S\beta}$ – converter voltage vector components in the stationary α, β coordinates
u_{Sd} – converter voltage vector components in the synchronous d, q coordinates
u_{Sq} – converter voltage vector components in the synchronous d, q coordinates

u_{dc} – DC link voltage
i_{dc} – DC link current

S_a, S_b, S_c – Switching state of the converter

C – capacitance
I – root mean square value of current
L – inductance
R – resistance
S – apparent power
T – time period
P – active power
Q – reactive power
Z - impedance

Subscripts
..a, ..b, ..c - phases of three-phase system
..d, ..q - direct and quadrature component
..+, -, 0 - positive, negative and zero sequence component
..α, ..β, ..0 - alpha, beta components and zero sequence component
..h – harmonic order of current and voltage, harmonic component
..n – harmonic order
..max - maximum
..min - minimum
..L-L - line to line
..Load - load
..conv - converter
..Loss - losses
..ref - reference
..m - amplitude
..rms - root mean square value

Abbreviations

AF	active PWM filter
ANN	artificial neural network
ASD	adjustable speed drives
ASVM	adaptive space vector modulation
CB-PWM	carrier based pulse width modulation

CSI	current source inverter
DPC	direct power control
DSP	digital signal processor
DTC	direct torque control
EMI	electro-magnetic interference
FOC	field-oriented control
IFOC	indirect field-oriented control
IGBT	insulated gate bipolar transistor
PCC	point of common coupling
PFC	power factor correction
PI	proportional integral (controller)
PLL	phase locked loop
PWM	pulse-width modulation
REC	rectifier
SVM	space vector modulation
THD	total harmonic distortion
UPF	unity power factor
VF	virtual flux
VF-DPC	virtual flux based direct power control
VFOC	virtual flux oriented control
VOC	voltage oriented control
VSI	voltage source inverter
ZSS	zero sequence signal

2. PWM RECTIFIER

2.1. INTRODUCTION

As it has been observed for recent decades, an increasing part of the generated electric energy is converted through rectifiers, before it is used at the final load. In power electronic systems, especially, diode and thyristor rectifiers are commonly applied in the front end of DC-link power converters as an interface with the *AC* line power (grid) - Fig. 2.1. The rectifiers are nonlinear in nature and, consequently, generate harmonic currents in to the *AC* line power. The high harmonic content of the line current and the resulting low power factor of the load, causes a number of problems in the power distribution system like:

- voltage distortion and electromagnetic interface (*EMI*) affecting other users of the power system,
- increasing voltampere ratings of the power system equipment (generators, transformers, transmission lines, etc.).

Therefore, governments and international organizations have introduced new standards (in the USA: *IEEE 519* and in Europe: *IEC 61000-3*)[A8] which limit the harmonic content of the current drown from the power line by the rectifiers. As a consequence a great number of new switch-mode rectifier topologies that comply with the new standards have been developed.

In the area of variable speed AC drives, it is believed that three-phase PWM boost AC/DC converter will replace the diode rectifier. The resulting topology consists of two identical bridge PWM converters (Fig. 2.4). The line-side converter operates as rectifier in forward energy flow, and as inverter in reverse energy flow. In farther discussion assuming the forward energy flow, as the basic mode of operation the line-side converter will be called as PWM rectifier. The AC side voltage of PWM rectifier can be controlled in magnitude and phase so as to obtain sinusoidal line current at unity power factor (UPF). Although such a PWM rectifier/inverter (AC/DC/AC) system is expensive, and the control is complex, the topology is ideal for four-quadrant operation. Additionally, the PWM rectifier provides DC bus voltage stabilization and can also act as active line conditioner (*ALC*) that compensate harmonics and reactive power at the point of common coupling of the distribution network. However, reducing the cost of the PWM rectifier is vital for the competitiveness compared to other front-end rectifiers. The cost of power switching devices (e.g. *IGBT*) and digital signal processors (*DSP's*) are generally decreasing and further reduction can be obtained by reducing the number of sensors. Sensorless control exhibits advantages such as improved reliability and lower installation costs.

2.2. RECTIFIERS TOPOLOGIES

A voltage source PWM inverter with diode front-end rectifier is one of the most common power configuration used in modern variable speed AC drives (Fig. 2.1). An uncontrolled diode rectifier has the advantage of being simple, robust and low cost. However, it allows only undirectional power flow. Therefore, energy returned from the motor must be dissipated on power resistor controlled by chopper connected across the DC link. The diode input circuit also results in lower power factor and high level of harmonic input currents. A further restriction is that the maximum motor output voltage is always less than the supply voltage.
Equations (2.1) and (2.2) can be used to determine the order and magnitude of the harmonic currents drawn by a six-pulse diode rectifier:

$$h = 6k \pm 1 \qquad k = 1, 2, 3,... \tag{2.1}$$

$$\frac{I_h}{I_1} = 1/h \tag{2.2}$$

Harmonic orders as multiples of the fundamental frequency: 5^{th}, 7^{th}, 11^{th}, 13^{th} etc., with a 50 Hz fundamental, corresponds to 250, 350, 550 and 650 Hz, respectively. The magnitude of the harmonics in per unit of the fundamental is the reciprocal of the harmonic order: 20% for the 5^{th} , 14,3% for the 7^{th}, etc. Eqs. (2.1)-(2.2) are calculated from the Fourier series for ideal square wave current (critical assumption for infinite inductance on the input of the converter). Equations (2.1) is fairly good description of the harmonic orders generally encountered. The magnitude of actual harmonic currents often differs from the relationship described in (2.2). The shape of the *AC* current depends on the input inductance of converter (Fig. 2.2). The ripple current is equal 1/L times the integral of the DC ripple voltage. With infinite inductance the ripple current is zero and the flap-top wave of Fig. 2.2d results. The full description of harmonic calculation in six-pulse converter can be found in [116].

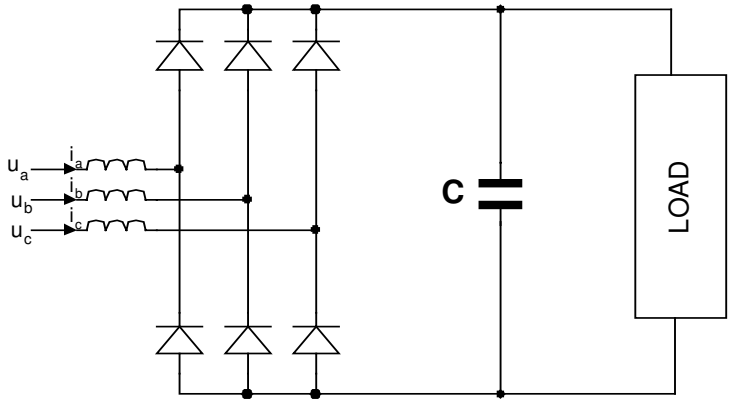


Fig. 2.1 Diode rectifier

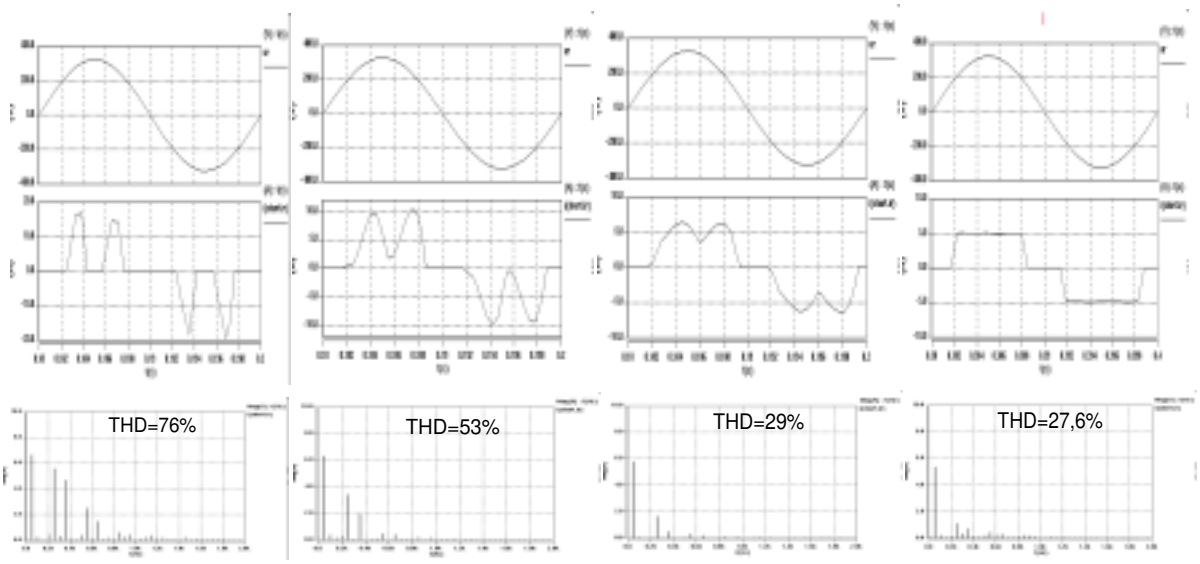


Fig. 2.2 Simulation results of diode rectifier at different input inductance (from 0 to infinity)

Besides of six-pulse bridge rectifier a few other rectifier topologies are known [117-118]. Some of them are presented in Fig. 2.3. The topology of Fig. 2.3(a) presents simple solution of boost – type converter with possibility to increase DC output voltage. This is important feature for *ASD's* converter giving maximum motor output voltage. The main drawback of this solution is stress on the components, low frequency distortion of the input current. Next topologies (b) and (c) uses a PWM rectifier modules with a very low current rating (20-25% level of rms current comparable with (e) topology). Hence they have a low cost potential provide only possibility of regenerative braking mode (b) or active filtering (c). Fig. 2.3d presents 3-level converter called *Vienna* rectifier [112]. The main advantage is low switch voltage, but not typical switches are required. Fig. 2.3e presents most popular topology used in *ASD*, *UPS* and recently like a PWM rectifier. This universal topology has the advantage of using a low-cost three-phase module with a bi-directional energy flow capability. Among disadvantages are: high per-unit current ratting, poor immunity to shoot-through faults, and high switching losses. The features of all topologies are compared in Table 2.1.

Table 2.1 Features of three-phase rectifiers

feature / topology	Regulation of DC output voltage	Low harmonic distortion of line current	Near sinusoidal current waveforms	Power factor correction	Bi-directional power flow	Remarks
Diode rectifier	-	-	-	-	-	
Rec(a)	+	-	-	+	-	
Rec(b)	-	-	-	-	+	
Rec(c)	-	+	+	+	-	UPF
Rec(d)	+	+	+	+	-	UPF
Rec(e)	+	+	+	+	+	UPF

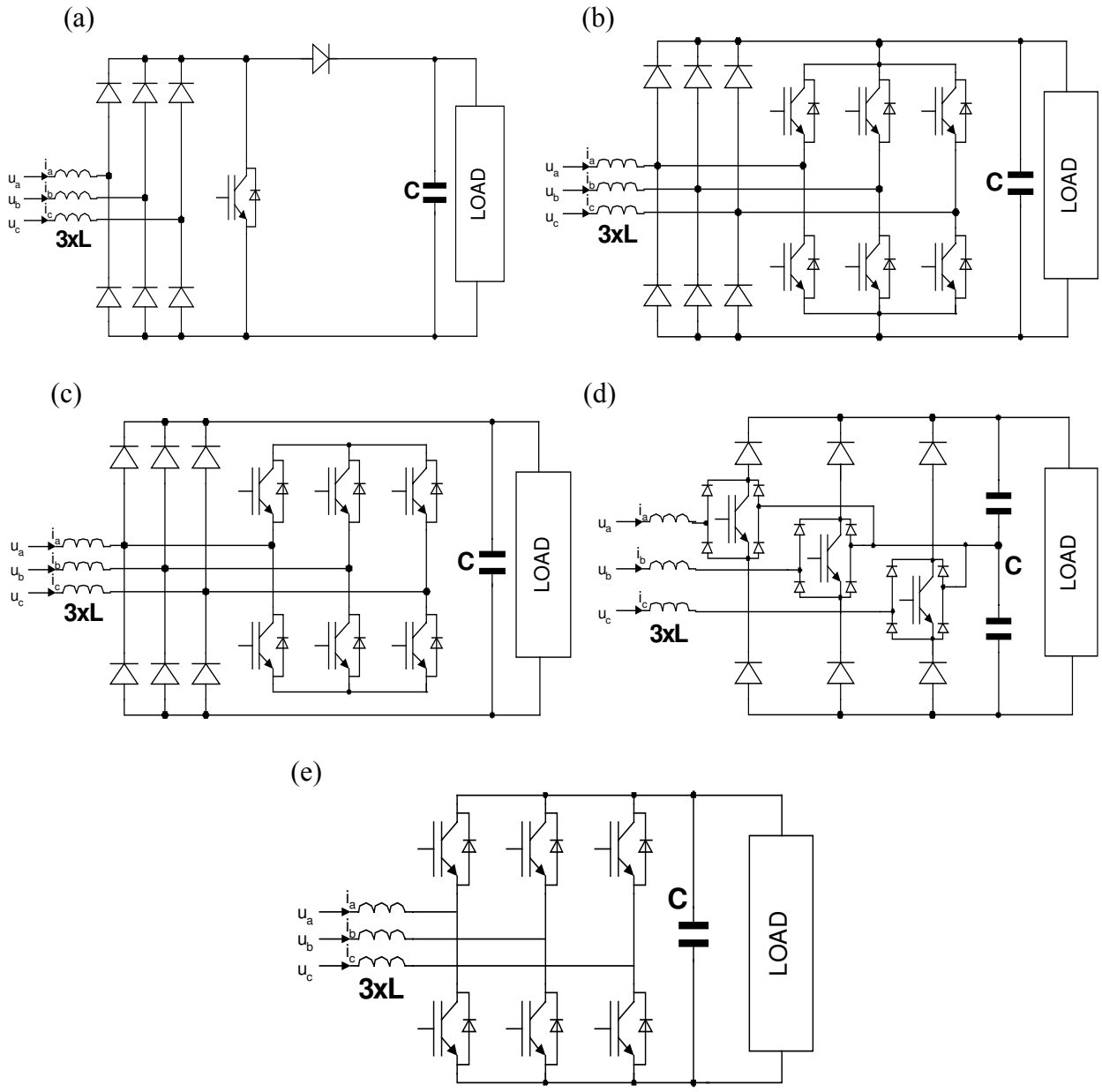


Fig.2.3 Basic topologies of switch-mode three-phase rectifiers
a) simple boost-type converter b) diode rectifier with PWM regenerative braking rectifier
c) diode rectifier with PWM active filtering rectifier d) Vienna rectifier (3 – level converter)
e) PWM reversible rectifier (2 – level converter)

The last topology is most promising therefore was chosen by most global company (SIMENS, ABB and other). In a *DC* distributed Power System (Fig. 2.5) or AC/DC/AC converter (Fig. 2.4), the *AC* power is first transformed into *DC* thanks to three-phase PWM rectifier. It provides *UPF* and low current harmonic content. The converters connected to the DC-bus provide further desired conversion for the loads, such as adjustable speed drives for induction motors (*IM*) and permanent magnet synchronous motor (*PMSM*), DC/DC converter, multidrive operation, etc.

The AC/DC/AC converter (Fig. 2.4) is known in ABB like an ACS611/ACS617 (15 kW - 1,12 MW) complete four-quadrant drive. The line converter is identical to the ACS600 (DTC) motor converter with the exception of the control software [20,121]. Similar solutions possess SIEMENS in Simovert Masterdrive (2,2 kW – 2,3 MW) [127]. Furthermore, AC/DC/AC provide:

- the motor can operate at a higher speed without field weakening (by maintaining the DC-bus voltage above the supply voltage peak),
- decreased theoretically by one-third common mode voltage compared to conventional configuration thanks to the simultaneous control of rectifier - inverter (same switching frequency and synchronized sampling time may avoid common-mode voltage pulse because the different type of zero voltage (U_0, U_7) are not applied at the same time) [114],
- the response of the voltage controller can be improved by fed-forward signal from the load what gives possibility to minimize the DC link capacitance while maintaining the DC-link voltage within limits under step load conditions [104, 111].

Other solution used in industry is shown in Fig. 2.5 like a multidrive operation [120]. ABB propose active front-end converter ACA 635 (250 kW - 2,5 MW) and Siemens Simovert Masterdrive in range of power from 7,5 kW up to 1,5 MW.

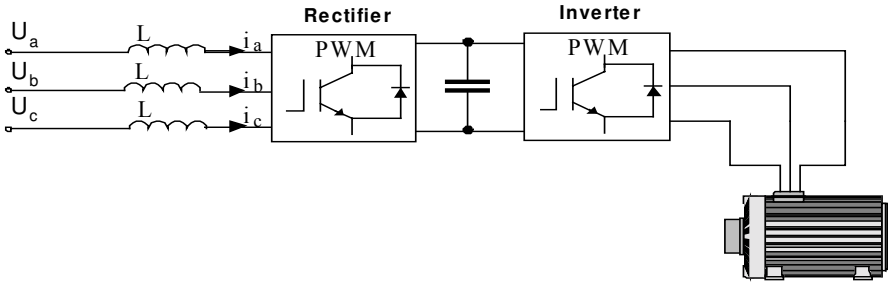


Fig. 2.4 AC/DC/AC converter

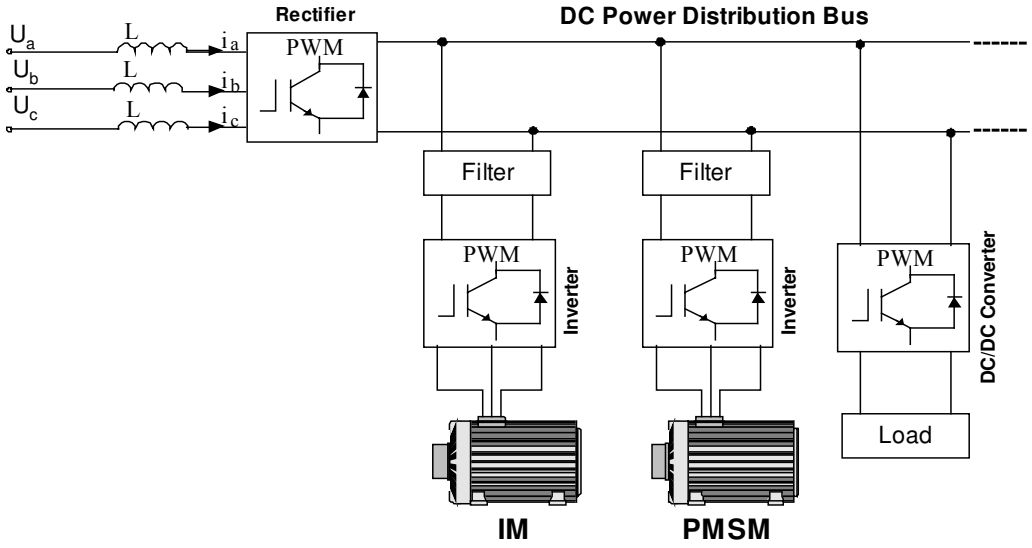


Fig. 2.5 DC distributed Power System

2.3 OPERATION OF THE PWM RECTIFIER

Fig. 2.6b shows a single-phase representation of the rectifier circuit presented in Fig. 2.6a. L and R represents the line inductor. $\underline{u}_L$ is the line voltage and $\underline{u}_S$ is the bridge converter voltage controllable from the DC-side. Magnitude of $\underline{u}_S$ depends on the modulation index and DC voltage level.

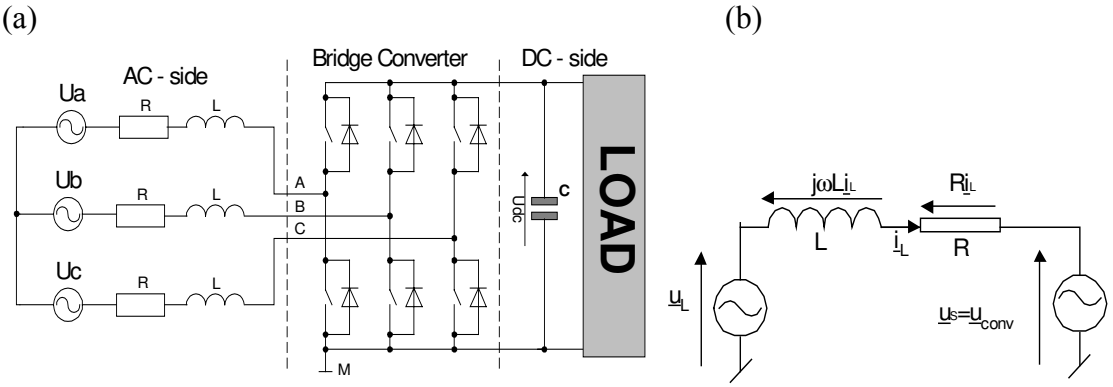


Fig. 2.6 Simplified representation of three-phase PWM rectifier for bi-directional power flow. a) main circuit b) single-phase representation of the rectifier circuit

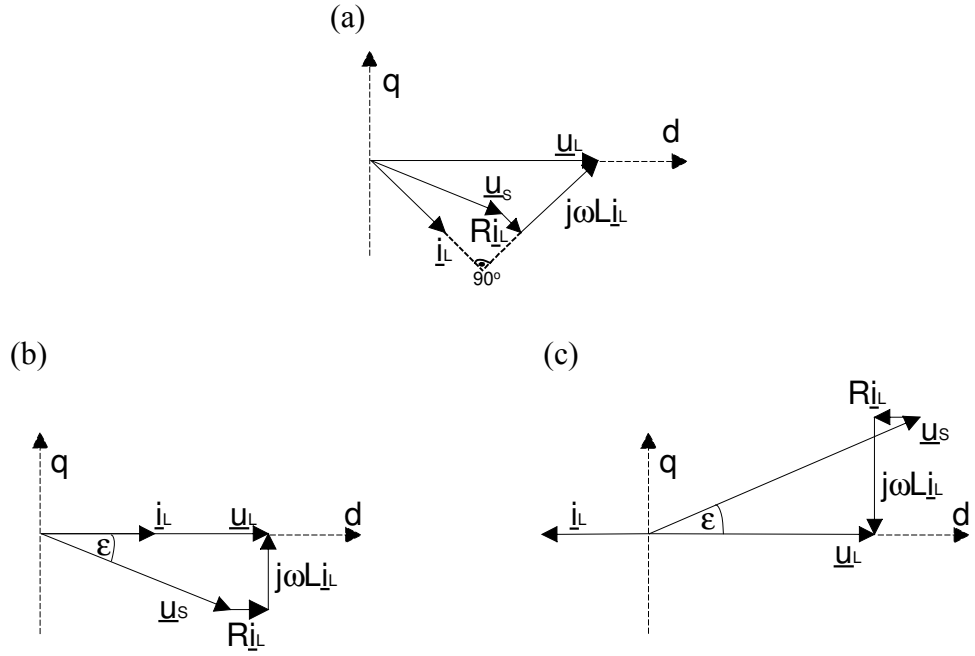


Fig. 2.7 Phasor diagram for the PWM rectifier a) general phasor diagram b) rectification at unity power factor c) inversion at unity power factor

Inductors connected between input of rectifier and lines are integral part of the circuit. It brings current source character of input circuit and provide boost feature of converter. The line current i_L is controlled by the voltage drop across the inductance L interconnecting two voltage sources (line and converter). It means that the inductance voltage u_I equals the difference between the line voltage u_L and the converter voltage u_S. When we control phase angle ε and amplitude of converter voltage u_S, we control

indirectly phase and amplitude of line current. In this way average value and sign of *DC* current is subject to control what is proportional to active power conducted through converter. The reactive power can be controlled independently with shift of fundamental harmonic current I_L in respect to voltage U_L.
Fig. 2.7 presents general phasor diagram and both rectification and regenerating phasor diagrams when unity power factor is required. The figure shows that the voltage vector $\underline{u_S}$ is higher during regeneration (up to 3%) then rectifier mode. It means that these two modes are not symmetrical [67].
Main circuit of bridge converter (Fig. 2.6a) consists of three legs with *IGBT* transistor or, in case of high power, *GTO* thyristors. The bridge converter voltage can be represented with eight possible switching states (Fig. 2.8 six-active and two-zero) described by equation:

$$u_{k+1} = \begin{cases} (2/3)u_{dc}e^{jk\pi/3} \\ 0 \end{cases} \quad \text{for } k = 0...5 \tag{2.3}$$

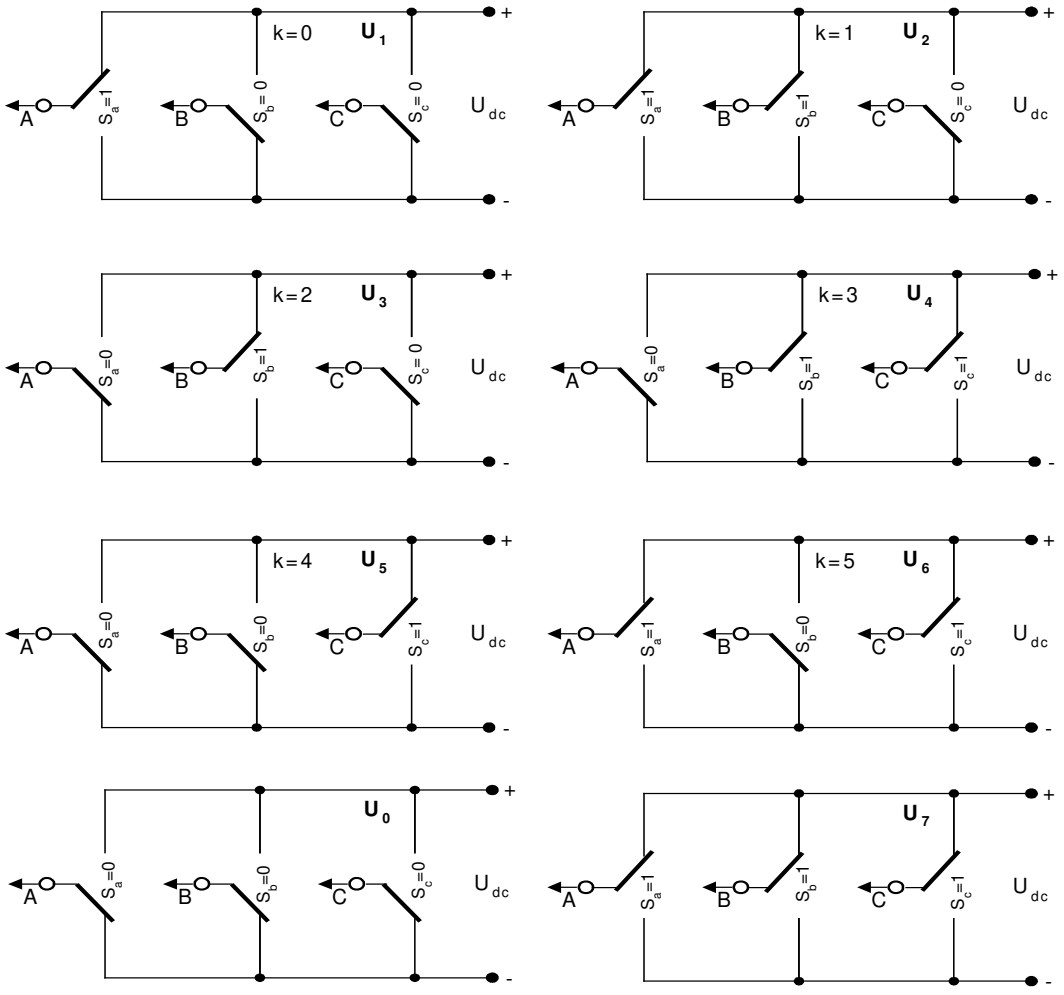


Fig. 2.8 Switching states of PWM bridge converter

2.3.1 Mathematical description of the PWM rectifier

The basic relationship between vectors of the PWM rectifier is presented in Fig. 2.9.

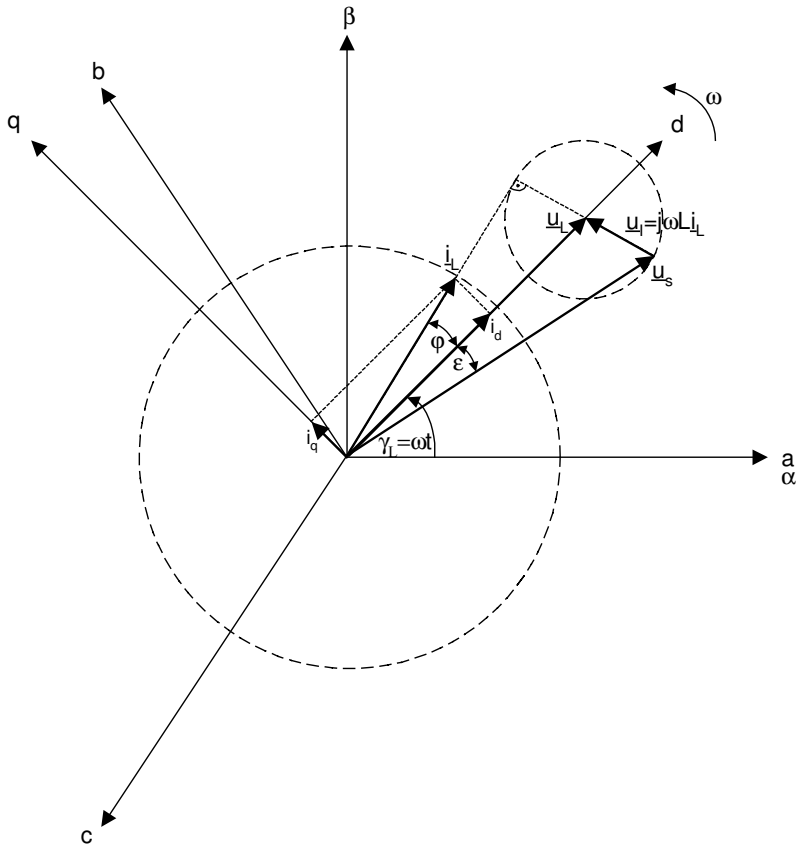


Fig. 2.9 Relationship between vectors in PWM rectifier

Description of line voltages and currents

Three phase line voltage and the fundamental line current is:

$$u_a = E_m \cos \omega t \tag{2.4a}$$

$$u_b = E_m \cos(\omega t + \frac{2\pi}{3}) \tag{2.4b}$$

$$u_c = E_m \cos(\omega t - \frac{2\pi}{3}) \tag{2.4c}$$

$$i_a = I_m \cos(\omega t + \varphi) \tag{2.5a}$$

$$i_b = I_m \cos(\omega t + \frac{2\pi}{3} + \varphi) \tag{2.5b}$$

$$i_c = I_m \cos(\omega t - \frac{2\pi}{3} + \varphi) \tag{2.5c}$$

where E_m (I_m) and ω are amplitude of the phase voltage (current) and angular frequency, respectively, with assumption

$$i_a + i_b + i_c \equiv 0 \tag{2.6}$$

we can transform equations (2.4) to α-β system thanks to equations (A.2.22a) and the input voltage in α-β stationary frame are expressed by:

$$u_{L\alpha} = \sqrt{\frac{3}{2}} E_m \cos(\omega t) \tag{2.7}$$

$$u_{L\beta} = \sqrt{\frac{3}{2}} E_m \sin(\omega t) \tag{2.8}$$

and the input voltage in the synchronous *d-q* coordinates (Fig. 2.9) are expressed by:

$$\begin{bmatrix} u_{Ld} \\ u_{Lq} \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{3}{2}} E_m \\ 0 \end{bmatrix} = \begin{bmatrix} \sqrt{u_{L\alpha}^2 + u_{L\beta}^2} \\ 0 \end{bmatrix} \tag{2.9}$$

Description of input voltage in PWM rectifier

Line to line input voltages of PWM rectifier can be described with the help of Fig. 2.8 as:

$$u_{Sab} = (S_a - S_b) \cdot u_{dc} \tag{2.10a}$$

$$u_{Sbc} = (S_b - S_c) \cdot u_{dc} \tag{2.10b}$$

$$u_{Sca} = (S_c - S_a) \cdot u_{dc} \tag{2.10c}$$

and phase voltages are equal:

$$u_{Sa} = f_a \cdot u_{dc} \tag{2.11a}$$

$$u_{Sb} = f_b \cdot u_{dc} \tag{2.11b}$$

$$u_{Sc} = f_c \cdot u_{dc} \tag{2.11c}$$

where:

$$f_a = \frac{2S_a - (S_b + S_c)}{3} \tag{2.12a}$$

$$f_b = \frac{2S_b - (S_a + S_c)}{3} \tag{2.12b}$$

$$f_c = \frac{2S_c - (S_a + S_b)}{3} \tag{2.12c}$$

The f_a, f_b, f_c are assume *0, ±1/3 and ±2/3*.

Description of PWM rectifier

Model of three-phase PWM rectifier

The voltage equations for balanced three-phase system without the neutral connection can be written as (Fig. 2.7b):

$$\underline{u_L} = \underline{u_I} + \underline{u_S} \tag{2.13}$$

$$\underline{u_L} = R\underline{i_L} + \frac{d\underline{i_L}}{dt}L + \underline{u_S} \tag{2.14}$$

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = R\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + L\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} u_{Sa} \\ u_{Sb} \\ u_{Sc} \end{bmatrix} \tag{2.15}$$

and additionally for currents

$$C\frac{du_{dc}}{dt} = S_a i_a + S_b i_b + S_c i_c - i_{dc} \tag{2.16}$$

The combination of equations (2.11, 2.12, 2.15, 2.16) can be represented as three-phase block diagram (Fig. 2.10) [34].

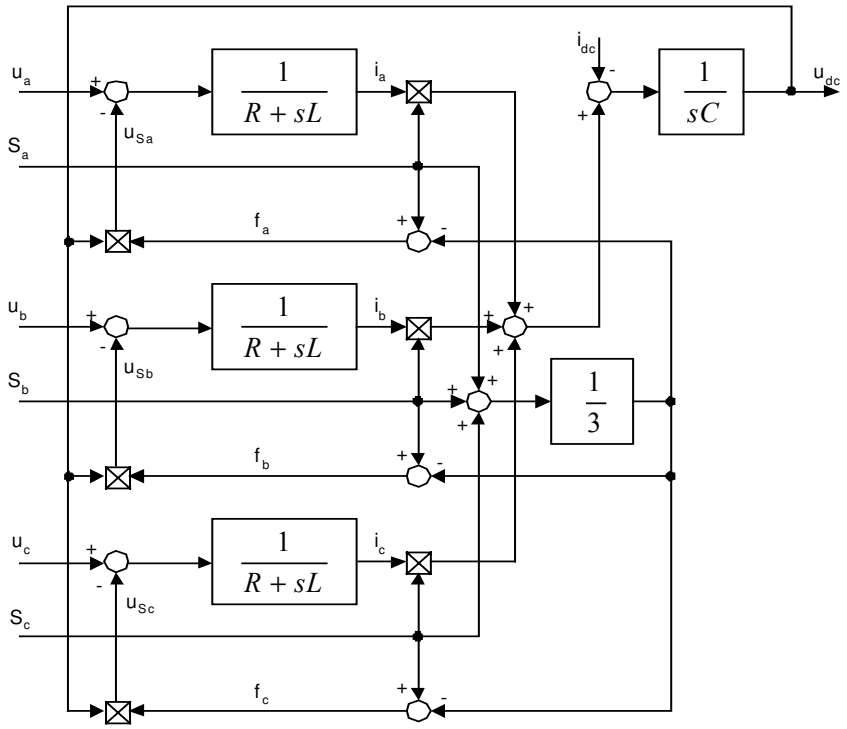


Fig. 2.10 Block diagram of voltage source PWM rectifier in natural three-phase coordinates

Model of PWM rectifier in stationary coordinates (α- β)

The voltage equation in the stationary α -β coordinates are obtained by applying (A.2.22a) to (2.15) and (2.16) and are written as:

$$\begin{bmatrix} u_{L\alpha} \\ u_{L\beta} \end{bmatrix} = R\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} + L\frac{d}{dt}\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} + \begin{bmatrix} u_{S_\alpha} \\ u_{S_\beta} \end{bmatrix} \tag{2.17}$$

and

$$C\frac{du_{dc}}{dt} = (i_{L\alpha}S_\alpha + i_{L\beta}S_\beta) - i_{dc} \tag{2.18}$$

where: $S_\alpha = \frac{1}{\sqrt{6}}(2S_a - S_b - S_c)$; $S_\beta = \frac{1}{\sqrt{2}}(S_b - S_c)$

A block diagram of α-β model is presented in Fig. 2.11.

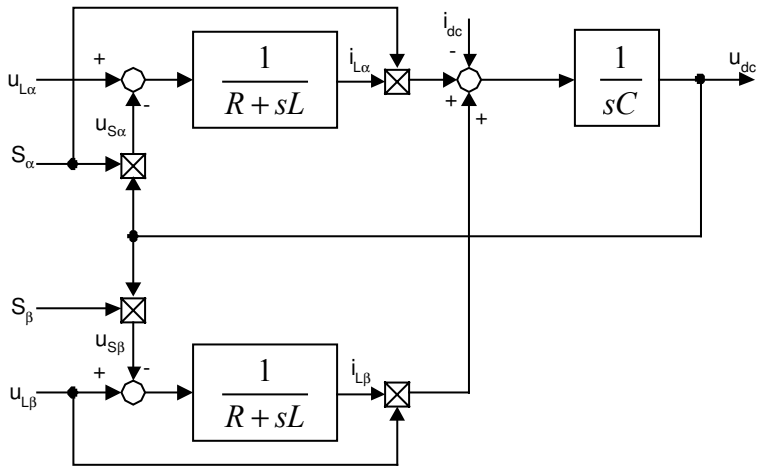


Fig. 2.11 Block diagram of voltage source PWM rectifier in stationary α-β coordinates

Model of PWM rectifier in synchronous rotating coordinates (d-q)
The equations in the synchronous *d-q* coordinates are obtained with the help of transformation 4.1a:

$$u_{Ld} = Ri_{Ld} + L\frac{di_{Ld}}{dt} - \omega L i_{Lq} + u_{Sd} \tag{2.19a}$$

$$u_{Lq} = Ri_{Lq} + L\frac{di_{Lq}}{dt} + \omega L i_{Ld} + u_{Sq} \tag{2.19b}$$

$$C\frac{du_{dc}}{dt} = (i_{Ld}S_d + i_{Lq}S_q) - i_{dc} \tag{2.20}$$

where: $S_d = S_\alpha \cos\omega t + S_\beta \sin\omega t$; $S_q = S_\beta \cos\omega t - S_\alpha \sin\omega t$

A block diagram of *d-q* model is presented in Fig. 2.12.

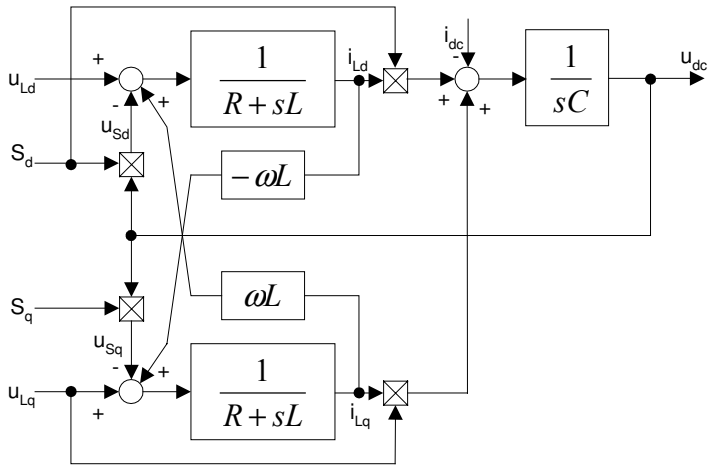


Fig. 2.12 Block diagram of voltage source PWM rectifier in synchronous d-q coordinates

R can be practically neglected because voltage drop on resistance is much lower than voltage drop on inductance, what gives simplified equations (2.14), (2.15), (2.17), (2.19).

$$\underline{u_L} = \frac{d\underline{i_L}}{dt}L + \underline{u_S} \tag{2.21}$$

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} u_{Sa} \\ u_{Sb} \\ u_{Sc} \end{bmatrix} \tag{2.22}$$

$$\begin{bmatrix} u_{L\alpha} \\ u_{L\beta} \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} + \begin{bmatrix} u_{S_\alpha} \\ u_{S_\beta} \end{bmatrix} \tag{2.23}$$

$$u_{Ld} = L\frac{di_{Ld}}{dt} - \omega L i_{Lq} + u_{Sd} \tag{2.24a}$$

$$u_{Lq} = L\frac{di_{Lq}}{dt} + \omega L i_{Ld} + u_{Sq} \tag{2.24b}$$

The active and reactive power supplied from the source is given by [see A.2]

$$p = \mathrm{Re}\left\{\underline{u} \cdot \underline{i}^*\right\} = u_\alpha i_\alpha + u_\beta i_\beta = u_a i_a + u_b i_b + u_c i_c \tag{2.25}$$

$$q = \mathrm{Im}\left\{\underline{u} \cdot \underline{i}^*\right\} = u_\beta i_\alpha - u_\alpha i_\beta = \frac{1}{\sqrt{3}}\left(u_{bc} i_a + u_{ca} i_b + u_{ab} i_c\right) \tag{2.26}$$

It gives in the synchronous *d-q* coordinates:

$$p = (u_{Lq} i_{Lq} + u_{Ld} i_{Ld}) = \frac{3}{2} E_m I_m \tag{2.27}$$

$$q = (u_{Lq} i_{Ld} - u_{Ld} i_{Lq}) \tag{2.28}$$

(if we make assumption of unity power factor, we will obtain following properties $i_{Lq} = 0$, $u_{Lq} = 0$, $u_{Ld} = \sqrt{\frac{3}{2}} E_m$, $i_{Ld} = \sqrt{\frac{3}{2}} I_m$, $q = 0$ (see Fig. 2.13)).

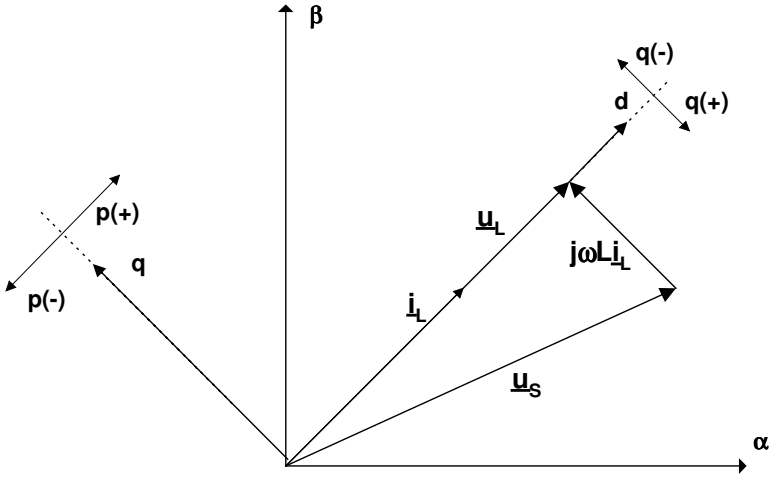


Fig. 2.13 Power flow in bi-directional AC/DC converter as dependency of $\underline{i_L}$ direction.

2.3.2 Steady-state properties and limitations

For proper operation of PWM rectifier a minimum DC-link voltage is required. Generally it can be determined by the peak of line-to-line supply voltage:

$$V_{dc\min} \rangle V_{LN(rms)} * \sqrt{3} * \sqrt{2} = 2{,}45 * V_{LN(rms)} \tag{2.29}$$

It is true definition but not concern all situations. Other publication [36,37] defines minimum voltage but do not take into account line current (power) and line inductors. The determination of this voltage is more complicated and is presented in [59].
Equations (2.24) can be transformed to vector form in synchronous d-q coordinates defining derivative of current as:

$$L\frac{d\underline{i}_{Ldq}}{dt} = \underline{u}_{Ldq} - j\omega L\underline{i}_{Ldq} - \underline{u}_{Sdq}\,. \tag{2.30}$$

Equation (2.30) defines direction and rate of current vector movement. Six active vectors ($U_{1\text{-}6}$) of input voltage in PWM rectifier rotate clockwise in synchronous *d-q* coordinates. For vectors U_0, U_1, U_2, U_3, U_4, U_5, U_6, U_7 the current derivatives are denoted respectively as U_{p0}, U_{p1}, U_{p2}, U_{p3}, U_{p4}, U_{p5}, U_{p6}, U_{p7} (Fig. 2.14).

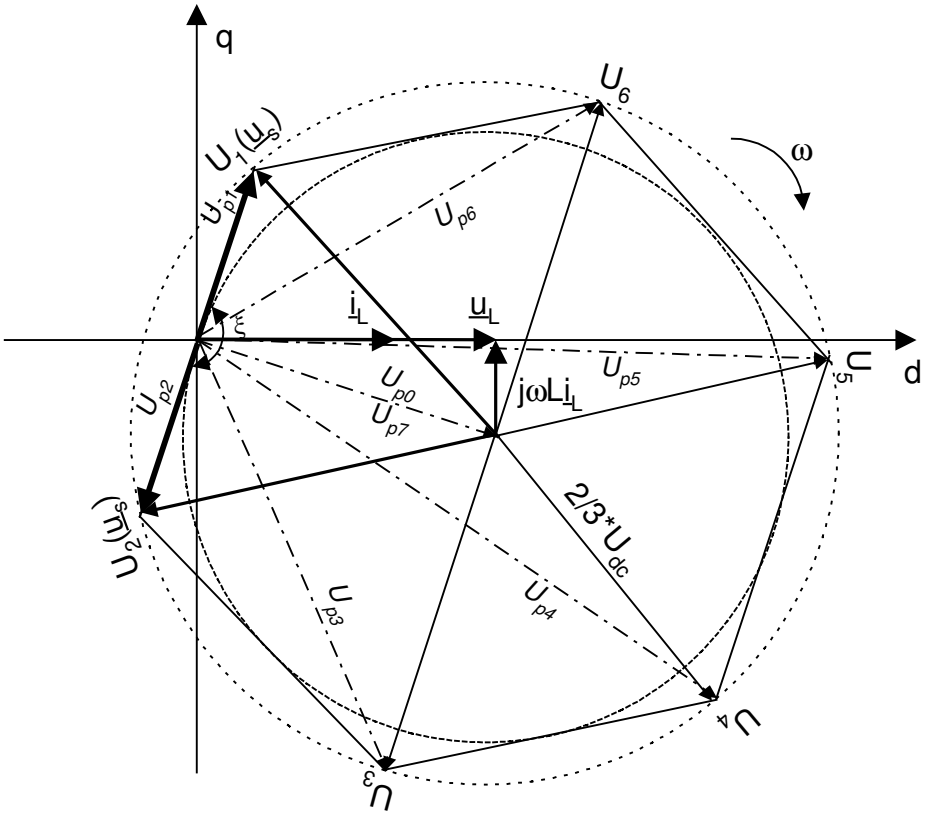


Fig. 2.14 Instantaneous position of vectors

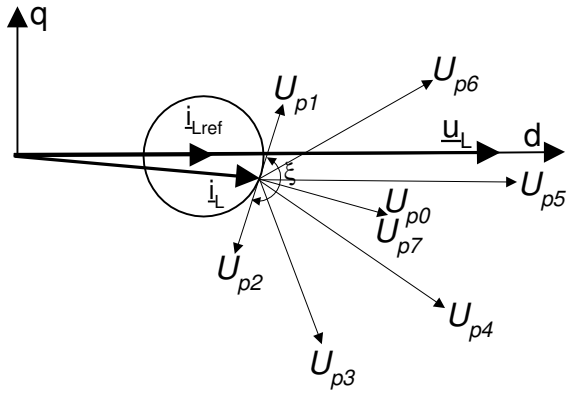


Fig. 2.15 Limitation for operation of PWM rectifier

The full current control is possible when the current is kept in specified error area (Fig. 2.15). Fig. 2.14 and Fig. 2.15 presents that any vectors can force current vector inside error area when angle created by vectors U_{p1} and U_{p2} is $\xi \leq \pi$. It results from trigonometrical condition that vectors U_{p1}, U_{p2}, U_1 and U_2 form an equilateral triangle for $\xi = \pi$ where $\underline{u}_{Ldq} - j\omega L\underline{i}_{Ldq}$ is an altitude. Therefore, from simple trigonometrical relationship, it is possible to define boundary condition as:

$$\left|\underline{u}_{Ldq} - j\omega L\underline{i}_{Ldq}\right| = \frac{\sqrt{3}}{2}\underline{u}_{sdq} \tag{2.31}$$

and after transformation, assumpting that $\underline{u}_{Sdq} = 2/3U_{dc}$, $\underline{u}_{Ldq} = E_m$, $\underline{i}_{Ldq} = i_{Ld}$ (for *UPF*) we get condition for minimal DC-link voltage:

$$u_{dc} \rangle \sqrt{3\left[E_m^2 + (\omega L i_{Ld})^2\right]} \quad \text{and } \xi > \pi\,. \tag{2.32}$$

Above equation shows relation between supply voltage (usually constant), output dc voltage, current (load) and inductance. It also means that sum of vector $\underline{u}_{Ldq} - j\omega L\underline{i}_{Ldq}$ should not exceed linear region of modulation i.e. circle inscribed in the hexagon (see Section 4.4).

The inductor has to be designed carefully because low inductance will give a high current ripple and will make the design more depending on the line impedance. The high value of inductance will give a low current ripple, but simultaneously reduce the operation range of the rectifier. The voltage drop across the inductance has influence for the line current. This voltage drop is controlled by the input voltage of the PWM rectifier but maximal value is limited by the DC-link voltage. Consequently, a high current (high power) through the inductance requires either a high DC-link voltage or a low inductance (low impedance). Therefore, after transformation of equation (2.32) the maximal inductance can be determinate as:

$$L \langle \frac{\sqrt{\frac{u_{dc}^2}{3} - E_m^2}}{\omega i_{Ld}}\,. \tag{2.33}$$

2.4 SENSORLESS OPERATION

Normally, the PWM rectifier needs three kinds of sensors:

- DC-voltage sensor (1 sensor)
- AC-line current sensors (2 or 3 sensors)
- AC-line voltage sensors (2 or 3 sensors)

The sensorless methods provide technical and economical advantages to the system as: simplification, isolation between the power circuit and control system, reliability and cost effectiveness. The possibility to reduce the number of the expensive sensors have been studied especially in the field of motor drive application [1], but the rectifier application differ from the inverter operation in the following reasons:

- Zero vector will shorted the line power,
- The line operates at constant frequency 50Hz and synchronization is necessary.

The most used solution for reducing of sensors include:

- AC voltage and current sensorless,
- AC current sensorless,
- AC voltage sensorless.

AC voltage and current sensorless

Reductions of current sensors especially for AC drives are well known [1]. The two-phase currents may be estimated based on information of DC link current and reference voltage vector in every PWM period. No fully protection is main practical problem in the system. Particularly for PWM rectifier the zero vectors (U_0, U_7) presents no current in DC-link and three line phases are short circuit simultaneously. New improved method presented in [30, 115] is to sample DC-link current few times in one switching period. Basic principle of current reconstruction is shown in Fig. 2.16 together with a voltage vector's patterns determining the direction of current flow. One active voltage vector takes it to reconstruct one phase current and another voltage vector is used to reconstruct a second phase current using values measured from DC current sensor. A relationship between the applied active vectors and the phase currents measured from DC link sensor is shown in TABLE 2.2, which is based on eight voltage vectors composed of six active vectors and two zero vectors.

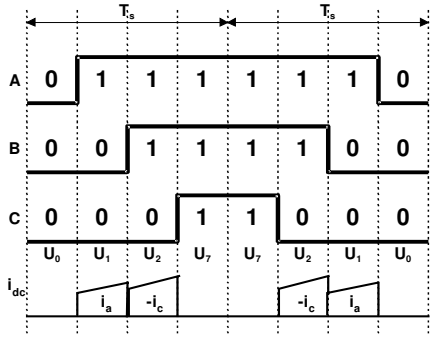


Fig. 2.16 PWM signals and DC link current in sector I

Table 2.2 Relationship between voltage vectors of converter, DC-link current and line currents.

Voltage Vector	DC link current i_{dc}
$U_1(100)$	$+i_a$
$U_2(110)$	$-i_c$
$U_3(010)$	$+i_b$
$U_4(011)$	$-i_a$
$U_5(001)$	$+i_c$
$U_6(101)$	$-i_b$
$U_0(000)$	0
$U_7(111)$	0

The main problem of AC current estimation based on minimum pulse-time for DC-link current sampling. It appears when either of two active vectors is not present, or is applied only for a short time. In such a case, it is impossible to reconstruct phase current. This occur in the case of reference voltage vectors passing one of the six possible active vectors or a low modulation index (Fig. 2.17). The minimum short time to obtain a correct estimation depends on the rapidness of the system, delays, cable length and *dead-time* [30]. The way to solve the problem is to adjust the PWM-pulses or to allow that no currents information is present in some time period. Therefore improved compensation consists of calculating the error, which are introduced by the PWM pulse adjustment and then compensate this error in the next switching period.

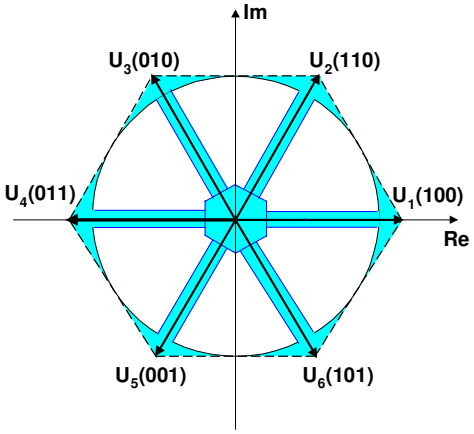


Fig. 2.17. Voltage vector area requiring the adjustment of PWM signals, when a reference voltage passes one of possible six active vectors and in case of low modulation index and overmodulation

The AC voltage and current sensorless methods in spite of cost reduction posses several disadvantages: higher contents of current ripple, problems with discontinuous modulation and overmodulation mode [see Section 4.4], sampling is presented few times per switching state what is not technically convenient, unbalance and start up condition are not reported.

AC current sensorless

This very simple solution based on inductor voltage (u_l) measurement in two lines. Supply voltage can be estimated with assumption that voltage on inductance is equal to line voltage when the zero-vector occurs in converter (Fig. 2.18)

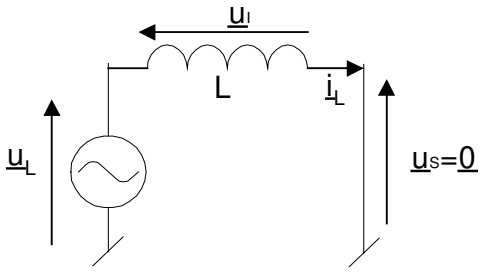


Fig. 2.18. PWM rectifier circuit when the zero voltage vector is applied.

On the basis of the inductor voltage described in equation (2.34)

$$u_{IR} = L\frac{di_{LR}}{dt} \tag{2.34}$$

the line current can be calculated as:

$$i_{LR} = \frac{1}{L}\int u_{IR}dt \tag{2.35}$$

Thanks to equation (2.35) the observed current will not be affected by derivation noise, but it directly reduces the dynamic of the control. This gains problems with over-current protection

AC voltage sensorless

Previous solutions present some over voltage and over current protection troubles. Therefore the *DC*-voltage and the *AC*-line current sensors are an important part of the over-voltage and over-current protection, while it is possible to replace the *AC*-line voltage sensors with a line voltage estimator or virtual flux estimator what is described in next point.

2.5 VOLTAGE AND VIRTUAL FLUX ESTIMATION

Line voltage estimator [44]

An important requirement for a voltage estimator is to estimate the voltage correct also under unbalanced conditions and pre-existing harmonic voltage distortion. Not only the fundamental component should be estimated correct, but also the harmonic components and the voltage unbalance. It gives a higher total power factor [21]. It is possible to calculate the voltage across the inductance by the current differentiating. The line voltage can then be estimated by adding reference of the rectifier input voltage to the calculated voltage drop across the inductor [52]. However, this approach has the disadvantage that the current is differentiated and noise in the current signal is gained through the differentiation. To prevent this a voltage estimator based on the power estimator of [21] can be applied. In [21] the current is sampled and the power is estimated several times in every switching state.

In conventional space vector modulation (SVM) for three-phase voltage source converters, the *AC* currents are sampled during the zero-vector states because no switching noise is present and a filter in the current feedback for the current control loops can be avoided. Using equation (2.36) and (2.37) the estimated active and reactive power in this special case (zero states) can be expressed as:

$$p = L\left(\frac{di_a}{dt}i_a + \frac{di_b}{dt}i_b + \frac{di_c}{dt}i_c\right) = 0 \tag{2.36}$$

$$q = \frac{3L}{\sqrt{3}}\left(\frac{di_a}{dt}i_c - \frac{di_c}{dt}i_a\right). \tag{2.37}$$

It should be noted that in this special case it is only possible to estimate the reactive power in the inductor. Since powers are *DC*-values it is possible to prevent the noise of the differentiated current by use of a simple (digital) low pass filter. This ensures a robust and noise insensitive performance of the voltage estimator.
Based on instantaneous power theory, the estimated voltages across the inductance is:

$$\begin{bmatrix} u_{I\alpha} \\ u_{I\beta} \end{bmatrix} = \frac{1}{i_{L\alpha}^2 + i_{L\beta}^2} \begin{bmatrix} i_{L\alpha} & -i_{L\beta} \\ i_{L\beta} & i_{L\alpha} \end{bmatrix} \begin{bmatrix} 0 \\ q \end{bmatrix} \tag{2.38}$$

where:
$u_{I\alpha}$, $u_{I\beta}$ are the estimated values of the three-phase voltages across the inductance L, in the fixed α-β coordinates.

The estimated line voltage $u_{L(est)}$ can now be found by adding the voltage reference of the PWM rectifier to the estimated inductor voltage [44].

$$\underline{u}_{L(est)} = \underline{u}_S + \underline{u}_I \tag{2.39}$$

Virtual flux estimator
The voltage imposed by the line power in combination with the AC side inductors are assumed to be quantities related to a virtual AC motor as shown in Fig. 2.19.

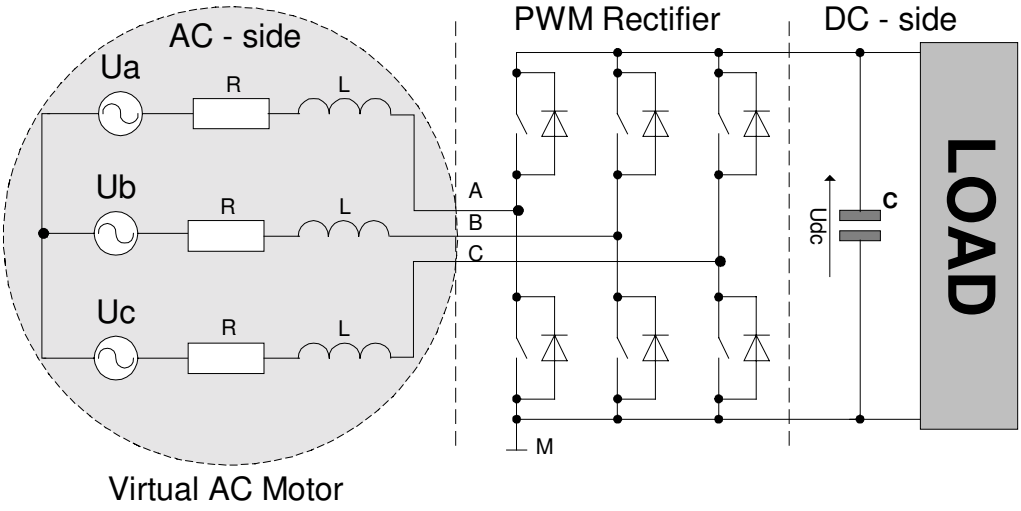


Fig. 2.19. Three-phase PWM rectifier system with AC-side presented as virtual AC motor

Thus, R and L represent the stator resistance and the stator leakage inductance of the virtual motor and phase-to-phase line voltages: U_{ab}, U_{bc}, U_{ca} would be induced by a virtual air gap flux. In other words the integration of the voltages leads to a virtual line flux vector $\underline{\Psi}_L$, in stationary α-β coordinates (Fig. 2.20).

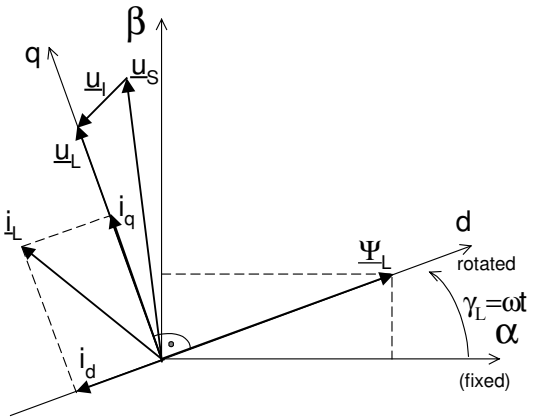


Fig. 2.20. Reference coordinates and vectors
$\underline{\Psi}_L$ – virtual line flux vector, $\underline{u}_S$ – converter voltage vector, $\underline{u}_L$ - line voltage vector, $\underline{u}_I$ – inductance voltage vector, $\underline{i}_L$ – line current vector

Similarly to Eq. (2.39) a virtual flux equation can be presented as [65, 102] (Fig. 2.21):

$$\underline{\psi}_{L(est)} = \underline{\psi}_S + \underline{\psi}_I \tag{2.40}$$

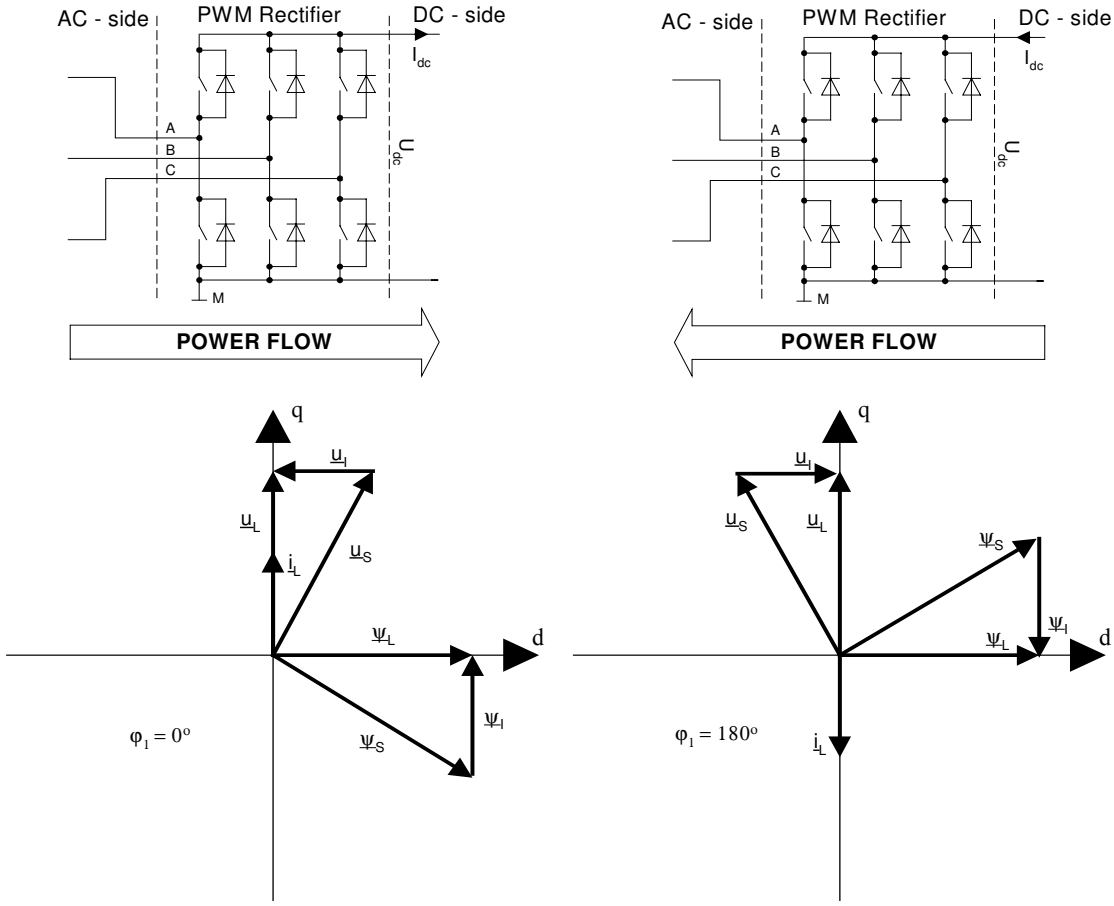


Fig. 2.21 Relation between voltage and flux for different power flow direction in PWM rectifier.

Based on the measured DC-link voltage U_{dc} and the converter switch states S_a, S_b, S_c the rectifier input voltages are estimated as follows

$$u_{S\alpha} = \sqrt{\frac{2}{3}} U_{dc} (S_a - \frac{1}{2}(S_b + S_c)) \tag{2.41a}$$

$$u_{S\beta} = \frac{1}{\sqrt{2}} U_{dc} (S_b - S_c) \tag{2.41b}$$

Then, the virtual flux $\underline{\Psi_L}$ components are calculated from the (2.41) in stationary (α-β) coordinates system

$$\Psi_{L\alpha(est)} = \int (u_{S\alpha} + L \frac{di_{L\alpha}}{dt}) dt \tag{2.42a}$$

$$\Psi_{L\beta(est)} = \int (u_{S\beta} + L \frac{di_{L\beta}}{dt}) dt \tag{2.42b}$$

The virtual flux components calculation is shown in Fig. 2.22.

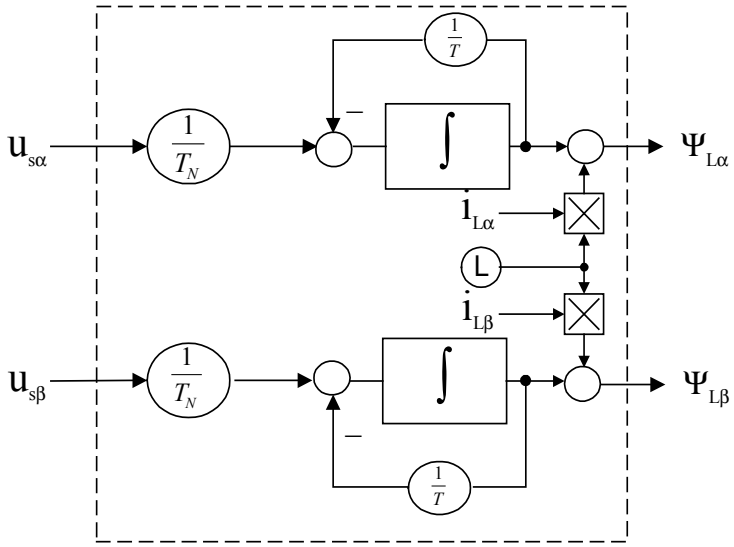


Fig. 2.22. Block scheme of virtual flux estimator with first order filter.

3. VOLTAGE AND VIRTUAL FLUX BASED DIRECT POWER CONTROL

3.1 INTRODUCTION

Control of PWM rectifier can be considered as a dual problem to vector control of an induction motor (Fig. 3.1) [4,110]. Various control strategies have been proposed in recent works on this type PWM converter. Although these control strategies can achieve the same main goals, such as the high power factor and near-sinusoidal current waveforms, their principles differ. Particularly, the Voltage Oriented Control (*VOC*), which guarantees high dynamics and static performance via an internal current control loops, has become very popular and has constantly been developed and improved [46, 48], [51], [53-54]. Consequently, the final configuration and performance of the *VOC* system largely depends on the quality of the applied current control strategy [6]. Another control strategy called Direct Power Control (*DPC*) is based on the instantaneous active and reactive power control loops [21], [22]. In *DPC* there are no internal current control loops and no *PWM* modulator block, because the converter switching states are selected by a switching table based on the instantaneous errors between the commanded and estimated values of active and reactive power. Therefore, the key point of the *DPC* implementation is a correct and fast estimation of the active and reactive line power.

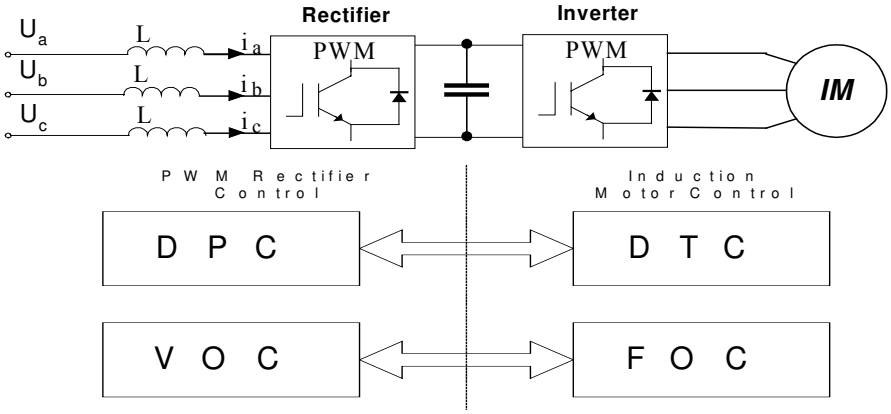


Fig.3.1 Relationship between control of PWM line rectifier and PWM inverter – fed *IM*

The control techniques for PWM rectifier can be generally classified as voltage based and virtual flux based, as shown in Fig. 3.2. The virtual flux based method corresponds to direct analogy of *IM* control.

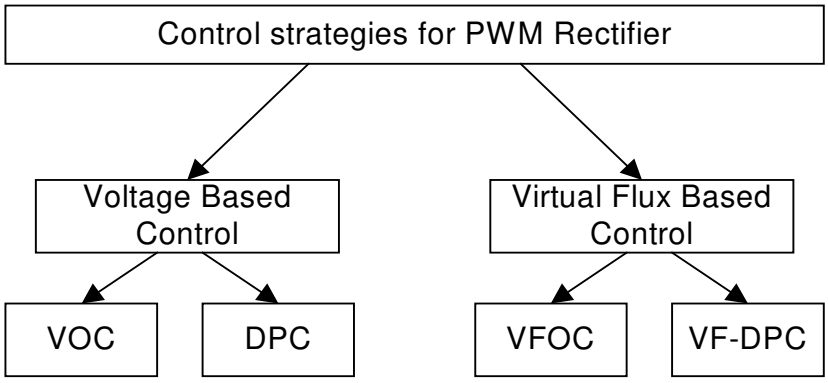


Fig. 3.2 Classification of control methods for PWM rectifier

3.2 BASIC BLOCK DIAGRAM OF DIRECT POWER CONTROL (DPC)

The main idea of *DPC* proposed in [22] and next developed by [21] is similar to the well-known Direct Torque Control (*DTC*) for induction motors. Instead of torque and stator flux the instantaneous active (*p*) and reactive (*q*) powers are controlled (Fig. 3.3).

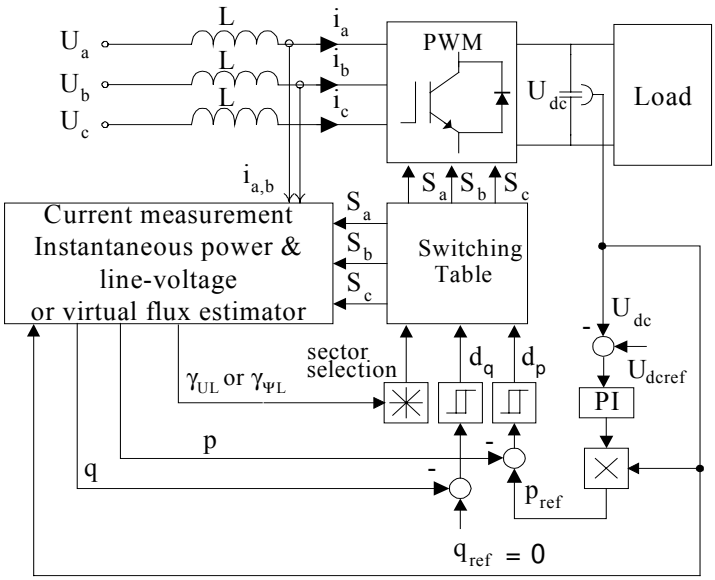


Fig. 3.3 Block scheme of DPC.

The commands of reactive power q_{ref} (set to zero for unity power factor) and active power p_{ref} (delivered from the outer *PI-DC* voltage controller) are compared with the estimated q and p values (described in section 3.3 and 3.4), in reactive and active power hysteresis controllers, respectively.

The digitized output signal of the reactive power controller is defined as:

$$d_q = 1 \text{ for } q < q_{ref} - H_q \quad (3.1a)$$
$$d_q = 0 \text{ for } q > q_{ref} + H_q, \quad (3.1b)$$

and similarly of the active power controller as

$$d_p = 1 \text{ for } p < p_{ref} - H_p \quad (3.2a)$$
$$d_p = 0 \text{ for } p > p_{ref} + H_p, \quad (3.2b)$$

where: H_q & H_p are the hysteresis bands.

The digitized variables d_p, d_q and the voltage vector position $\gamma_{UL} = arc\ tg\ (u_{L\alpha}/u_{L\beta})$ or flux vector position $\gamma_{\Psi L} = arc\ tg\ (\psi_{L\alpha}/\psi_{L\beta})$ form a digital word, which by accessing the address of the look-up table selects the appropriate voltage vector according to the switching table (described in section 3.5).

The region of the voltage or flux vector position is divided into twelve sectors, as shown in Fig. 3.5 and the sectors can be numerically expressed as:

$$(n-2)\frac{\pi}{6} \le \gamma_n < (n-1)\frac{\pi}{6} \quad \text{where } n = 1, 2...12 \quad (3.3)$$

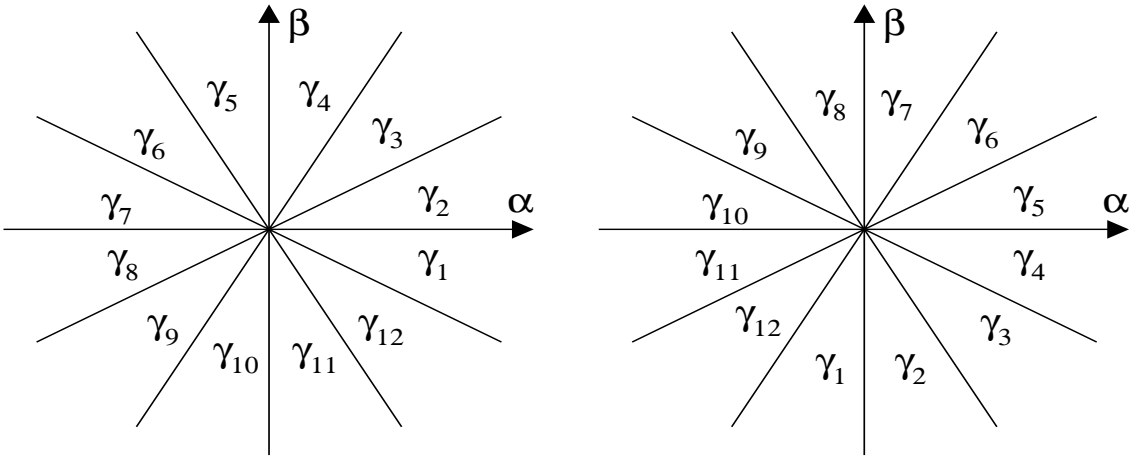


Fig. 3.5 Sector selection for DPC and VF-DPC

Note, that the sampling frequency has to be about few times higher than the average switching frequency. This very simple solution allows precisely control of instantaneous active and reactive power and errors are only limited by the hysteresis band. No transformation into rotating coordinates is needed and the equations are easy implemented. This method deals with instantaneous variables, therefore, estimated values contain not only a fundamental but also harmonic components. This feature also improves the total power factor and efficiency [21].

Further improvements regarding VF-DPC operation can be achieved by using sector detection with *PLL* (Phase-Locked Loop) generator instead of zero crossing voltage detector (Fig. 3.6). This guarantees a very stable and free of disturbances sector detection, even under operation with distorted and unbalanced line voltages (Fig.3.19).

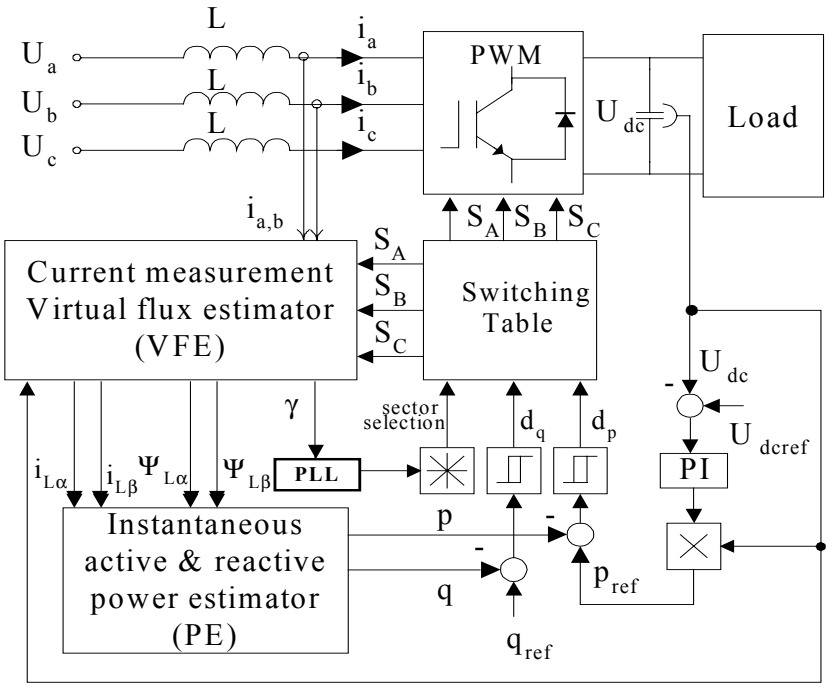


Fig. 3.6. Block scheme of *VF-DPC* with *PLL* generator

3.3 INSTANTANEOUS POWER ESTIMATION BASED ON THE LINE VOLTAGE

The main idea of voltage based power estimation for DPC was proposed in [21-22]. The instantaneous active and reactive powers are defined by the product of the three phase voltages and currents (2.25-2.26). The instantaneous values of active (p) and reactive power (q) in AC voltage sensorless system are estimated by Eqs. (3.8) and (3.9). The active power p is the scalar product of the current and the voltage, whereas the reactive power q is calculated as a vector product of them. The first part of both equations represents power in the inductance and the second part is the power of the rectifier.

$$p = L\left(\frac{di_a}{dt}i_a + \frac{di_b}{dt}i_b + \frac{di_c}{dt}i_c\right) + U_{dc}(S_a i_a + S_b i_b + S_c i_c) \tag{3.8}$$

$$q = \frac{1}{\sqrt{3}}\{3L\left(\frac{di_a}{dt}i_c - \frac{di_c}{dt}i_a\right) - U_{dc}[S_a(i_b - i_c) + S_b(i_c - i_a) + S_c(i_a - i_b)]\} \tag{3.9}$$

As can be seen in (3.8) and (3.9), the form of equations have to be changed according to the switching state of the converter, and both equations require the knowledge of the line inductance L. Supply voltage usually is constant, therefore the instantaneous active and reactive powers are proportional to the i_{Ld} and i_{Lq}.

The *AC*-line voltage sector is necessary to read the switching table, therefore knowledge of the line voltage is essential. However, once the estimated values of active and reactive power are calculated and the *AC*-line currents are known, the line voltage can easily be calculated from instantaneous power theory as:

$$\begin{bmatrix} u_{L\alpha} \\ u_{L\beta} \end{bmatrix} = \frac{1}{i_{L\alpha}^2 + i_{L\beta}^2} \begin{bmatrix} i_{L\alpha} & -i_{L\beta} \\ i_{L\beta} & i_{L\alpha} \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix} \tag{3.10}$$

The instantaneous power and AC voltage estimators are shown in Fig. 3.7.

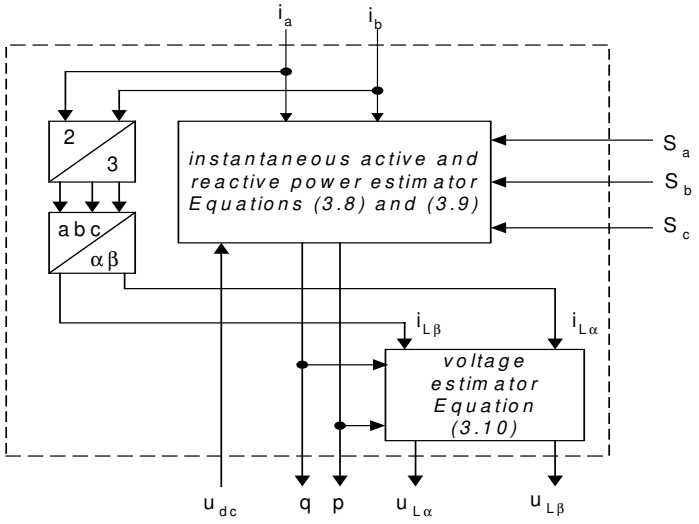


Fig. 3.7 Instantaneous power estimator based on line voltage.

In spite of the simplicity, this power estimation method has several disadvantages such as:

- high values of the line inductance and sampling frequency are needed (important point for the estimator, because a smooth shape of current is needed).
- power estimation depends on the switching state. Therefore, calculation of the power and voltage should be avoided at the moment of switching, because of high estimation errors.

3.4 INSTANTANEOUS POWER ESTIMATION BASED ON THE VIRTUAL FLUX

The Virtual Flux (*VF*) based approach has been proposed by Author to improve the *VOC* [42, 56]. Here it will be applied for instantaneous power estimation, where voltage imposed by the line power in combination with the *AC* side inductors are assumed to be quantities related to a virtual *AC* motor as shown in section 2.5.

With the definitions

$$\underline{\Psi}_L = \int \underline{u}_L dt \tag{3.11}$$

where

$$\underline{u}_L = \begin{bmatrix} u_{L\alpha} \\ u_{L\beta} \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1 & 1/2 \\ 0 & \sqrt{3}/2 \end{bmatrix} \begin{bmatrix} u_{ab} \\ u_{bc} \end{bmatrix} \tag{3.12}$$

$$\underline{\Psi}_L = \begin{bmatrix} \Psi_{L\alpha} \\ \Psi_{L\beta} \end{bmatrix} = \begin{bmatrix} \int u_{L\alpha} dt \\ \int u_{L\beta} dt \end{bmatrix} \tag{3.13}$$

$$\underline{i}_L = \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 3/2 & 0 \\ \sqrt{3}/2 & \sqrt{3} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \end{bmatrix} \tag{3.14}$$

$$\underline{u}_S = \underline{u}_{conv} = \begin{bmatrix} u_{s\alpha} \\ u_{s\beta} \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} u_{AM} \\ u_{BM} \\ u_{CM} \end{bmatrix} \tag{3.15}$$

the voltage equation can be written as

$$\underline{u}_L = R\underline{i}_L + \frac{d}{dt}(L\underline{i}_L + \underline{\Psi}_S)\,. \tag{3.16a}$$

In practice, R can be neglected, giving

$$\underline{u}_L = L\frac{d\underline{i}_L}{dt} + \frac{d}{dt}\underline{\Psi}_S = L\frac{d\underline{i}_L}{dt} + \underline{u}_S \tag{3.16b}$$

Using complex notation, the instantaneous power can be calculated as follows:

$$p = \mathrm{Re}(\underline{u}_L \cdot \underline{i}_L^{\,*}) \tag{3.17a}$$

$$q = \mathrm{Im}(\underline{u}_L \cdot \underline{i}_L^{\,*}) \tag{3.17b}$$

where * denotes the conjugate line current vector. The line voltage can be expressed by the virtual flux as

$$\underline{u}_L = \frac{d}{dt}\underline{\Psi}_L = \frac{d}{dt}(\Psi_L e^{j\omega t}) = \frac{d\Psi_L}{dt}e^{j\omega t} + j\omega\Psi_L e^{j\omega t} = \frac{d\Psi_L}{dt}e^{j\omega t} + j\omega\underline{\Psi}_L \quad (3.18)$$

where $\underline{\Psi}_L$ denotes the space vector and Ψ_L its amplitude. For the virtual flux oriented *d-q* coordinates (Fig. 2.20), $\underline{\Psi}_L = \Psi_{Ld}$, and the instantaneous active power can be calculated from (3.17a) and (3.18) as

$$p = \frac{d\Psi_{Ld}}{dt} i_{Ld} + \omega\Psi_{Ld} i_{Lq} \quad (3.19)$$

For sinusoidal and balanced line voltages, equation (3.19) is reduced to

$$\frac{d\Psi_{Ld}}{dt} = 0 \quad (3.20)$$

$$p = \omega\Psi_{Ld} i_{Lq} \quad (3.21)$$

which means that only the current components orthogonal to the flux $\underline{\Psi}_L$ vector, produce the instantaneous active power. Similarly, the instantaneous reactive power can be calculated as:

$$q = -\frac{d\Psi_{Ld}}{dt} i_{Lq} + \omega\Psi_{Ld} i_{Ld} \quad (3.22)$$

and with (3.20) it is reduced to:

$$q = \omega\Psi_{Ld} i_{Ld} \quad (3.23)$$

However, to avoid coordinate transformation into *d-q* coordinates, the power estimator for the *DPC* system should use stator-oriented quantities, in α-β coordinates (Fig.2.20).

Using (3.17) and (3.18)

$$\underline{u}_L = \left.\frac{d\Psi_L}{dt}\right|_\alpha + j\left.\frac{d\Psi_L}{dt}\right|_\beta + j\omega\left(\Psi_{L\alpha} + j\Psi_{L\beta}\right) \quad (3.24)$$

$$\underline{u}_L \underline{i}_L^* = \left\{\left.\frac{d\Psi_L}{dt}\right|_\alpha + j\left.\frac{d\Psi_L}{dt}\right|_\beta + j\omega\left(\Psi_{L\alpha} + j\Psi_{L\beta}\right)\right\}\left(i_{L\alpha} - j i_{L\beta}\right) \quad (3.25)$$

That gives

$$p = \left\{\left.\frac{d\Psi_L}{dt}\right|_\alpha i_{L\alpha} + \left.\frac{d\Psi_L}{dt}\right|_\beta i_{L\beta} + \omega\left(\Psi_{L\alpha} i_{L\beta} - \Psi_{L\beta} i_{L\alpha}\right)\right\} \quad (3.26a)$$

and

$$q = \left\{-\left.\frac{d\Psi_L}{dt}\right|_\alpha i_{L\beta} + \left.\frac{d\Psi_L}{dt}\right|_\beta i_{L\alpha} + \omega\left(\Psi_{L\alpha} i_{L\alpha} + \Psi_{L\beta} i_{L\beta}\right)\right\}. \quad (3.26b)$$

For sinusoidal and balanced line voltage the derivatives of the flux amplitudes are zero. The instantaneous active and reactive powers can be computed as [17-19]

$$p = \omega \cdot (\Psi_{L\alpha} i_{L\beta} - \Psi_{L\beta} i_{L\alpha}) \tag{3.27a}$$

$$q = \omega \cdot (\Psi_{L\alpha} i_{L\alpha} + \Psi_{L\beta} i_{L\beta}) . \tag{3.27b}$$

The measured line currents i_a, i_b and the estimated virtual flux components $\Psi_{L\alpha}, \Psi_{L\beta}$ are delivered to the instantaneous power estimator block (*PE*) as depicted in Fig. 3.8.

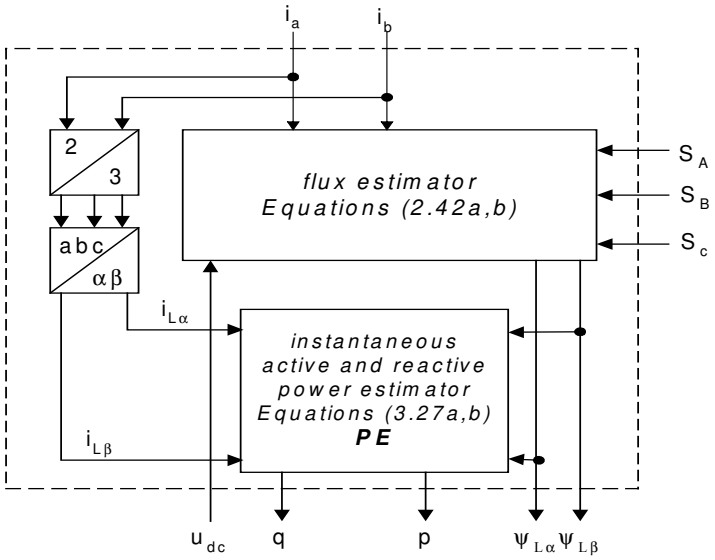


Fig. 3.8 Instantaneous power estimator based on virtual flux

3.5 SWITCHING TABLE

It can be seen in Fig. 3.9, that the instantaneous active and reactive power depends on position of converter voltage vector. It has indirect influence on inductance voltage as well as phase and amplitude of line current. Therefore, different pattern of switching table can be applied to direct control (*DTC, DPC*). It influence control condition as: instantaneous power and current ripple, switching frequency and dynamic performance. Some works, propose different switching tables for *DTC* but we cannot find too much reference for *DPC*. For drives exist more switching table techniques because of wide range of output frequency and dynamic demands [24-29]. For PWM rectifier we have constant line frequency and only instantaneous power varies. Fig. 3.9 presents four different situations, which illustrate the variations of instantaneous power. Point *M* presents reference values of active and reactive power.

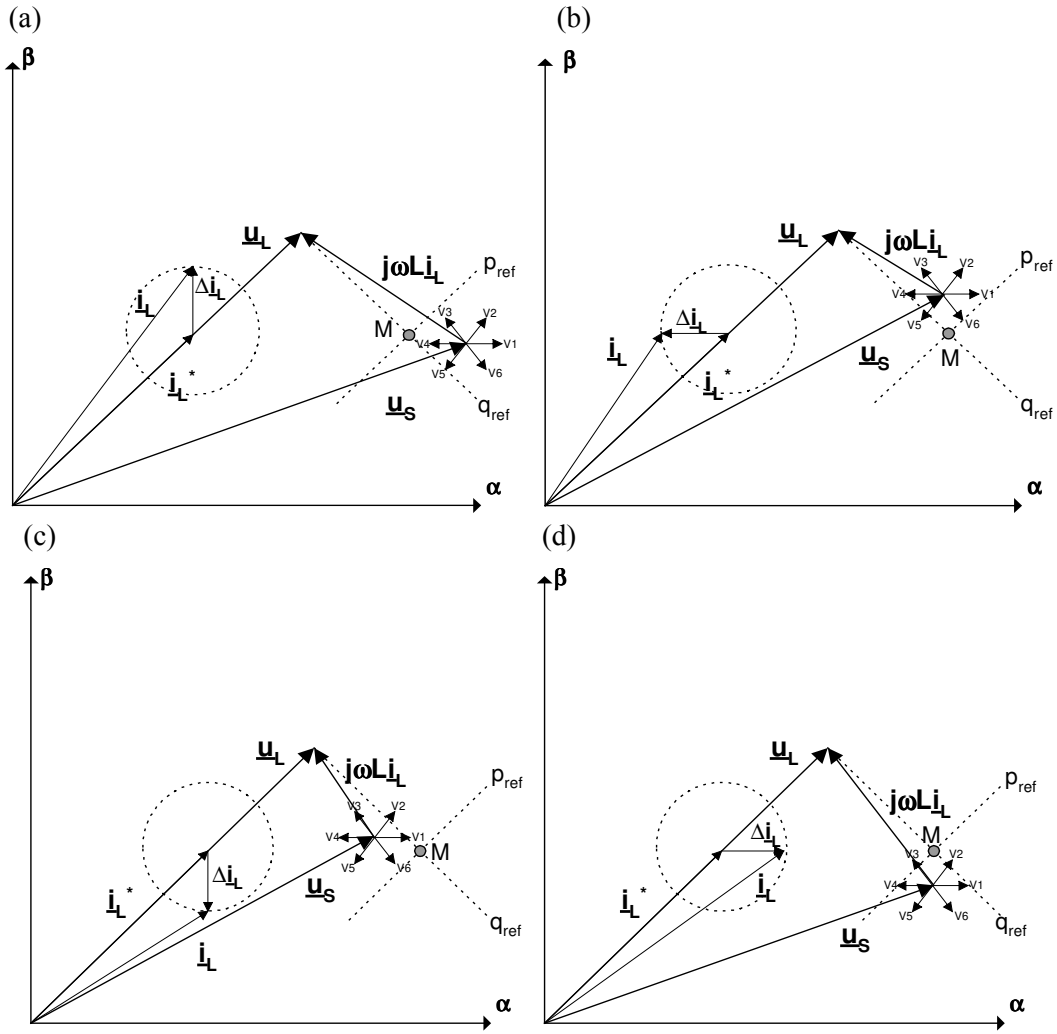


Fig. 3.9 Instantaneous power variation:
a) $p_{ref}<p$, $q_{ref}>q$ (0,1); b) $p_{ref}>p$, $q_{ref}>q$ (1,1); c) $p_{ref}>p$, $q_{ref}<q$ (1,0); d) $p_{ref}<p$, $q_{ref}<q$ (0,0);

The selection of vector is made so that the error between q and q_{ref} should be within the limits (Eqs. (3.1),(3.2)). It depends not only on the error of the amplitude but also the direction of q as shown in Fig. 3.10.

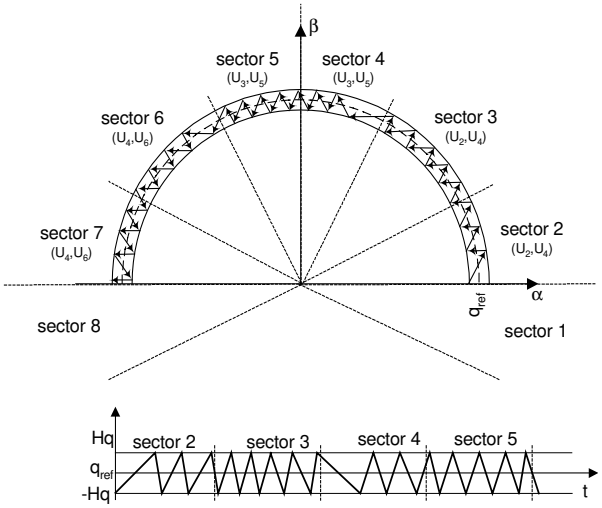


Fig.3.10 Selection of voltage vectors for **q**

Some behaviour of *DPC* are not satisfactory. For instance when the instantaneous reactive power vector is close to one of sector boundary, two of four possible active vectors are wrong. These wrong vectors can only change the instantaneous active power without correction of the reactive power error. This is easy visible on a current. A few methods to improve the *DPC* behaviour in the sector bonders is well known. One of them is to add more sectors or hysteresis levels. Therefore, switching table are generally constructed with difference in:

- number of sectors,
- dynamic performance,
- two and three level hysteresis controllers.

Number of sectors

Usually the vectors plane is divided for 6 (3. 28) or 12 (3. 29) sectors (Fig. 3.11). It has influence for switching table construction (Table 3.1).

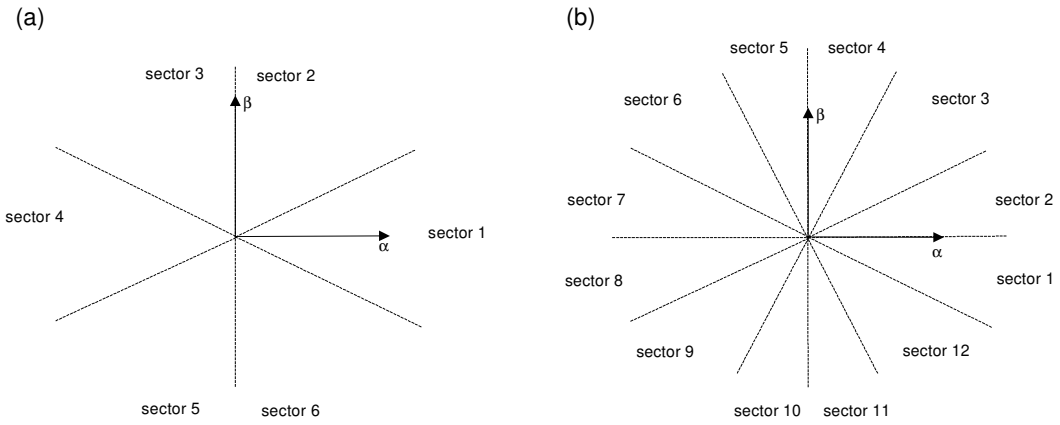


Fig. 3.11 Voltage plane with a) 6 sectors b) 12 sectors

$$(2n-3)\frac{\pi}{6} \le \gamma_n < (2n-1)\frac{\pi}{6} \qquad n = 1, 2, ..., 6 \qquad (3.28)$$

$$(n-2)\frac{\pi}{6} \le \gamma_n < (n-1)\frac{\pi}{6} \qquad n = 1, 2, ..., 12 \qquad (3.29)$$

Table 3.1.b Switching table for 6 sectors

d_p	d_q	Sector A
1	0	U_B
	1	U_0
0	0	U_B
	1	U_A
U_A=U_1(100),U_2(110),U_3(010),U_4(011),U_5(001),U_6(101) U_B=U_6(101),U_1(100),U_2(110),U_3(010),U_4(011),U_5(001) U_0=U_0(000),U_7(111)		

Table 3.1.a Switching table for 12 sectors

d_p	d_q	Sector A	Sector B
1	0	U_B	U_7
	1	U_0	U_7
0	0	U_B	
	1	U_A	
U_A=U_1(100),U_2(110),U_3(010),U_4(011),U_5(001),U_6(101) U_B=U_6(101),U_1(100),U_2(110),U_3(010),U_4(011),U_5(001) U_0=U_0(000),U_7(111)			

When region of the voltage vector position is divided into twelve sectors, the area between adjoining vectors contain two sectors. Sector *A* is located closer to U_A and sector *B* closer to U_B.

Hysteresis controllers

The wide of the instantaneous active and reactive hysteresis band have a relevant effect on the converter performance. In particular, the harmonic current distortion, the average converter switching frequency, the power pulsation and the losses are strongly affected by the hysteresis wide. The controllers proposed by [21] in classical *DPC* are two level comparators for instantaneous active and reactive power (Fig 3.12a). Three level comparators can provide further improvements. Possible combinations of hysteresis controllers for active and reactive power are presented in Fig. 3.12.

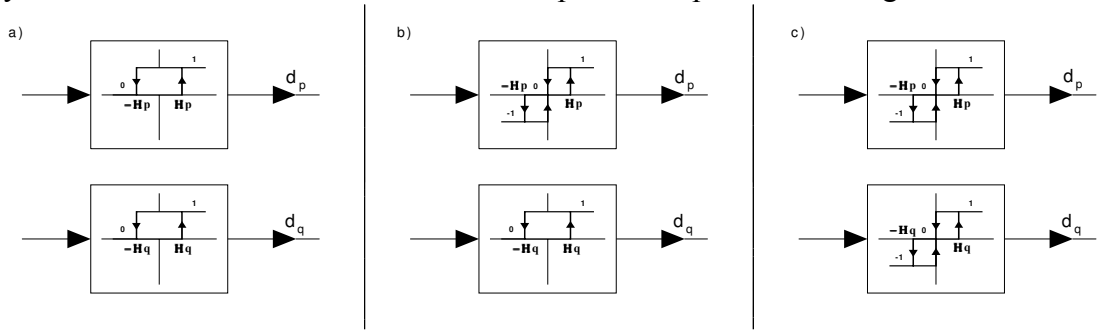


Fig. 3.12 Hysteresis controllers: a) two level; b) mixed two and three level; c) three levels.

The two level hysteresis controllers for instantaneous reactive power can be described as

if $\Delta q > H_q$ then $d_q = 1$
if $-H_q \leq \Delta q \leq H_q$ and $d\Delta q/dt > 0$ then $d_q = 0$
if $-H_q \leq \Delta q \leq H_q$ and $d\Delta q/dt < 0$ then $d_q = 1$
if $\Delta q < -H_q$ then $d_q = 0$.

The three level hysteresis controllers for the instantaneous active power can be described as a sum of two level hysteresis

if $\Delta p > H_p$ then $d_p = 1$
if $0 \leq \Delta p \leq H_p$ and $d\Delta p/dt > 0$ then $d_p = 0$
if $0 \leq \Delta p \leq H_p$ and $d\Delta p/dt < 0$ then $d_p = 1$
if $-H_q \leq \Delta p \leq 0$ and $d\Delta p/dt > 0$ then $d_p = -1$
if $-H_q \leq \Delta p \leq 0$ and $d\Delta p/dt < 0$ then $d_p = 0$
if $\Delta p < -H_p$ then $d_p = -1$.

Dynamic performance

Combinations of each converter voltage space vector used for instantaneous active and reactive power variation are summarized in Table 3.3. Situation is presented for vector located in the *k-th* sector ($k = 1, 2, 3, 4, 5, 6$) of the α, β plane as shown in Fig. 3.13 [24]. In the table, a single arrow means a small variation, whereas two arrows mean a large variation. As it appears from the table, an increment of reactive power (↑) is obtained by applying the space vector U_K, U_{K+1} and U_{K+2}. Conversely, a decrement of reactive power (↓) is obtained by applying vector U_{K-2}, U_{K-1}, or U_{K+3}. Active power increase when U_{K+2}, U_{K+3}, U_{K+1}, U_{K-2} or U_0, U_7 are applied and active power decrease when U_K, U_{K-1} are applied.

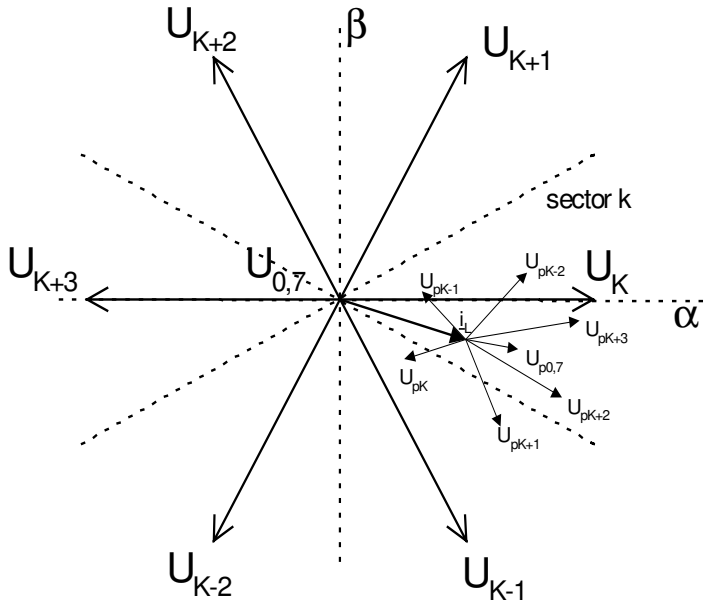


Fig. 3.13 Variation of converter voltage space vector

Table 3.3 Instantaneous active and reactive variations due to the applied voltage vectors

	$\mathbf{U_{K-2}}$	$\mathbf{U_{K-1}}$	$\mathbf{U_K}$	$\mathbf{U_{K+1}}$	$\mathbf{U_{K+2}}$	$\mathbf{U_{K+3}}$	$\mathbf{U_0U_7}$
q	↓↓	↓	↑↑	↑	↑	↓	↑↓
p	↑	↓	↓	↑	↑↑	↑↑	↑

General features of switching table and hysteresis controllers

- The switching frequency depends on the hysteresis wide of active and reactive power comparators.
- By using three-level comparators, the zero vectors are naturally and systematically selected. Thus, the number of switching is considerably smaller than in the system with two-level hysteresis comparators.
- Zero vectors decrease switching frequency but it provides short-circuit for the line to line voltage.
- Zero vectors *U_0(000)* and *U_7(111)* should be appropriate chosen.
- For *DPC* only the neighbour vectors should be selected what decrease dynamics but provide low current and power ripples (low *THD*).
- Switching table with *PLL* (Phase-Locked Loop) sector detection guarantees a very stable and free of disturbances operation, even under distorted and unbalanced line voltages.
- 12 sectors provide more accurate voltage vector selection.

3.6 SIMULATION AND EXPERIMENTAL RESULTS

To study the operation of the *VF-DPC* system under different line conditions and to carry out a comparative investigation, the PWM rectifier with the whole control scheme has been simulated using the *SABER* software [A.4]. The main electrical parameters of the power circuit and control data are given in the Table A.4.1.
The simulation study has been performed with two main objectives:

- explaining and presenting the steady state operation of the proposed by Author *VF-DPC* with a purely sinusoidal and distorted unbalanced supply line voltage, as well as performance comparison with the conventional scheme where the instantaneous power is estimated based on calculated voltage (not virtual flux) signals [21];
- presenting the dynamic performance of power control.

The simulated waveforms for the proposed by Author *VF-DPC* and for the *DPC* reported in [21] are shown in Fig. 3.14. These results were obtained for purely sinusoidal supply line voltage. Similarly Fig. 3.15 shows on oscilogram for distorted (5% of 5-th harmonic) and unbalanced (4,5%) line voltages (see A.1). Fig. 3.15 and Fig. 3.16 show that *VF-DPC* provides sinusoidal and balanced line currents even at distorted and unbalanced supply voltage. This is thanks to fact that voltage was replaced by virtual flux.
The dynamic behaviour under a step change of the load is presented in Fig. 3.21. Note, that in spite of the lower sampling frequency (50 kHz), the *VF* based power estimator gives much less noisy instantaneous active and reactive power signals (Fig. 3.21b) in comparison to the conventional *DPC* system with 80 kHz sampling frequency (Fig. 3.21a). This is thanks to the natural low-pass filter behaviour of the integrators used in (2.42) (because *k-th* harmonics are reduced by a factor *1/k* and the ripple caused by high frequency power transistor switching is effectively damped). Consequently, the derivation of the line current, which is necessary in conventional *DPC* for sensorless voltage estimation, is in the *VF-DPC* eliminated. However, the dynamic behaviour of both control systems, are identical (see Fig. 3.21). The excellent dynamic properties of the *VF-DPC* system at distorted and unbalanced supply voltage are shown in Fig. 3.22.

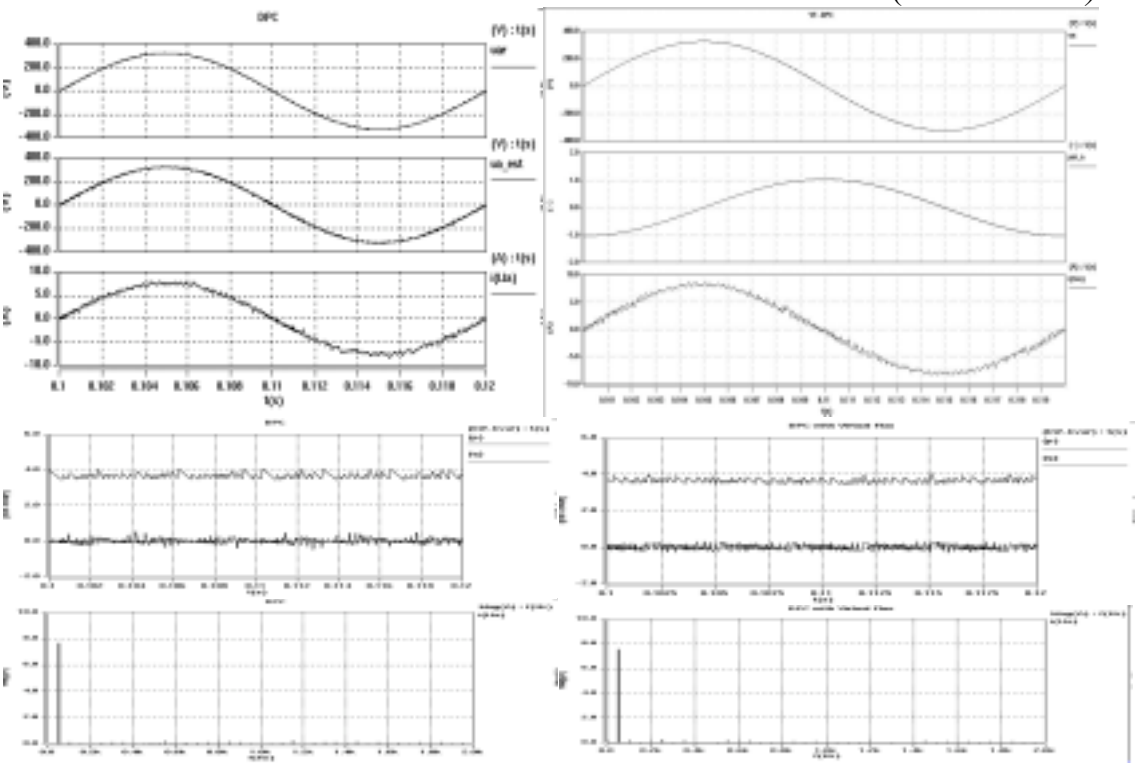
Experimental results were realized on laboratory setup presented in A.6. The main electrical parameters of the power circuit and control data are given in the Table A.6.2. The experimental results are measured for significantly distorted line voltage what is presented in Fig. 3.17. Steady state operation for *DPC* and *VF-DPC* are shown in Fig. 3.18 - 3.20. The shape of the current for conventional DPC is strongly distorted because two undesirable conditions are applied:

- sampling time was 20μs (should be about 10μs [21]),
- the line voltage was not purely sinusoidal.

VF-DPC in comparison with the conventional solution at the same condition provides sinusoidal current (Fig. 3.19-3.20) with low total harmonic distortion. The dynamic behaviour under a step change of the load for *VF-DPC* are shown in Fig. 3.23-3.24.

STEADY STATE BEHAVIOUR

- *RESULTS UNDER PURELY SINUSOIDAL LINE VOLTAGE* (*SIMULATION)*



(a) (b)

Fig. 3.14 Simulated basic signal waveforms and line current harmonic spectrum under purely sinusoidal line voltage: a) conventional *DPC* presented in [21], b) proposed *VF-DPC*,. From the top: line voltage, estimated line voltage (left) and estimated virtual flux (right), line currents, instantaneous active and reactive power, harmonic spectrum of the line current. *DPC THD* = 5.6%, *VF-DPC THD* = 5.2%.

- *RESULTS UNDER NON SINUSOIDAL LINE VOLTAGE* (SIMULATION)

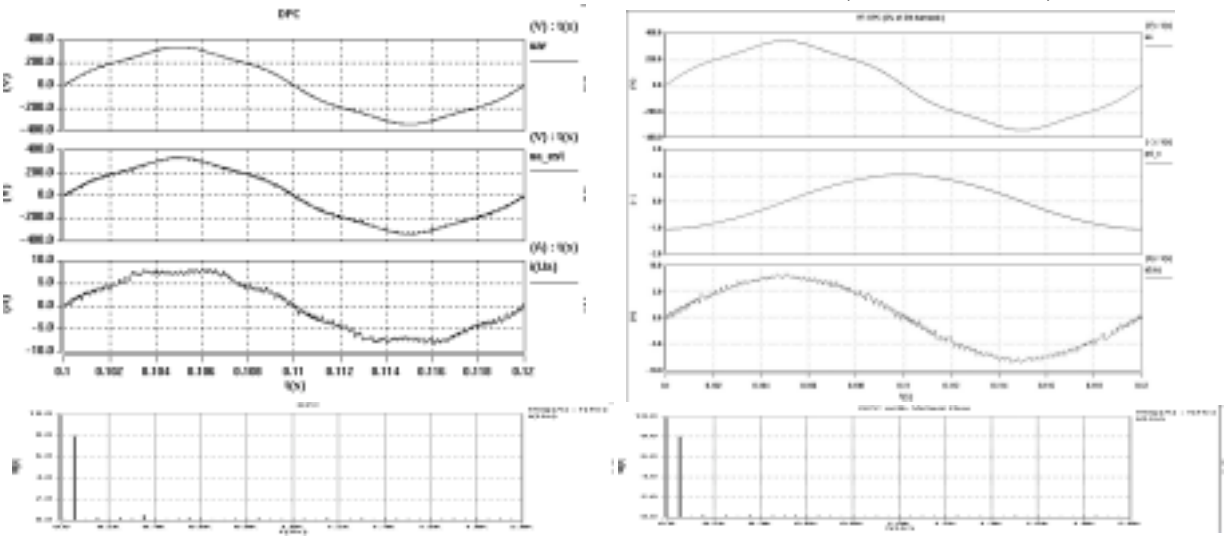


Fig. 3.15. Simulated waveforms and line current harmonic spectrum under pre-distorted (5% of 5th harmonic) and unbalanced (4.5%) line voltage for conventional *DPC* and *VF-DPC*. From the top: line voltage, estimated line voltage(left) and virtual flux (right), line currents, harmonic spectrum of the line current.

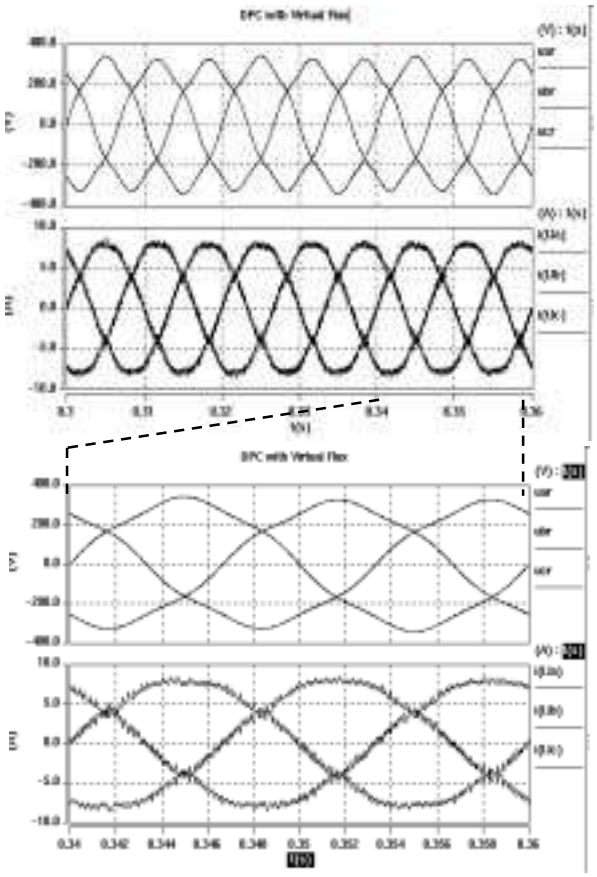


Fig. 3.16. Simulated basic signal waveforms in the *VF-DPC* under pre-distorted (5% of 5th harmonic) and unbalanced (4.5%) line voltage.
From the top: line voltages, line currents. *THD* = 5.6%

➢ *RESULTS UNDER NON SINUSOIDAL LINE VOLTAGE* (EXPERIMENT)

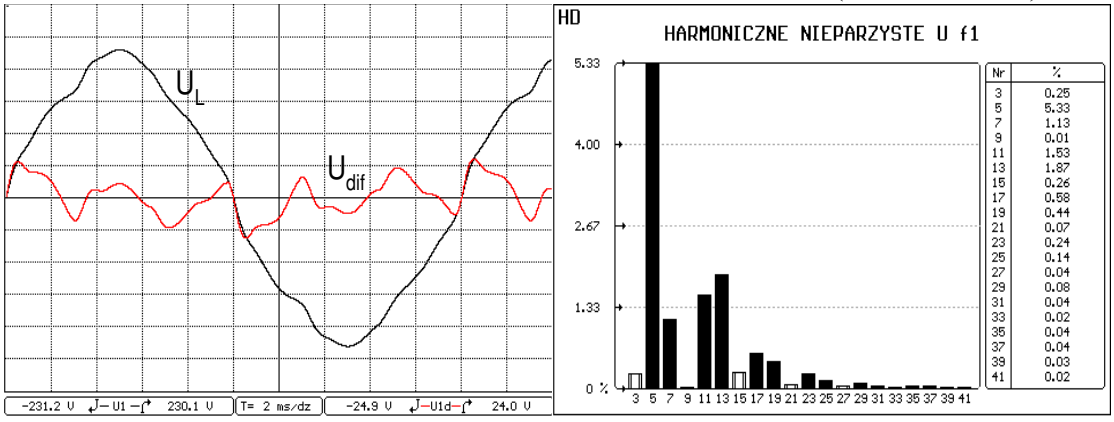


Fig.3.17. Line voltage with harmonic spectrum
(u_L – line voltage, u_{dif} -distortion from purely sinusoidal supply line voltage).

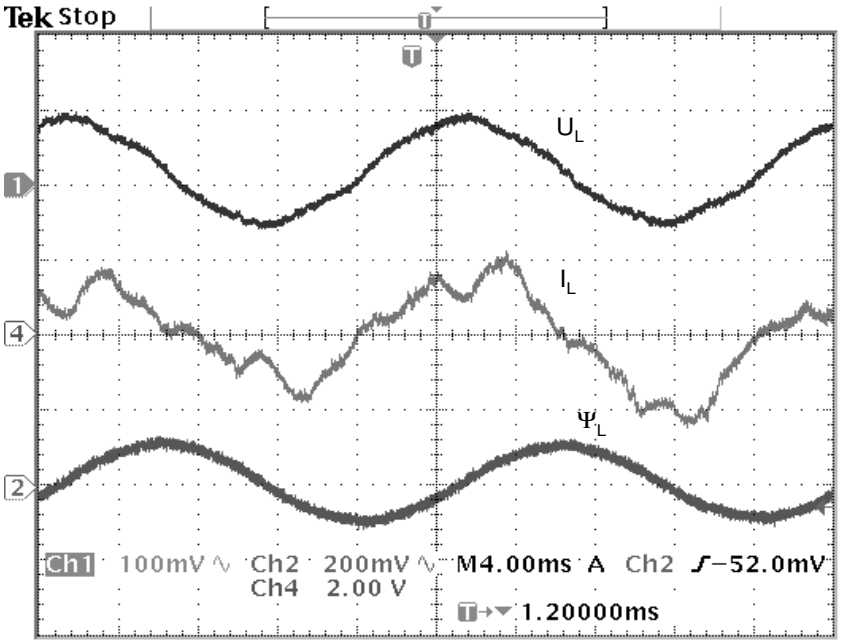


Fig.3.18. Experimental waveforms with distorted line voltage for conventional *DPC*. From the top: line voltage, line currents (5A/div) and estimated virtual flux.

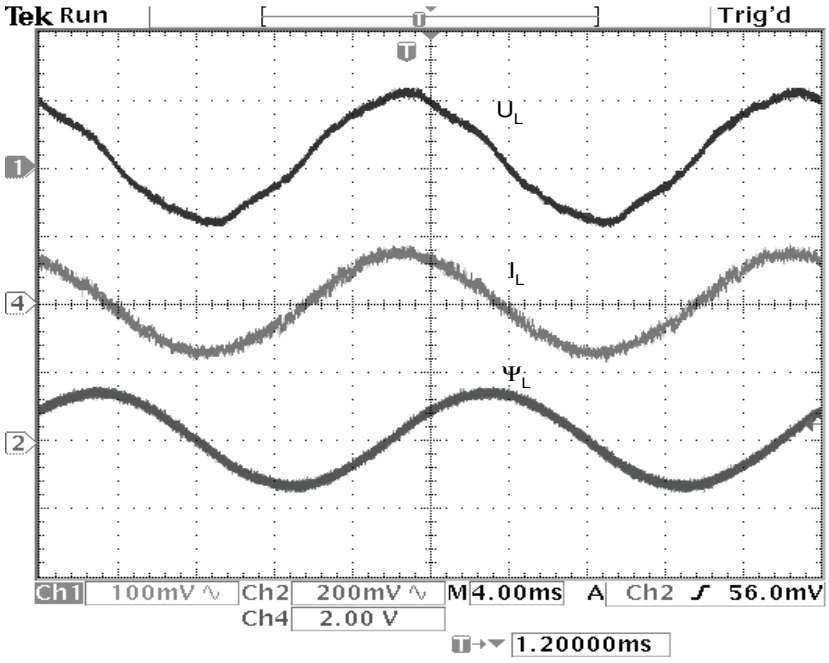


Fig.3.19. Experimental waveforms with distorted line voltage for *VF- DPC*. From the top: line voltage, line currents (5A/div) and estimated virtual flux

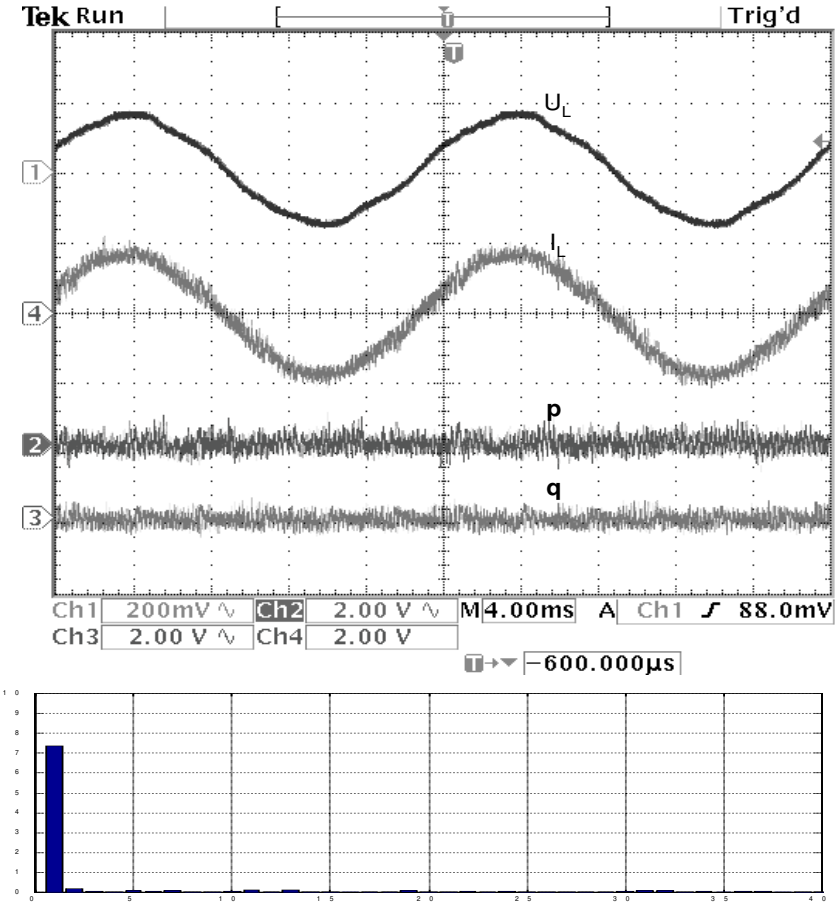


Fig.3.20. Experimental waveforms with distorted line voltage for *VF-DPC*. From the top: line voltage, line currents (5A/div), instantaneous active (2 kW/div) and reactive power (2 kVAr/div), harmonic spectrum of line current (*THD* = 5,6%) [17].

DYNAMIC BEHAVIOUR

- RESULTS UNDER PURELY SINUSOIDAL LINE VOLTAGE *(SIMULATION)*

(a) (b)

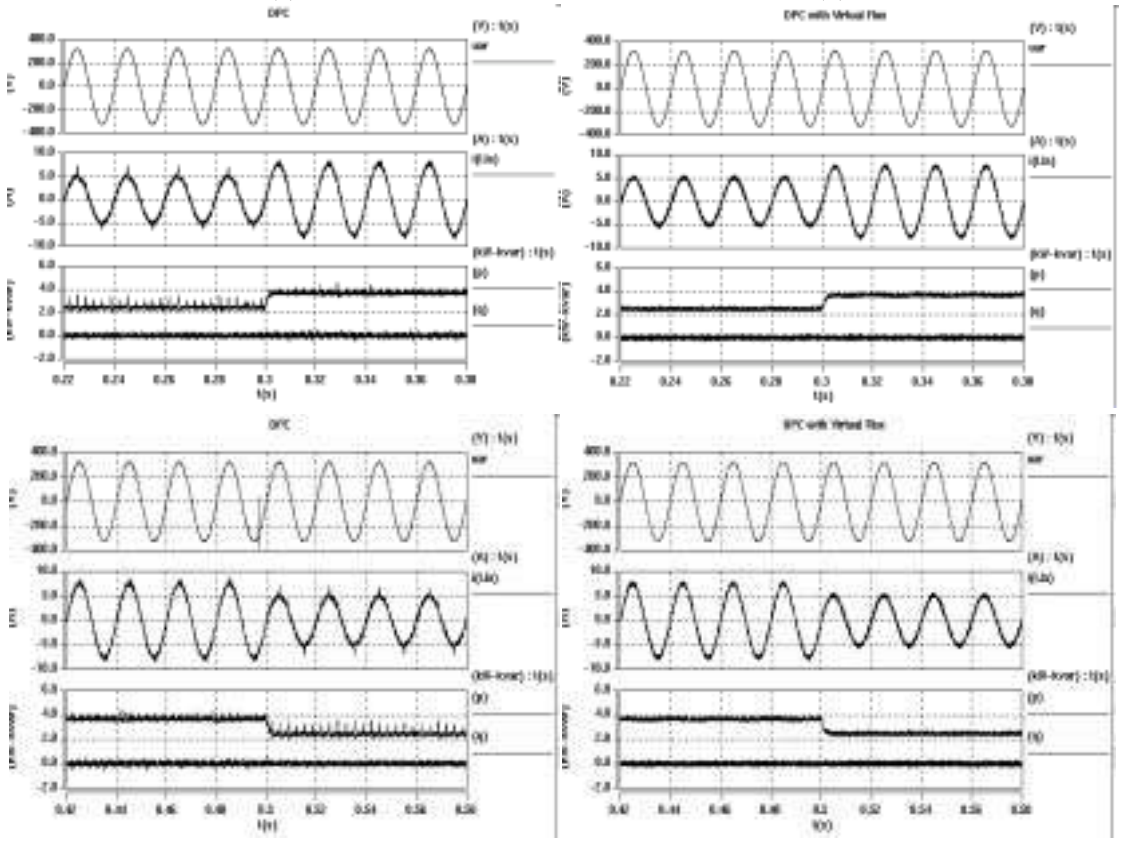


Fig. 3.21. Transient of the step change of the load:
(a) conventional *DPC* presented in [21], (b) proposed *VF-DPC*,.
From the top: line voltage, line currents, instantaneous active and reactive power.

- *RESULTS UNDER NON SINUSOIDAL LINE VOLTAGE (SIMULATIONS)*

(a) (b)

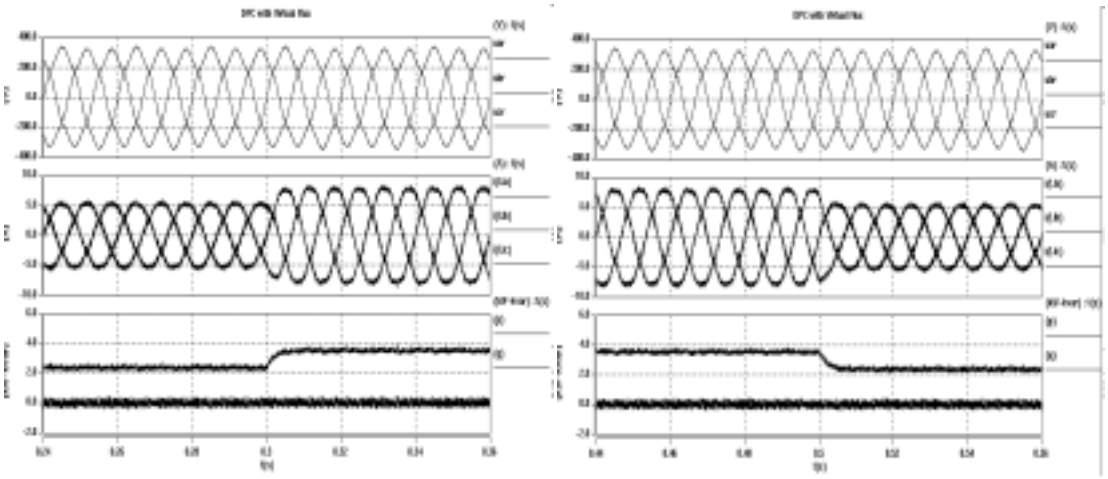


Fig. 3.22. Transient to the step change of the load in the *VF-DPC*:
(a) load increasing (b) load decreasing.
From the top: line voltages, line currents, instantaneous active and reactive power.

➢ *RESULTS UNDER NON SINUSOIDAL LINE VOLTAGE (EXPERIMENT)*

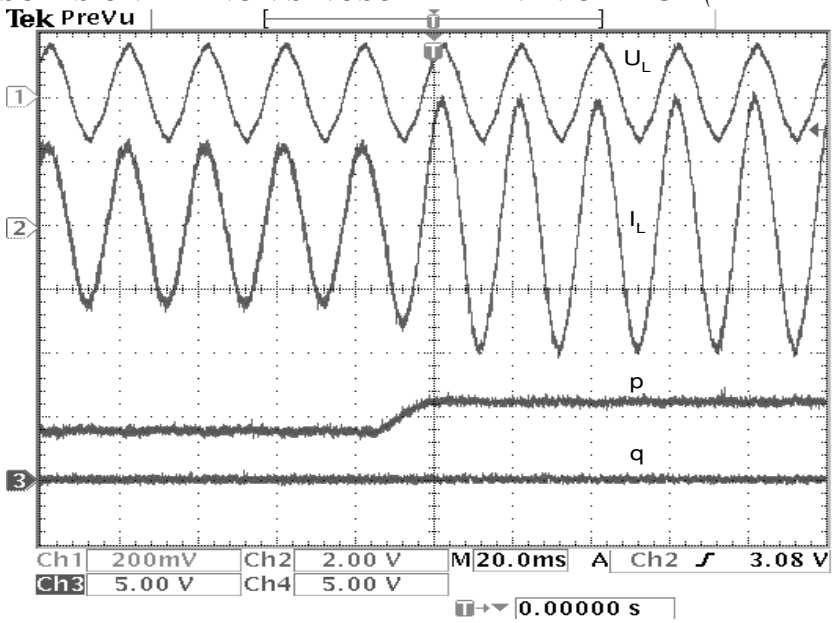


Fig. 3.23. Transient of the step change of the load in the improved *VF-DPC*: load increasing. From the top: line voltages, line currents (5A/div), instantaneous active (2 kW/div) and reactive power (2 kVAr/div).

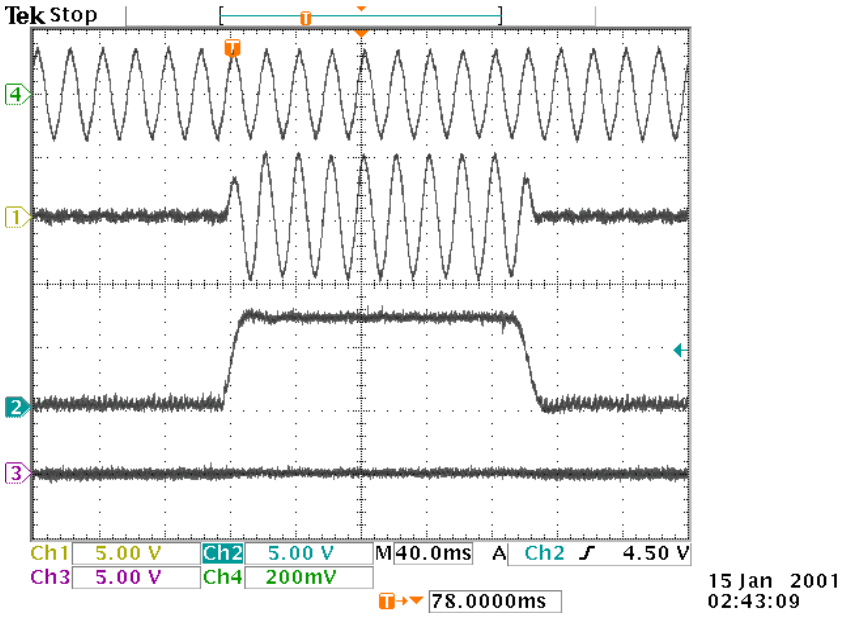


Fig. 3.24 Transient of the step change of the load in the improved *VF-DPC*: start-up of converter. From the top: line voltages, line currents (5A/div), instantaneous active (2 kW/div) and reactive power (2 kVAr/div).

3.8 SUMMARY

The presented *DPC* system constitutes a viable alternative to the *VOC* system [see Chapter 4] of PWM line rectifiers. However, conventional solution shown by [21] possess several disadvantages:

- the estimated values are changed every time according to the switching state of the converter, therefore, it is important to have high sampling frequency. (good performance is obtained at 80kHz sampling frequency, it means that result precisely depends on sampling time),
- the switching frequency is not constant, therefore, a high value of inductance is needed (about 10%). (this is an important point for the line voltage estimation because a smooth shape of current is needed),
- the wide range of the variable switching frequency can be problem, when designing the necessary LC input filter,
- calculation of power and voltage should be avoided at the moment of switching because it gives high errors of the estimated values.

Based on duality with a PWM inverter-fed induction motor, a new method of instantaneous active and reactive power calculation has been proposed. This method uses the estimated Virtual Flux (*VF*) vector instead of the line voltage vector. Consequently, voltage sensorless line power estimation is much less noisy thanks to the natural low-pass behaviour of the integrator used in the calculation algorithm. Also, differentiation of the line current is avoided in this scheme. So, the presented *VF-DPC* of PWM rectifier has the following features and advantages:

- no line voltage sensors are required,
- simple and noise robust power estimation algorithm, easy to implement in a *DSP*,
- lower sampling frequency (as conventional *DPC* [21]),
- sinusoidal line currents (low *THD*),
- no separate *PWM* voltage modulation block,
- no current regulation loops,
- coordinate transformation and *PI* controllers are not required,
- high dynamic, decoupled active and reactive power control,
- power and voltage estimation gives possibility to obtain instantaneous variables with all harmonic components, what have influence for improvement of total power factor and efficiency [21].

The typical disadvantages are:

- variable switching frequency,
- fast microprocessor and A/D converters, are required.

As shown in the Chapter 3, thanks to duality phenomena, an experience with the high performance decoupled PWM inverter-fed induction motor control can be used to improve properties of the PWM rectifier control.

4. VOLTAGE AND VIRTUAL FLUX ORIENTED CONTROL (VOC, VFOC)

4.1 INTRODUCTION

Similarly as in *FOC* of an induction motor [4], the Voltage Oriented Control (*VOC*) and Virtual Flux Oriented Control (*VFOC*) for line side PWM rectifier is based on coordinate transformation between stationary α-β and synchronous rotating *d-q* reference system. Both strategies guarantees fast transient response and high static performance via an internal current control loops. Consequently, the final configuration and performance of system largely depends on the quality of applied current control strategy [6]. The easiest solution is hysteresis current control that provides a fast dynamic response, good accuracy, no *DC* offset and high robustness. However the major problem of hysteresis control is that its average switching frequency varies with the load current, which makes the switching pattern uneven and random, thus, resulting in additional stress on switching devices and difficulties of LC input filter design. Therefore, several strategies are reported in literature to improve performance of current control [2], [38-40], [68-69]. Among presented regulators the widely used scheme for high performance current control is the *d-q* synchronous controller, where the currents being regulated are *DC* quantities what eliminates steady state error.

4.2 BLOCK DIAGRAM OF THE VOLTAGE ORIENTED CONTROL (VOC)

The conventional control system uses closed-loop current control in rotating reference frame, the Voltage Oriented Control (*VOC*) scheme is shown in Fig. 4.1.

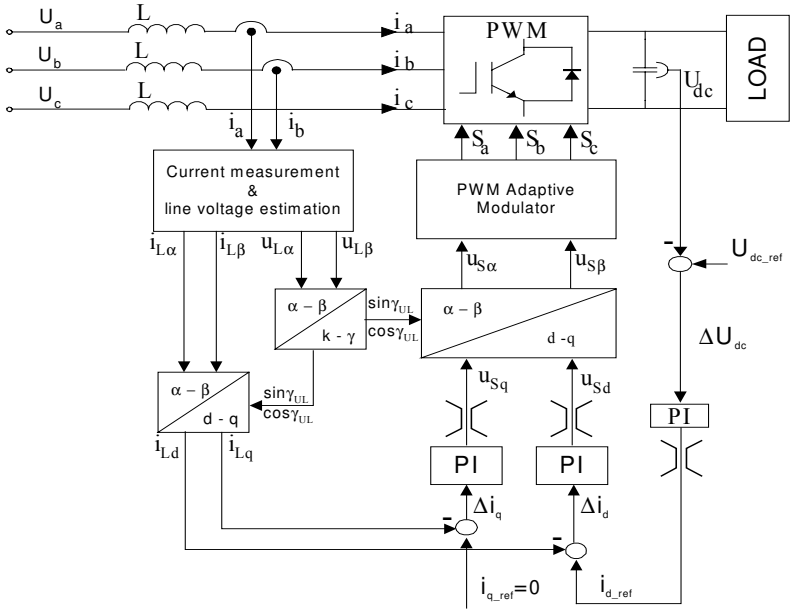


Fig. 4.1 Block scheme of AC voltage sensorless VOC

A characteristic feature for this current controller is processing of signals in two coordinate systems. The first is stationary α-β and the second is synchronously rotating *d-q* coordinate system. Three phase measured values are converted to equivalent two-phase system α-β and then are transformed to rotating coordinate system in a block α-β/*d-q*:

$$\begin{bmatrix} k_d \\ k_q \end{bmatrix} = \begin{bmatrix} \cos\gamma_{UL} & \sin\gamma_{UL} \\ -\sin\gamma_{UL} & \cos\gamma_{UL} \end{bmatrix} \begin{bmatrix} k_\alpha \\ k_\beta \end{bmatrix} \tag{4.1a}$$

Thanks to this type of transformation the control values are DC signals. An inverse transformation *d-q*/α-β is achieved on the output of control system and it gives a result the rectifier reference signals in stationary coordinate:

$$\begin{bmatrix} k_\alpha \\ k_\beta \end{bmatrix} = \begin{bmatrix} \cos\gamma_{UL} & -\sin\gamma_{UL} \\ \sin\gamma_{UL} & \cos\gamma_{UL} \end{bmatrix} \begin{bmatrix} k_d \\ k_q \end{bmatrix} \tag{4.1b}$$

For both coordinate transformation the angle of the voltage vector γ_{UL} is defined as:

$$\sin\gamma_{UL} = u_{L\beta} / \sqrt{(u_{L\alpha})^2 + (u_{L\beta})^2} \tag{4.2a}$$

$$\cos\gamma_{UL} = u_{L\alpha} / \sqrt{(u_{L\alpha})^2 + (u_{L\beta})^2} \,. \tag{4.2b}$$

In voltage oriented *d-q* coordinates, the AC line current vector $\underline{i_L}$ is split into two rectangular components $\underline{i_L} = [i_{Ld}, i_{Lq}]$ (Fig. 4.2). The component i_{Lq} determinates reactive power, whereas i_{Ld} decides about active power flow. Thus the reactive and the active power can be controlled independently. The *UPF* condition is met when the line current vector, $\underline{i_L}$, is aligned with the line voltage vector, $\underline{u_L}$ (Fig. 2.7b) By placing the d-axis of the rotating coordinates on the line voltage vector a simplified dynamic model can be obtained.

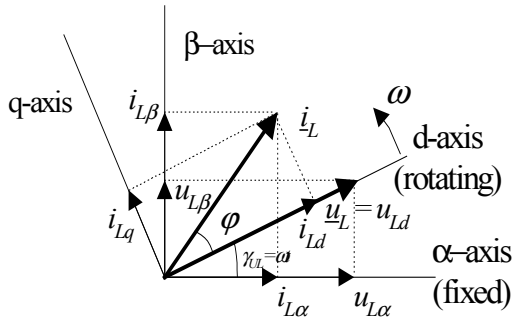


Fig. 4.2: Vector diagram of VOC. Coordinate transformation of line current, line voltage and rectifier input voltage from stationary α–β coordinates to rotating *d-q* coordinates.

The voltage equations in the *d-q* synchronous reference frame in accordance with equations 2.19 are as follows:

$$u_{Ld} = R \cdot i_{Ld} + L\frac{di_{Ld}}{dt} + u_{Sd} - \omega \cdot L \cdot i_{Lq} \tag{4.3}$$

$$u_{Lq} = R \cdot i_{Lq} + L\frac{di_{Lq}}{dt} + u_{Sq} + \omega \cdot L \cdot i_{Ld} \tag{4.4}$$

Regarding to Fig. 4.1, the *q*-axis current is set to zero in all condition for unity power factor control while the reference current i_{Ld} is set by the DC-link voltage controller and

controls the active power flow between the supply and the DC-link. For $R \approx 0$ equations (4.3), (4.4) can be reduced to:

$$u_{Ld} = L\frac{di_{Ld}}{dt} + u_{Sd} - \omega \cdot L \cdot i_{Lq} \tag{4.5}$$

$$0 = L\frac{di_{Lq}}{dt} + u_{Sq} + \omega \cdot L \cdot i_{Ld} \tag{4.6}$$

Assuming that the q-axis current is well regulated to zero, the following equations hold true

$$u_{Ld} = L\frac{di_{Ld}}{dt} + u_{Sd} \tag{4.7}$$

$$0 = u_{Sq} + \omega \cdot L \cdot i_{Ld} \tag{4.8}$$

As current controller, the PI-type can be used. However, the *PI* current controller has no satisfactory tracing performance, especially, for the coupled system described by Eqs. (4.5), (4.6). Therefore for high performance application with accuracy current tracking at dynamic state the decoupled controller diagram for the PWM rectifier should be applied what is shown in Fig. 4.3 [49]:

$$u_{Sd} = \omega L i_{Lq} + u_{Ld} + \Delta u_d \tag{4.9}$$

$$u_{Sq} = -\omega L i_{Ld} + \Delta u_q \tag{4.10}$$

where Δ is the output signals of the current controllers

$$\Delta u_d = k_p(i_d^* - i_d) + k_i\int(i_d^* - i_d)dt \tag{4.11}$$

$$\Delta u_q = k_p(i_q^* - i_q) + k_i\int(i_q^* - i_q)dt \tag{4.12}$$

The output signals from PI controllers after *dq/αβ* transformation (Eq. (4.1b)) are used for switching signals generation by a Space Vector Modulator [see Section 4.4].

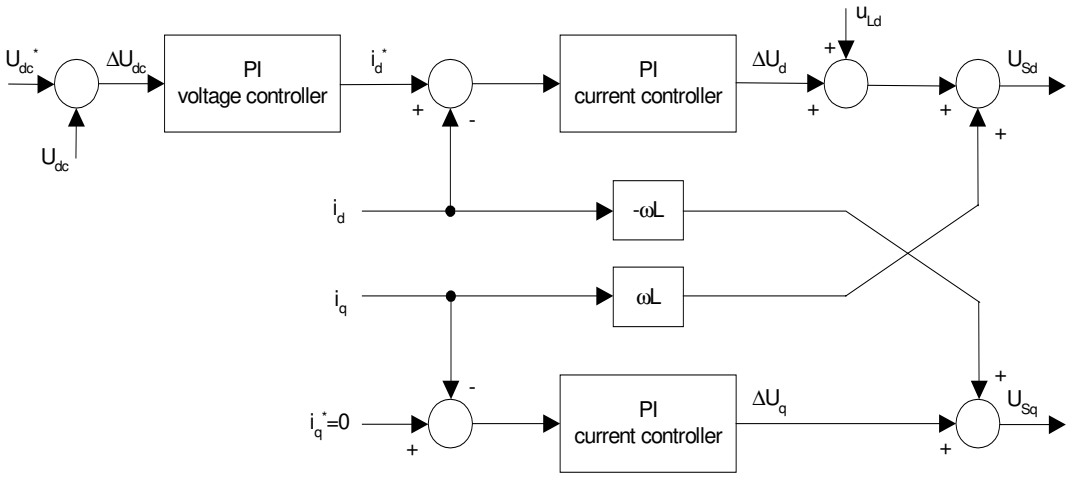


Fig. 4.3 Decoupled current control of PWM rectifier

4.3 BLOCK DIAGRAM OF THE VIRTUAL FLUX ORIENTED CONTROL (VFOC)

The concept of Virtual Flux (*VF*) can also be applied to improve *VOC* scheme, because disturbances superimposed onto the line voltage influence directly the coordinate transformation in control system (4.2). Sometimes this is solved only by phase-locked loops (*PLL's*) only, but the quality of the controlled system depends on how effectively the *PLL's* have been designed [31]. Therefore, it is easier to replace angle of the line voltage vector γ_{UL} by angle of *VF* vector $\gamma_{\Psi L}$, because $\gamma_{\Psi L}$ is less sensitive than γ_{UL} to disturbances in the line voltage, thanks to the natural low-pass behavior of the integrators in (2.42) (because *n*th harmonics are reduced by a factor $1/k$ and the ripple related to the high frequency transistor is strongly damped). For this reason, it is not necessary to implement *PLL's* to achieve robustness in the flux-oriented scheme, since $\underline{\Psi}_L$ rotates much more smoothly than $\underline{u}_L$. The angular displacement of virtual flux vector $\underline{\Psi}_L$ in α-β coordinate is defined as:

$$\sin\gamma_{\Psi L} = \Psi_{L\beta} / \sqrt{\left(\Psi_{L\alpha}\right)^2 + \left(\Psi_{L\beta}\right)^2} \tag{4.13a}$$

$$\cos\gamma_{\Psi L} = \Psi_{L\alpha} / \sqrt{\left(\Psi_{L\alpha}\right)^2 + \left(\Psi_{L\beta}\right)^2} \tag{4.13b}$$

The Virtual Flux Oriented Control (*VFOC*) scheme is shown in Fig. 4.4.

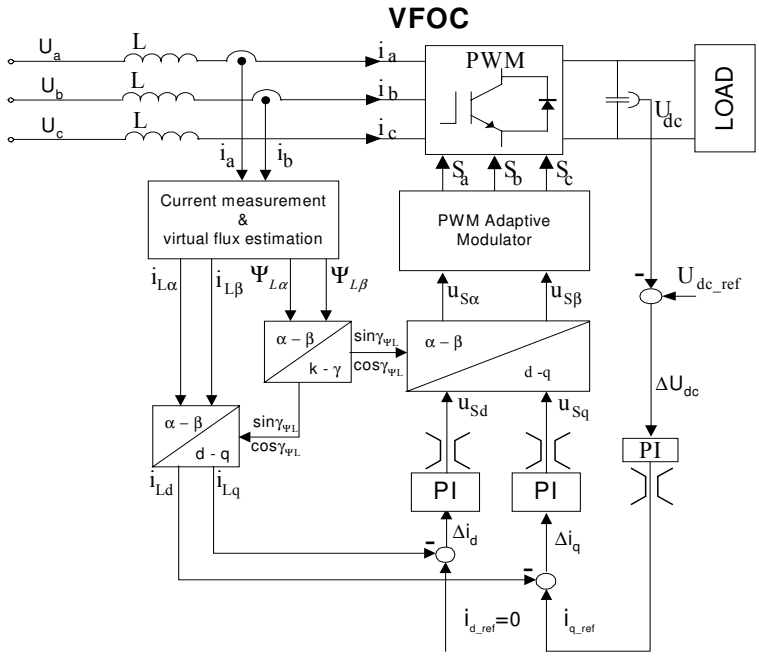


Fig. 4.4 Block scheme of VFOC

The vector of virtual flux lags the voltage vector by 90^o (Fig. 4.5). Therefore, for the UPF condition, the d-component of the current vector, $\underline{i}_L$, should be zero.

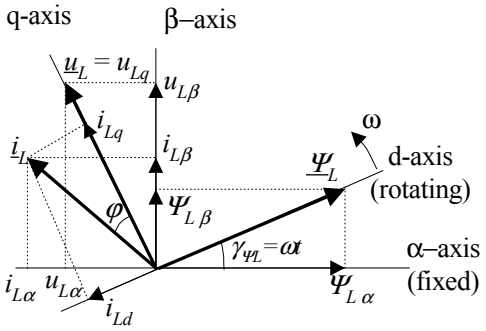


Fig. 4.5: Vector diagram of *VFOC*. Coordinate transformation of line voltage, rectifier input voltage and line current from fixed α–β coordinates to rotating *d-q* coordinates.

In the virtual flux oriented coordinates voltage equations are transformed into

$$u_{Lq} = L\frac{di_{Lq}}{dt} + u_{Sq} + \omega \cdot L \cdot i_{Ld} \tag{4.17}$$

$$0 = L\frac{di_{Ld}}{dt} + u_{Sd} - \omega \cdot L \cdot i_{Lq} \tag{4.18}$$

for $i_{Ld} = 0$ equations (4.17) and (4.18) can be described as:

$$u_{Lq} = L\frac{di_{Lq}}{dt} + u_{Sq} \tag{4.19}$$

$$0 = u_{Sd} - \omega \cdot L \cdot i_{Lq} \tag{4.20}$$

4.4 PULSE WIDTH MODULATION (PWM)

4.4.1 Introduction

Application and power converter topologies are still expanding thanks to improvements in semiconductor technology, which offer higher voltage and current rating as well as better switching characteristics. On the other hand, the main advantages of modern power electronic converters such as: high efficiency, low weight and small dimensions, fast operation and high power densities are being achieved trough the use of the so called *switch mode operation*, in which power semiconductor devices are controlled in *ON/OFF* fashion. This leads to different types of Pulse Width Modulation (*PWM*), which is basic energy processing technique applied in power converter systems. In modern converters, *PWM* is high-speed process ranging – depending on a rated power – from a few kHz (motor control) up to several MHz (resonant converters for power supply). Therefore, an on-line optimisation procedure is hard to be implemented especially, for three or multi-phase converters. Development of *PWM* methods is, however, still in progress [70-101].

Fig.4.7 presents three-phase voltage source PWM converter, which is the most popular power conversion circuit used in industry. This topology can work in two modes:

- **inverter** - when energy, of adjusted amplitude and frequency, is converted from *DC* side to *AC* side. This mode is used in variable speed drives and *AC* power supply including uninterruptible power supply (*UPS*),
- **rectifier** - when energy of mains (50 Hz or 60Hz) is converted from *AC* side to *DC* side. This mode has application in power supply with Unity Power Factor (*UPF*).

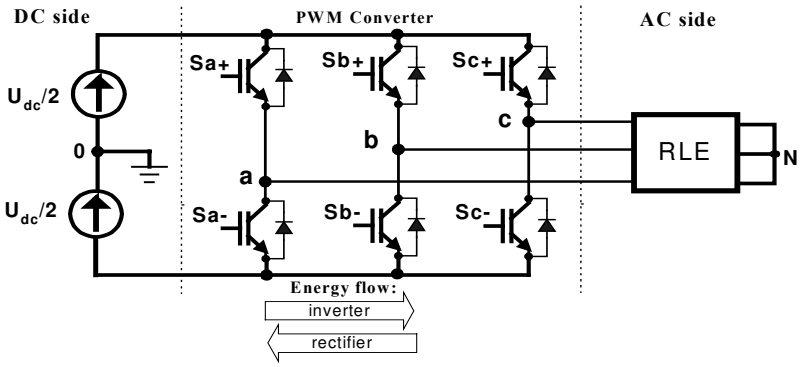


Fig. 4.7. Three-phase voltage source PWM converter

Basic requirements and definitions

Performance significantly depends on control methods and type of modulation. Therefore the PWM converter, should perform some general demands like:

- *wide range of linear operation*, [3, 72, 74, 78, 81, 85, 89],
- *minimal number of (frequency) switching* to keep low switching losses in power components, [5, 72, 74, 80, 87, 93],
- *low content of higher harmonics in voltage and current*, because they produce additional losses and noise in load [5, 77],
- *elimination of low frequency harmonics* (in case of motors it generates torque pulsation)
- *operation in overmodulation region including square wave* [75, 79, 85, 89, 96].

Additionally, investigations are lead with the purpose of:
- *simplification* because modulator is one of the most time-consuming part of control algorithm and reducing of computations intensity at the same performance is the main point for industry (it gives possibility to use simple and inexpensive microprocessors) [76, 95, 101],
- *reduction of common mode voltage* [90],
- *good dynamics* [28, 93],
- *reduction of acoustic noise* (random modulation)[70].

Basic definition and parameters, which characterize *PWM* methods, are summarized in Tab.4.1.

Tab. 4.1. Basic parameters of *PWM*.

lp.	Name of parameter	Symbol	Definition	Remarques
1	Modulation index	M	$M = U_{1m}/U_{1(six\text{-}step)} = U_{1m}/(2/\pi)U_d$	Two definition of modulation index are used. For sinusoidal modulation 0≤M≤0,785 or 0≤m≤1
		m	$m = U_m / U_{m(t)}$	
2	Max. linear range	M_{max}	0 ... 0.907	Depends on shape of modulation signal
		m_{max}	0 ... 1.154	
3	Overmodulation		$M > M_{\max}$ $m > m_{\max}$	Nonlinear range used for increase of output voltage
4	Frequency modulation ratio	m_f	$m_f = f_S / f_1$	For $m_f > 21$ asynchronous modulation is used
5	Switching frequency (number)	f_s (l_s)	$f_s = f_T = 1 / T_s$ T_s – sampling time	Constant
6	Total Harmonic Distortion	THD	THD=100%* I_h / I_{s1}	Used for voltage and current
7	Current distortion factor	d	$I_{h(rms)} / I_{h(six\text{-}step)(rms)}$	Independent of load parameters
8	Polarity consistency rule	PCR		Avoids ± 1 DC voltage transition

4.4.2. Carrier Based PWM

Sinusoidal PWM

Sinusoidal modulation is based on triangular carrier signal. By comparison of common carrier signal with three reference sinusoidal signals U_a^*, U_b^*, U_c^* (moved in phase of $2/3\pi$) the logical signals, which define switching instants of power transistor (Fig. 4.8) are generated. Operation with constant carrier signal concentrate voltage harmonics around switching frequency and multiple of switching frequency. Narrow range of linearity is a limitation for *CB-SPWM* modulator because modulation index reaches $M_{max} = \pi/4 = 0.785$ ($m = 1$) only, e.g. amplitude of reference signal and carrier are equal. Overmodulation region occurs above M_{max} and *PWM* converter, which is treated like a power amplifier, operates at nonlinear part of characteristic (see Fig. 4.21).

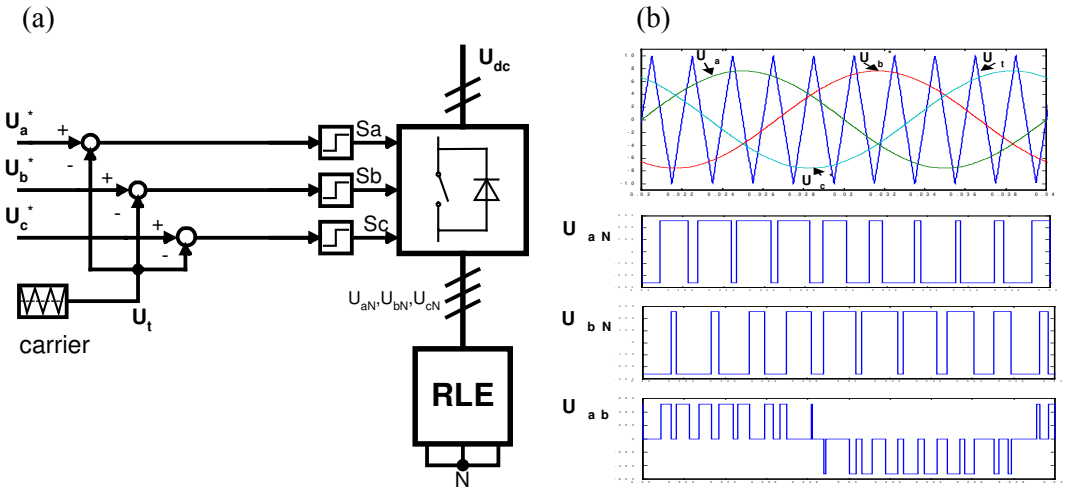


Fig. 4.8. a) Block scheme of carrier based sinusoidal modulation (*CB-SPWM*)
(b) Basic waveforms

CB-PWM with Zero Sequence Signal (ZSS)

If neutral point on AC side of power converter *N* is not connected with *DC* side midpoint *0* (Fig. 4.7), phase currents depend only on the voltage difference between phases. Therefore, it is possible to insert an additional Zero Sequence Signal (*ZSS*) of 3-th harmonic frequency, which does not produce phase voltage distortion U_{aN}, U_{bN}, U_{cN} and without affecting load average currents (Fig. 4.10). However, the current ripple and other modulator parameters (e.g. extending of linear region to $M_{max} = \pi / 2\sqrt{3} = 0.907$, reduction of the average switching frequency, current harmonics) are changed by the *ZSS*. Added *ZSS* occurs between *N* and *0* points and is visible like a U_{N0} voltage and can be observed in U_{a0}, U_{b0}, U_{c0} voltages (Fig. 4.10).

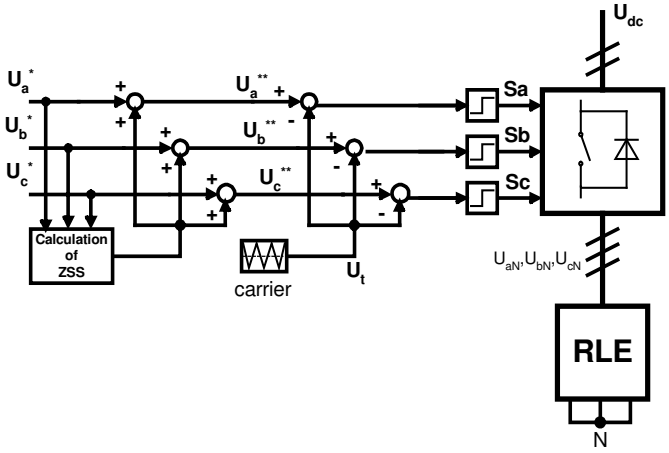


Fig. 4.9. Block scheme of modulator based on additional Zero Sequence Signal *(ZSS)*.

Fig. 4.10 presents different waveforms of additional *ZSS*, corresponding to different *PWM* methods. It can be divided in two groups: *continuous* and *discontinuous* modulation (*DPWM*) [92]. The most known of continuous modulation is method with sinusoidal *ZSS* with 1/4 amplitude, it corresponds to minimum of output current harmonics, and with 1/6 amplitude it corresponds to maximal linear range [86]. Triangular shape of *ZSS* with 1/4 peak corresponds to conventional (analogue) space vector modulation with symmetrical placement of zero vectors in sampling time [83]

(see Section 4.4.3). Discontinuous modulation is formed by unmodulated 60° segments (converter power switches do not switch) shifted from 0 to π/3 (different shift Ψ gives different type of modulation Fig. 4.11). It finally gives lower (average 33%) switching losses. Detailed description of different kind of modulation based on *ZSS* can be found in [80].

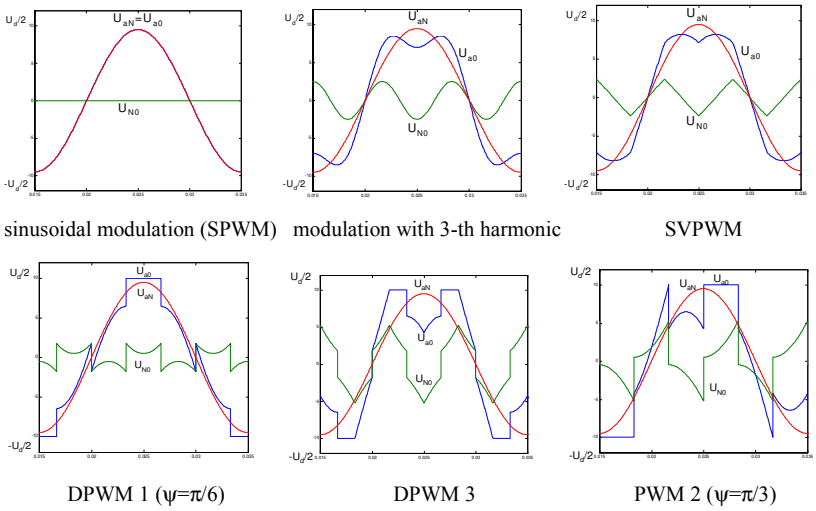


Fig. 4.10. Variants of PWM modulation methods in dependence on shape of ZSS.

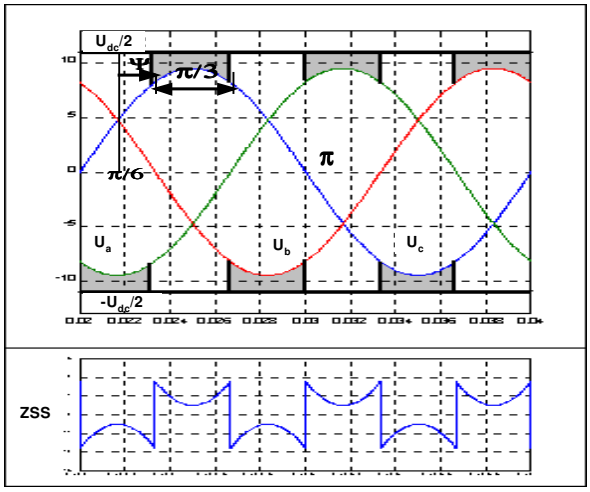


Fig. 4.11. Generation of ZSS for DPWM method.

4.4.3. Space Vector Modulation (SVM)

Basics of SVM

The SVM strategy, based on space vector representation (Fig. 4.12a) becomes very popular due to its simplicity [97]. A three-phase two-level converter provides eight possible switching states, made up of six active and two zero switching states. Active vectors divide plane for six sectors, where a reference vector U^* is obtained by switching on (for proper time) two adjacent vectors. It can be seen that vector U^* (Fig. 4.12a) is possible to implement by the different switch on/off sequence of U_1 and U_2, and that zero vectors decrease modulation index. Allowable length of U^* vector, for each of α angle, is equal $U^*_{\max} = U_{dc}/\sqrt{3}$. Higher values of output voltage (reach six-step mode) up to maximal modulation index ($M = 1$), can be obtained by an additional

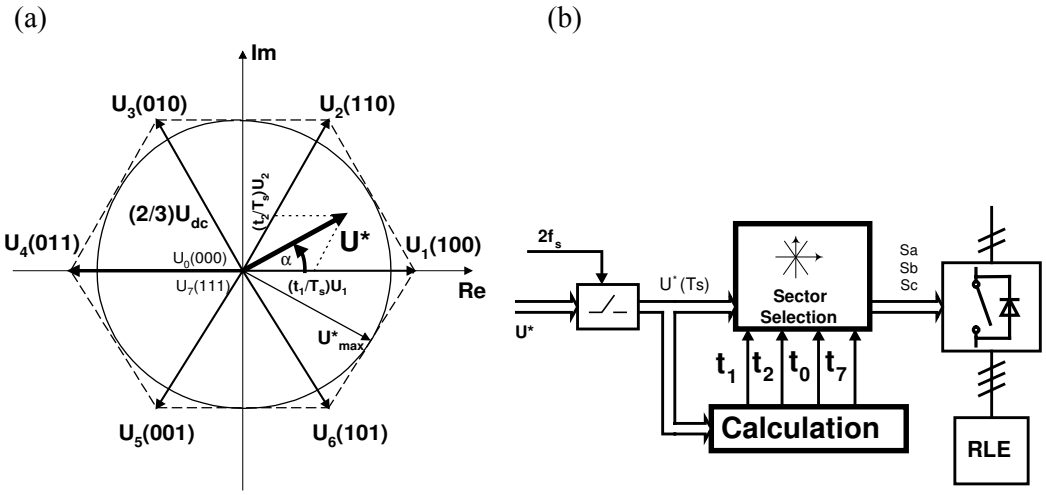


Fig. 4.12. (a) Space vector representation of three-phase converter, (b) Block scheme of SVM

non-linear overmodulation algorithm (see Section 4.4.5).

Contrary to *CB-PWM*, in the *SVM* there is no separate modulators for each phase. Reference vector U^* is sampled with fixed clock frequency $2f_s = 1/T_s$, and next $U^*(T_s)$ is used to solve equations which describe times t_1, t_2, t_0 and t_7 (Fig. 4.12b). Microprocessor implementation is described with the help of simple trigonometrical relationship for first sector (4.21a and 4.21b), and, recalculated for the next sectors (n).

$$t_1 = \frac{2\sqrt{3}}{\pi} M T_s \sin(\pi/3 - \alpha) \tag{4.21a}$$

$$t_2 = \frac{2\sqrt{3}}{\pi} M T_s \sin\alpha \tag{4.21b}$$

After t_1 and t_2 calculation, the residual sampling time is reserved for zero vectors U_0, U_7 with condition $t_1 + t_2 \le T_s$. The equations (4.21a), (4.21b) are identical for all variants of *SVM*. The only difference is in different placement of zero vectors $U_0(000)$ and $U_7(111)$. It gives different equations defining t_0 and t_7 for each of method, but total duration time of zero vectors must fulfil conditions:

$$t_{0,7} = T_s - t_1 - t_2 = t_0 + t_7 \tag{4.22}$$

The neutral voltage between *N* and *0* points is equal: (see Tab. 4.2) [91]

$$U_{N0} = \frac{1}{T_s}\left(-\frac{U_{dc}}{2}t_0 - \frac{U_{dc}}{6}t_1 + \frac{U_{dc}}{6}t_2 + \frac{U_{dc}}{2}t_7\right) = \frac{U_{dc}}{2}\frac{1}{Ts}\left(-t_0 - \frac{t_1}{3} + \frac{t_2}{3} + t_7\right) \tag{4.23}$$

Table 4.2. Voltages between *a, b, c* and *N, 0* for eight converter switching state

	U_{a0}	U_{b0}	U_{c0}	U_{aN}	U_{bN}	U_{cN}	U_{NO}
U_0	$-U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/2$	0	0	0	$-U_{dc}/2$
U_1	$U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/2$	$2U_{dc}/3$	$-U_{dc}/3$	$-U_{dc}/3$	$-U_{dc}/6$
U_2	$U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/3$	$U_{dc}/3$	$-2U_{dc}/3$	$U_{dc}/6$
U_3	$-U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/2$	$-U_{dc}/3$	$2U_{dc}/3$	$-U_{dc}/3$	$-U_{dc}/6$
U_4	$-U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$	$-2U_{dc}/3$	$U_{dc}/3$	$U_{dc}/3$	$U_{dc}/6$
U_5	$-U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/2$	$-U_{dc}/3$	$-U_{dc}/3$	$2U_{dc}/3$	$-U_{dc}/6$
U_6	$U_{dc}/2$	$-U_{dc}/2$	$U_{dc}/2$	$U_{dc}/3$	$-2U_{dc}/3$	$U_{dc}/3$	$U_{dc}/6$
U_7	$U_{dc}/2$	$U_{dc}/2$	$U_{dc}/2$	0	0	0	$U_{dc}/2$

Three-phase SVM with symmetrical placement of zero vectors (SVPWM)

The most popular *SVM* method is modulation with symmetrical zero states (*SVPWM*):

$$t_0 = t_7 = (T_s - t_1 - t_2)/2 \tag{4.24}$$

Figure 4.13a shows gate pulses for (*SVPWM*) and correlation between duty time T_{on}, T_{off} and duration of vectors t_1, t_2, t_0, t_7. For the first sector commutation delay can be computed as:

$$\begin{aligned} T_{aon} &= t_0/2 & T_{aoff} &= t_0/2 + t_1 + t_2 \\ T_{bon} &= t_0/2 + t_1 & T_{boff} &= t_0/2 + t_2 \\ T_{con} &= t_0/2 + t_1 + t_2 & T_{coff} &= t_0/2 \end{aligned} \tag{4.25}$$

For conventional *SVPWM* times t_1, t_2, t_0 are computed for one sector only. Commutation delay for other sectors can be calculated with the help of matrix:

$$\begin{bmatrix} T_{aoff} \\ T_{boff} \\ T_{coff} \end{bmatrix} = \left[\begin{array}{c|c|c|c|c|c} \text{sector1} & \text{sector2} & \text{sector3} & \text{sector4} & \text{sector5} & \text{sector6} \\ \hline 1\ 1\ 1 & 1\ 1\ 1 & 1\ 1\ 1 & 1\ 1\ 1 & 1\ 1\ 1 & 1\ 1\ 1 \\ 1\ 0\ 0 & 1\ 1\ 0 & 0\ 1\ 0 & 0\ 1\ 1 & 0\ 0\ 1 & 1\ 0\ 1 \\ 1\ 1\ 0 & 0\ 1\ 0 & 0\ 1\ 1 & 0\ 0\ 1 & 1\ 0\ 1 & 1\ 0\ 0 \end{array}\right]^T \begin{bmatrix} 0.5T_0 \\ t_1 \\ t_2 \end{bmatrix} \tag{4.26}$$

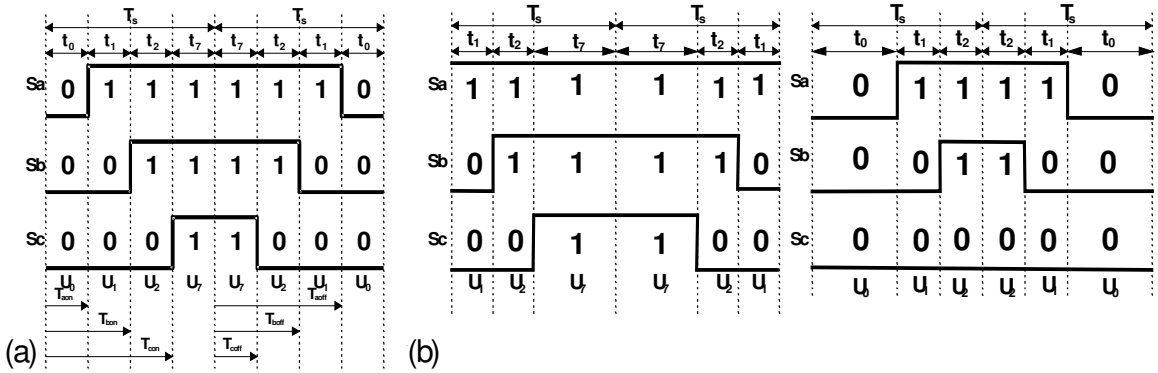


Fig. 4.13. Vectors placement in sampling time:
a) three-phase SVM (*SVPWM, $t_0 = t_7$*) b) two-phase *SVM* (*DPWM, $t_0 = 0$* and *$t_7 = 0$*)

Two-phase SVM

This type of modulation proposed in [98] was developed in [72,74,88] and is called discontinuous pulse width modulation (*DPWM*) for *CB* technique with an additional Zero Sequence Signal (*ZSS*) in [80]. The idea bases on assumption that only two phases are switched (one phase is clamped by 60^0 to lower or upper *DC* bus). It gives only one zero state per sampling time (Fig. 4.13b). Two-phase *SVM* provides 33% reduction of effective switching frequency. However, switching losses also strongly depend on a load power factor angle (see Chapter 4.4.6). It is very important criterion, which allows farther reduction of switching losses up to 50% [80].

Fig. 4.14a shows several different kind of two-phase *SVM*. It can be seen that sectors are adequately moved on 0^0, 30^0, 60^0, 90^0, and denoted as *PWM(0)*, *PWM(1)*, *PWM(2)*, *PWM(3)* respectively ($t_0 = 0$ means that one phase is clamped to one, while $t_7 = 0$ means that phase is clamped to zero). Fig. 4.14b presents phase voltage U_{aN}, pole voltage U_{a0}

and voltage between neutral points U_{N0} for these modulations. Zero states description for *PWM(1)* can be written as:

$$t_0=0 \Rightarrow t_7=T_s-t_1-t_2 \text{ when } 0\le\alpha<\pi/6 \qquad (4.27)$$
$$t_7=0 \Rightarrow t_0=T_s-t_1-t_2 \text{ when } \pi/6\le\alpha<\pi/3$$

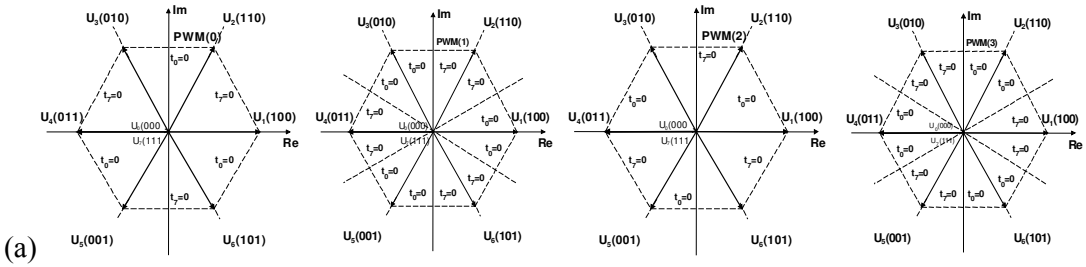


Fig. 4.14 a) Placement of zero vectors in two-phase *SVM*. Succession: *PWM(0)* = 0^0, *PWM(1)* = 30^0, *PWM(2)* = 60^0 and *PWM(3)* = 90^0 b) Phase voltage U_{aN}, pole voltage U_{a0} and voltage between neutral points U_{N0} for each of modulation

Variants of Space Vector Modulation

From equations (4.21)-(4.23) and knowledge of U_{N0} (Fig. 4.14b), it is possible to calculate duration of zero vectors t_0, t_7. An evaluation and properties of different modulation method shows Table 4.3.

Table 4.3. Variants of Space Vector Modulation

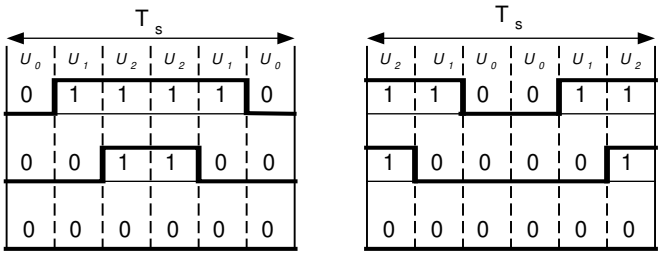
Vector modulation methods	**Calculation of t_0 and t_7**	***Remarques***
Vector modulation with $U_{N0} = 0$	$t_0 = \frac{T_s}{2}(1-\frac{4}{\pi}M\cos\alpha)$ $t_7 = T_s-t_0-t_1-t_2$	• Equivalent of classical *CB-SPWM* (no difference between U_{aN} and U_{b0} voltages) • Linear region $M_{max} = 0.785$
Vector modulation with 3-th harmonic	$t_0 = \frac{T_s}{2}(1-\frac{4}{\pi}M(\cos\alpha-\frac{1}{6}\cos 3\alpha))$ $t_7 = T_s-t_0-t_1-t_2$	• Low current distortions • More complicated calculation of zero vectors • Extended linear region: $M = 0.907$
Three-phase SVM with symmetrical zero states (*SVPWM*)	$t_0 = t_7 = (T_s-t_1-t_2)/2$	• Most often used in microprocessor technique for the sake of simple zero vector calculation (symmetrical in sampling time $2T_s$) • Current harmonic content almost identical like in previous method
Two-phase *SVM*	$t_0 = 0 \Rightarrow t_7 = T_s-t_1-t_2$ when $0\le\alpha<\pi/6$ $t_7 = 0 \Rightarrow t_0 = T_s-t_1-t_2$ when $\pi/6\le\alpha<\pi/3$ (for PWM(1))	• Equivalent of *DPWM* methods in *CB-PWM* technique • 33% switching frequency and switching losses reduction • Higher current harmonic content at low modulation index • Only one zero state per sampling time, simple calculation (Fig. 4.14)

The space vector modulation techniques with one zero state in sampling time may be additionally changed for the sake of different harmonic content what is presented in Tab.4.4 and Fig.4.15 [73].

Tab. 4.4 Different zero vector placement in *PWM(0)*

sector	PWM(0)	Different PWM(0)
1	U_0-U_1-U_2-U_2-U_1-U_0	U_2-U_1-U_0-U_0-U_1-U_2
2	U_3-U_2-U_7-U_7-U_2-U_3	U_3-U_2-U_7-U_7-U_2-U_3
3	U_0-U_3-U_4-U_4-U_3-U_0	U_4-U_3-U_0-U_0-U_3-U_4
4	U_5-U_4-U_7-U_7-U_4-U_5	U_5-U_4-U_7-U_7-U_4-U_5
5	U_0-U_5-U_6-U_6-U_5-U_0	U_6-U_5-U_0-U_0-U_5-U_6
6	U_1-U_6-U_7-U_7-U_6-U_1	U_1-U_6-U_7-U_7-U_6-U_1

a)



b)

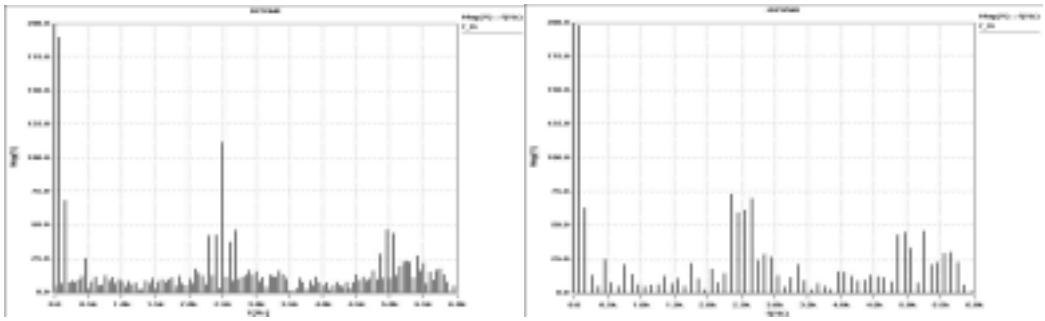


Fig. 4.15 Different *PWM(0)* methods presented above
a) vectors placement b) voltage harmonic content.

4.4.4 Carrier Based PWM Versus Space Vector PWM

Comparison of *CB-PWM* methods with additional *ZSS* to *SVM* is shown on Fig. 4.16. Upper part shows pulse generation through comparison of reference signal U_a^{**}, U_b^{**}, U_c^{**} with triangular carrier signal. Lower part of figure shows gate pulses generation in SVM (obtained by calculation of duration time of active vectors U_1, U_2 and zero vectors U_0, U_7). It is visible that both methods generate identical gate pulses. Also it can be observed from Fig. 4.14 and Fig. 4.16 that the degree of freedom represented in selection of *ZSS* waveform in *CB-PWM*, corresponds to different placement of zero vectors $U_0(000)$ and $U_7(111)$ in sampling time $T_s = 1/2f_s$ of the *SVM*. Therefore, there is no exist difference between *CB-PWM* and *SVM (CB-DPWM1 = PWM(1)-SVM)*. The difference is only in the treatment of the three-phase quantities: CB-PWM operates in terms of three natural components, whereas *SVM* uses artificial (mathematically transformed) vector representation.

(a) (b)

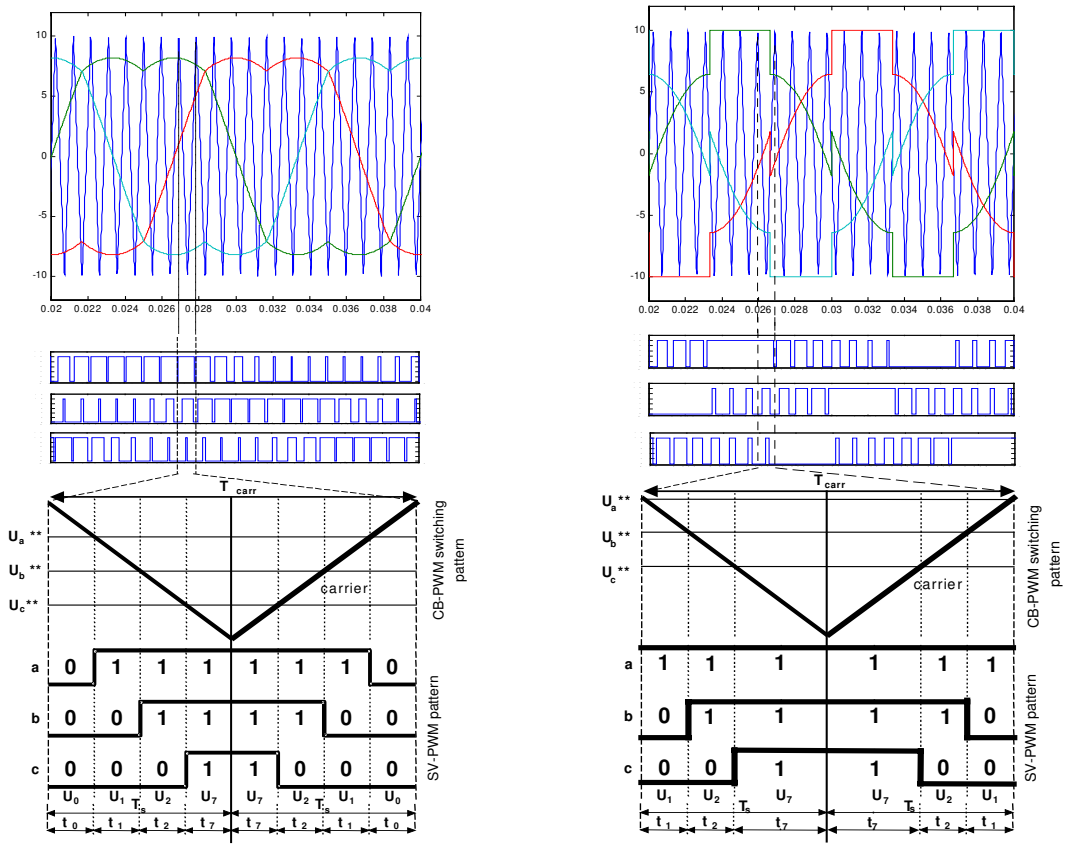


Fig. 4.16. Comparison of *CB-PWM* with *SVM* a) *SVPWM* b) *DPWM*
From the top: *CB-PWM* with pulses, short segment of reference signal at high carrier frequency (reference signals are straight lines), formation of pulses in *SVM*.

4.4.5 Overmodulation

Modulation is a basic techniques in power electronics, therefore for full description of this topic is necessary to presents also overmodulation. This part of modulation is not so important for PWM rectifier in the sake of higher harmonic contents in current but it is possible to find some application with similar mode [119].

Many approaches have been reported in the literature to increase the range of the PWM voltage source inverter [75,79,85,89]. Some of them are proposed as extensions of the Sinusoidal PWM (*SPWM*), and others as extensions of the Space Vector PWM (*SVPWM*). In *CB-PWM* by increasing the reference voltage beyond the amplitude of the triangular carrier signal, some switching cycles are skipped and the voltage of each phase remains clamped to one of the dc bus. This range shows a high non-linearity between reference and output voltage amplitude and requires infinite amplitude of reference in order to reach a six-step output voltage.

In *SVM* allowable length of reference vector U^* which provide linear modulation is equal $U^*_{\max} = U_{dc} / \sqrt{3}$ (circle inscribed in hexagon $M = 0.906$) (Fig. 4.17). To obtain higher values of output voltage (reach six-step mode) up to maximal modulation index $M = 1$, an additional non-linear overmodulation algorithm has to be apply. This is because minimal pulse width becomes shorter than critical (mainly dependent on power switches characteristic – usually few μs) or even negative. Zero vectors are never used in this type of modulation.

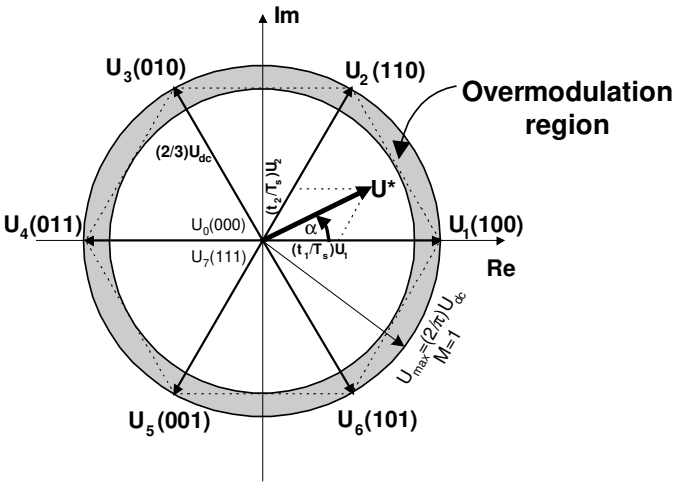


Fig. 4.17 Overmodulation region in space vector representation

Algorithm Based on Two Modes of Operation

Two overmodulation regions are considered (Fig. 4.18). In region I the magnitude of reference voltage is modified in order to keep space vector within the hexagon. It defines the maximum amplitude that can be reached for each angle. This mode extends the range of the modulation index up to 0.95. Mode II starts from $M = 0.95$ and reach six step mode $M = 1$. Mode II defines both the magnitude and the angle of the reference voltage. To implement both modes a lookup table or neural network [96] based approach can be applied.

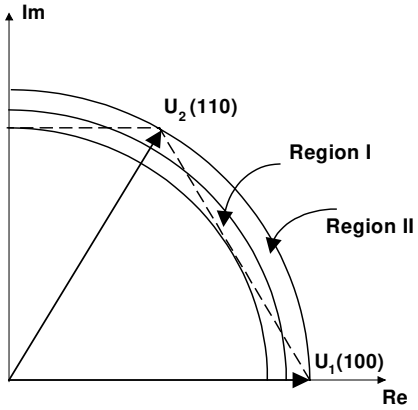


Fig. 4.18 Subdivision of the overmodulation region

Overmodulation mode I: distorted continuous reference signal

In this range, the magnitude of the reference vector is changed while the angle is transmitted without any changes ($\alpha_p = \alpha$). However, when the original reference trajectory passes outside the hexagon, the time average equation gives an unrealistic on duration for the zero vectors. Therefore, to compensate reduced fundamental voltage, i.e. to track with the reference voltage $\boldsymbol{U}^*$, a modified reference voltage trajectory $\boldsymbol{U}$ is selected (Fig. 4.19a). The reduced fundamental components in region where reference trajectory surpass hexagon is compensated by a higher value in corner (equal areas in one sector - see Fig. 4.19a) [85].

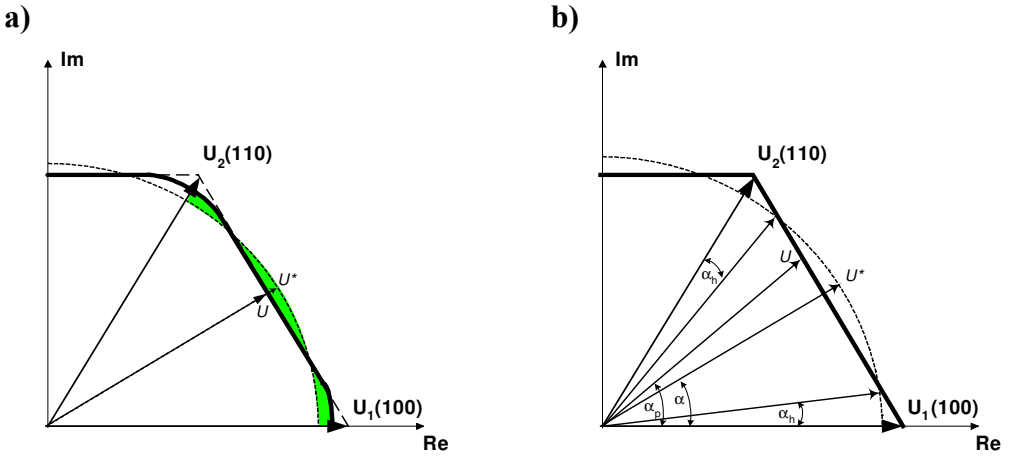


Fig. 4.19 Overmodulation: (a) mode I ($0.907 < M < 0.952$), (b) mode II ($0.952 < M < 1$)
U^* - reference trajectory (dashed line), U – modified reference trajectory (solid line)

The on time durations for region where modified reference trajectory is moved along hexagon are calculated as:

$$t_1 = T_S \frac{\sqrt{3}\cos\alpha - \sin\alpha}{\sqrt{3}\cos\alpha + \sin\alpha} \tag{4.28 a}$$

$$t_2 = T_S - t_1 \tag{4.28 b}$$

$$t_0 = 0 \tag{4.28 c}$$

Overmodulation mode II: distorted discontinuous reference signal.
The operation in this region is illustrated in Fig. 4.19b. The trajectory changes gradually from a continuous hexagon to the six-step operation. To achieve control in overmodulation mode II, both the reference magnitude and reference angle (from α to α_p) are changed:

$$\alpha_p = \begin{cases} 0 & 0 \le \alpha \le \alpha_h \\ \dfrac{\alpha - \alpha_h}{\pi/6 - \alpha_h}\dfrac{\pi}{6} & \alpha_h \le \alpha \le \pi/3 - \alpha_h \\ \pi/3 & \pi/3 - \alpha_h \le \alpha \le \pi/3 \end{cases} \tag{4.29}$$

The modified vector is held at a vertex of the hexagon for holding angle α_h over particular time and then partly tracking the hexagon sides in every sector for the rest of the switching period. The holding angle α_h controls the time interval when active switching state remains at the vertices, which uniquely controls the fundamental voltage. It is a nonlinear function of the modulation index, which can be piecewise linearized as [89]:

$$\begin{aligned} \alpha_h &= 6.4 \cdot M - 6.09 && (0.95 \le \mathrm{M} \le 0.98) \\ \alpha_h &= 11.75 \cdot M - 11.34 && (0.98 \le \mathrm{M} \le 0.9975) \\ \alpha_h &= 48.96 \cdot M - 48.43 && (0.9975 \le \mathrm{M} \le 1.0) \end{aligned} \tag{4.30}$$

The six-step mode is characterized by selection of the switching vector, which is closest to the reference vector for one-sixth of the fundamental period. In this way the modulator generates the maximum possible converter voltage. For a given switching

frequency, the current distortion increases with the modulation index. The distortion factor strongly increases when the reference waveform becomes discontinuous in the mode II.

Algorithm Based on Single Mode of Operation

In a simple technique proposed in [75], the desired voltage angle is held constant when the reference voltage vector is located outside of hexagon. The value, at which the command angle is held, is determined by the intersection of the circle (respond with modulation index) with the hexagon (Fig. 4.20). The angle at which the command is held (hold angles) depends on the desired modulation index (M) and can be found from Eq. (4.31) (max circular trajectory is related to the maximum possible fundamental output voltage $2/\pi U_{dc}$ not to $2/3U_{dc}$ – see Fig. 4.17):

$$\alpha_1 = \arcsin\left(\frac{\sqrt{3}}{2M'}\right) \tag{4.31a}$$

$$M' = \left(\frac{2\sqrt{3}-3}{2\sqrt{3}-\pi}\right)M + \left(\frac{3-\pi}{2\sqrt{3}-\pi}\right) \tag{4.31b}$$

$$\alpha_2 = \frac{\pi}{3} - \alpha_1 \tag{4.31c}$$

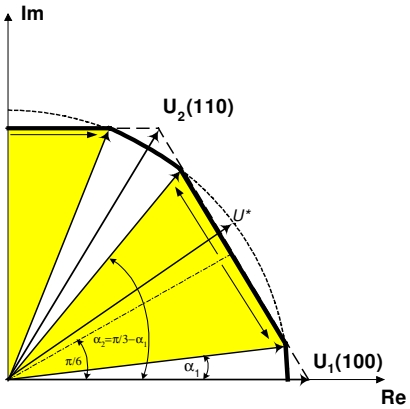


Fig. 4.20 Overmodulation: single mode of operation
U* - reference trajectory (dashed line), U – modified reference trajectory (solid line)

For a desired angle between 0 and α_1, the commanded angle tracks its value. When the desired angle increases over α_1, the commanded angle stays at α_1 until the desired angle becomes $\pi/6$. After that, the commanded angle jumps to value of $\alpha_2 = \pi/3-\alpha_1$. The commanded value of α is kept constant at α_2 for any desired angle between $\pi/6$ and α_2. For a desired angle between α_2 and $\pi/3$, the commanded angle tracks the value of desired angle, as in Fig. 4.20. The advantage of linearity and easy implementation is obtained on the cost of higher harmonic distortion.

4.4.6 Performance criteria

Several performance criteria are considered for selection of suitable modulation method [3]. Some of them are defined in the Table 4.1. Below further important criteria as: range of linear operation, current distortion factor and switching losses are discussed.

Range of linear operation

The linear range of the control characteristic for sinusoidal *CB-PWM* ends at $M = \pi/4 = 0.785$ ($m = 1$) of modulation index (Fig. 4.21) i.e. to equal of reference and carrier peak. The *SVM* or *CB-PWM* with *ZSS* injection provide extension of linear range up to $M_{max} = \pi / 2\sqrt{3} = 0.907$ ($m_{max} = 1.15$). The region above $M = 0.907$ is the non-linear overmodulation range.

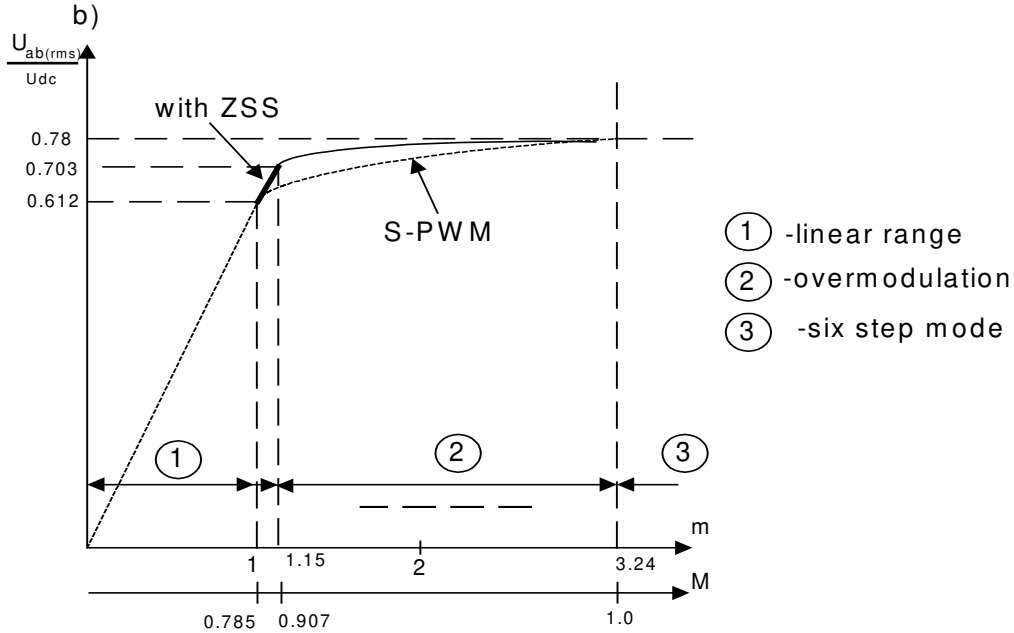


Fig. 4.21 Control characteristic of PWM converter

Switching losses

Power losses of the *PWM* converter can be generally divided into: conduction and switching losses (see in [87]). Conduction losses are practically the same for different *PWM* techniques and they are lower than switching losses. For the switching losses calculation, the linear dependency of a switching energy loss on the switched current is assumed. This also was proved by the measurement results [87]. Therefore, for high switching frequency, the total average value of the transistor switching power losses can be for the continuous *PWM* expressed as:

$$P_{sl(c)} = \frac{1}{2\pi} \int_{-\frac{\pi}{2}+\varphi}^{\frac{\pi}{2}+\varphi} k_{TD} \cdot i \cdot f_s d\alpha = \frac{k_{TD} I f_s}{\pi} \tag{4.32}$$

where: $k_{TD} = k_T + k_D$ - proportional relation of the switching energy loss per pulse period to the switched current for the transistor and the diode.

In the case of discontinuous *PWM* the following properties hold from the symmetry of the pole voltage:

$$P_{sl}(-\varphi) = P_{sl}(\varphi)$$
$$P_{sl}(\varphi) = P_{sl}(\pi - \varphi) \qquad \text{where} \qquad 0<\varphi<\pi. \tag{4.33}$$

Therefore, it is sufficient to consider the range of from *0* to *π/2* for the *DPWM* as follows [87]:

$$PWM(1) \Rightarrow P_{sl}(\varphi) = \begin{cases} P_{sl(c)} \cdot (1 - \frac{1}{2}\cos\varphi) & for\ 0 < \varphi < \pi/3 \\ P_{sl(c)} \cdot \frac{\sqrt{3}\sin\varphi}{2}) & for\ \pi/3 < \varphi < \pi/2 \end{cases} \tag{4.34}$$

$$PWM(0) \Rightarrow P_{sl}(\varphi) = P_{sl(PWM(1))} \cdot (\varphi - \frac{\pi}{6}) \tag{4.35}$$

$$PWM(2) \Rightarrow P_{sl}(\varphi) = P_{sl(PWM(1))} \cdot (\varphi + \frac{\pi}{6}) \tag{4.36}$$

$$PWM(3) \Rightarrow P_{sl}(\varphi) = \begin{cases} P_{sl(c)} \cdot (1 - \frac{\sqrt{3}-1}{2}\cos\varphi) & for\ 0 < \varphi < \pi/6 \\ P_{sl(c)} \cdot \frac{\sin\varphi + \cos\varphi}{2} & for\ \pi/6 < \varphi < \pi/3 \\ P_{sl(c)} \cdot (1 - \frac{\sqrt{3}-1}{2}\sin\varphi) & for\ \pi/3 < \varphi < \pi/2 \end{cases} \tag{4.37}$$

Switching losses depends on type of discontinuous modulation and power factor angle what is shown in Fig. 4.22 (comparison to continuous modulation). Since the switching losses increase with the magnitude of the phase current (approximately linearly), selecting a suitable modulation can significantly improve performance of the converter. Switching losses are average reduced about 33%. In favour conditions, when modulation is clamped in phase conducting max. current, switching losses decrease up to 50%.

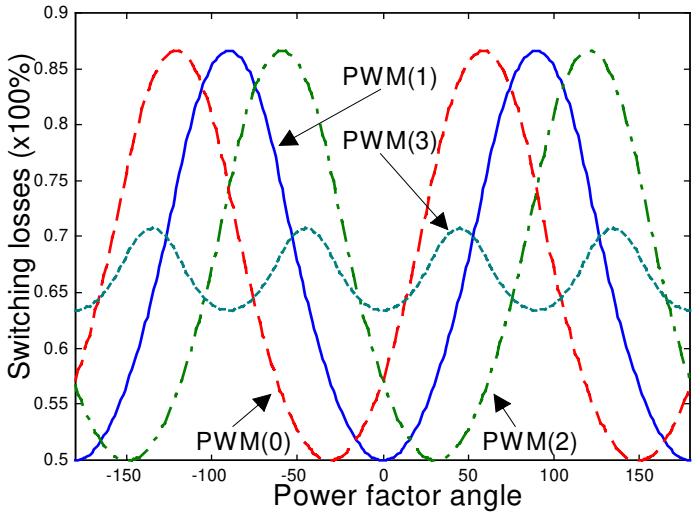


Fig. 4.22. Switching losses ($P_{sl(\varphi)}/P_{sl(c)}$) versus power factor angle

Distortion and Harmonic Copper Loss Factor

The current waveform quality of the *PWM* converter is determined by harmonics of switching frequency what have influence for copper losses and the instantaneous power ripple. Harmonics are changed according to the selected switching sequence. Detailed description is presented in [84, 98]. The rms harmonic current defined as:

$$I_{h(rms)} = \sqrt{\frac{1}{T}\int_0^T [i_L(t) - i_{L1}(t)]^2 \, dt} \quad , \tag{4.38}$$

depends on type of *PWM* and *AC* side impedance. To eliminate influence of *AC* side impedance parameters, the distortion factor is commonly used (see Table 4.1):

$$d = \mathrm{I_{h(rms)}} / \mathrm{I_{h(six\text{-}step)(rms)}} \tag{4.39}$$

For six-step operation the distortion factor is $d = 1$. It should be noted that harmonic copper losses in the *AC*-side are proportional to $\boldsymbol{d^2}$. Therefore, $\boldsymbol{d^2}$ can be considered as a loss factor. Values of loss factor can be compute for different modulation methods [3,87]. It depends on switching frequency, modulation index *M*, and shape of the *ZSS* (Fig. 4.23):

- for continuous modulation:

$$SPWM \quad d = \frac{4M}{\sqrt{6}\pi k_{f_{SB}}} \sqrt{1 - \frac{32M}{\sqrt{3}\pi^2} + \frac{3M^2}{\pi}} \quad M \in \left[0, \frac{\pi}{4}\right] \tag{4.40}$$

$$SVPWM \quad d = \frac{4M}{\sqrt{6}\pi k_{f_{SB}}} \sqrt{1 - \frac{32M}{\sqrt{3}\pi^2} + \frac{9M^2}{2\pi}\left(1 - \frac{3\sqrt{3}}{4\pi}\right)} \quad M \in \left[0, \frac{\pi}{2\sqrt{3}}\right] \tag{4.41}$$

- for discontinuous modulation (*DPWM*):

$$DPWM1 \quad d = \frac{4M}{\sqrt{6}\pi k_{f_{SB}}} \sqrt{4 - \frac{4M}{\sqrt{3}\pi^2}\left(8 + 15\sqrt{3}\right) + \frac{9M^2}{2\pi}\left(2 + \frac{\sqrt{3}}{2\pi}\right)} \quad M \in \left[0, \frac{\pi}{2\sqrt{3}}\right] \tag{4.42}$$

$$DPWM0(2) \quad d = \frac{4M}{\sqrt{6}\pi k_{f_{SB}}} \sqrt{4 - \frac{140M}{\sqrt{3}\pi^2} + \frac{9M^2}{2\pi}\left(2 + \frac{3\sqrt{3}}{4\pi}\right)} \quad M \in \left[0, \frac{\pi}{2\sqrt{3}}\right] \tag{4.43}$$

$$DPWM3 \quad d = \frac{4M}{\sqrt{6}\pi k_{f_{SB}}} \sqrt{4 - \frac{4M}{\sqrt{3}\pi^2}\left(62 - 15\sqrt{3}\right) + \frac{9M^2}{2\pi}\left(2 + \frac{\sqrt{3}}{\pi}\right)} \quad M \in \left[0, \frac{\pi}{2\sqrt{3}}\right] \tag{4.44}$$

where $k_{f_{SB}}$ is defined as a ratio of carrier frequency (sampling time) to base of carrier frequency. All continuous *PWM* have the advantage over *DPWM* methods for the sake of small distortion factor in the low range of modulation. When the modulation index increases and the *PWM* performance rapidly decreases, the *SVPWM* maintain at lowest distortion factor. The harmonic content for *SVPWM* and *DPWM* at the same carrier frequency is similar at high modulation index only (Fig. 4.23). However, we should remember that *DPWM* possess lower switching losses. Therefore, the carrier frequency can be increased by factor 3/2 for 33% reduction of switching losses, or 2 times increased for 50% reduction of switching losses. It provides to lower current distortion for *DPWM* in comparison to *SVPWM*.

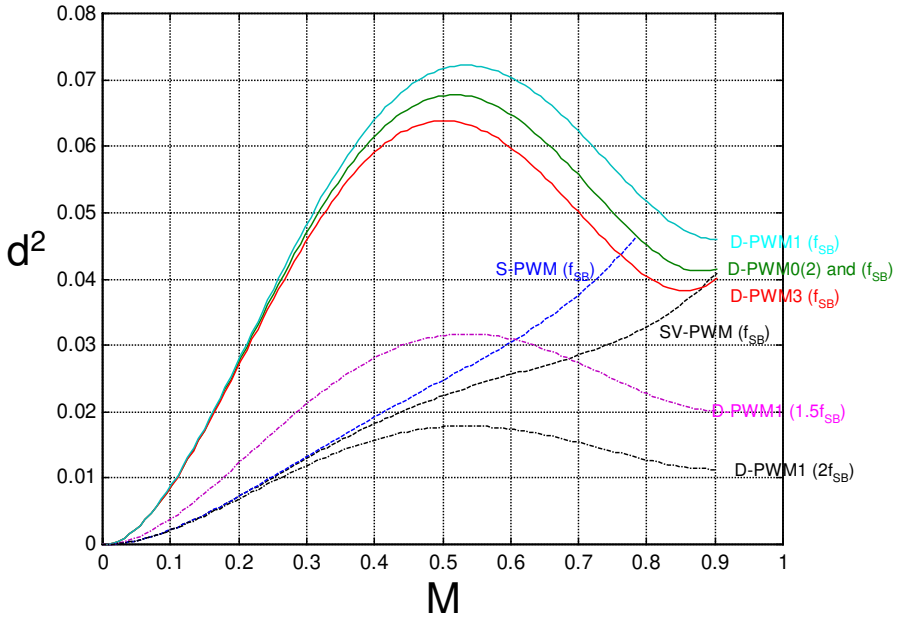


Fig. 4.23. Square of current distortion factor as function of modulation index.

4.4.7 Adaptive Space Vector Modulation (ASVM)

The concept of adaptive space vector modulation (*ASVM*) proposed by Author [93, Patent No. P340113] provides:

- full control range including overmodulation and six-step operation,
- theoretically, up to 50% reduction of switching losses at 33% reduction of average switching frequency,
- high dynamics.

The above features are achieved by use of four different modes of *SVM* with an instantaneous tracking of the *AC* current peak and an optimal switching table for fast response to step changes of the load. Four *PWM* operation modes are distributed in the range of modulation index (*M*) as follows (Fig. 4.24a):

A: $0 < M \leq 0.5$ – conventional *SVM* with symmetrical zero switching states,
B: $0.5 < M \leq 0.908$ – discontinuous SVM with one zero state per sampling time (two-phase or flap top *PWM*),
C: $0.908 < M \leq 0.95$ – overmodulation mode I, (see Section 4.4.6)
D: $0.95 < M \leq 1$ – overmodulation mode II.

The combination of regions *A* with *B* without current tracing, suggested in [72,80] is known as hybrid *PWM*. In the region *B* of discontinuous *PWM*, for maximal reduction of switching losses, the peak of the current should be located in the centre of "flat" parts. Therefore, it is necessary to observe the peak current position. Components $i_{L\alpha}$, $i_{L\beta}$ of the measured current are transformed into polar coordinates and compared with voltage reference angle (Eq. (4.45)). It gives possibility to identify power factor angle φ, which decide about placement of clamped region. Thus, the ring from Fig. 24b will be adequately moved (φ). For each of sector:

$$\text{if } \alpha < \varphi + \kappa \quad \Rightarrow t_0 = 0 \qquad (4.45)$$
$$\text{if } \alpha > \varphi + \kappa \quad \Rightarrow t_7 = 0$$

where: α - reference voltage angle, φ – power factor angle, κ - for successive sectors $\pi/6$, $\pi/2$, $5\pi/6$, $7\pi/6$, $3\pi/2$, $11\pi/6$

This provides tracking of the power factor angle in full range of φ (from $-\pi$ to π), what guarantees maximal reduction of switching losses (Fig. 4.25)

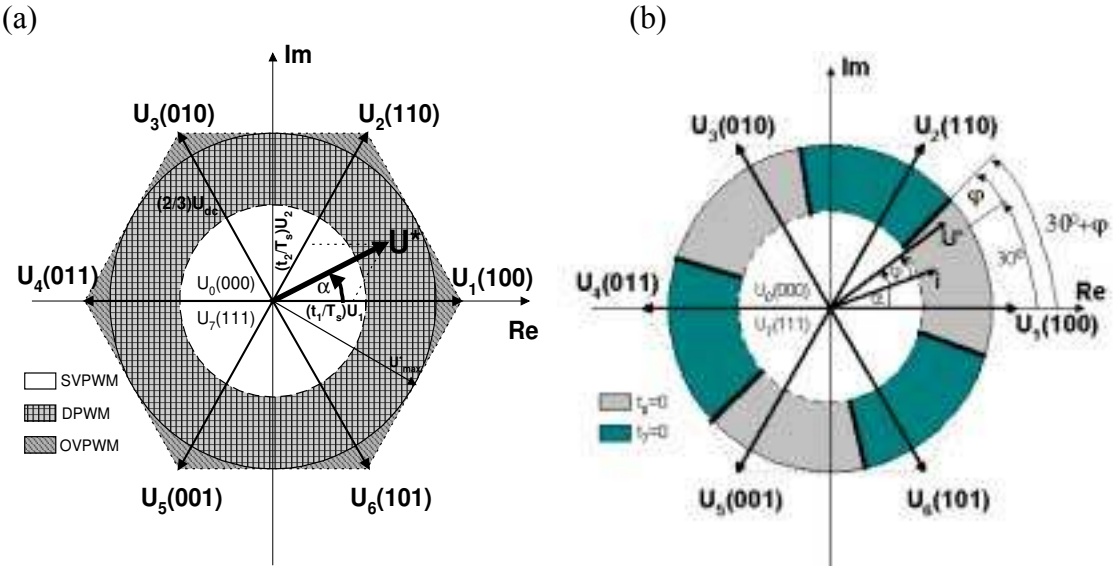


Fig. 4.24. Adaptive modulator
a) effect of modulation index b) effect of power factor angle

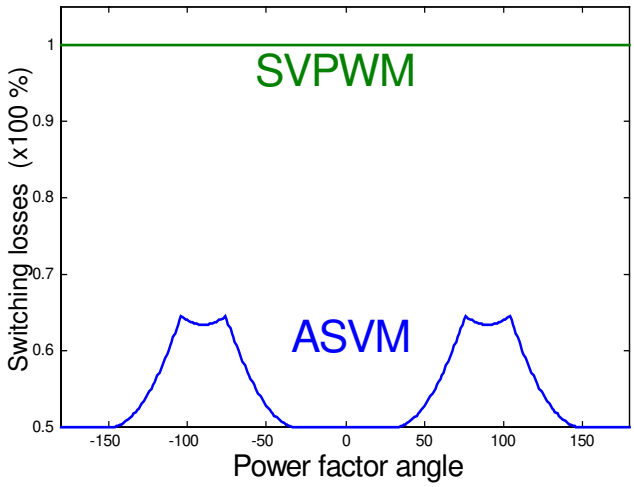


Fig. 4.25. Switching losses versus power factor angle for conventional *SVPWM* and *ASVM*

The dynamic state is identified after step change of load what results that switching table is used. After returning to steady state the *ASVM* operates like a conventional *SVM*. The full algorithm of adaptive modulator is presented in Fig. 4.26. Fig. 4.27 shows an example of implementation in a current regulator. Adaptive modulation with simplified switching time calculation is described in A.3.

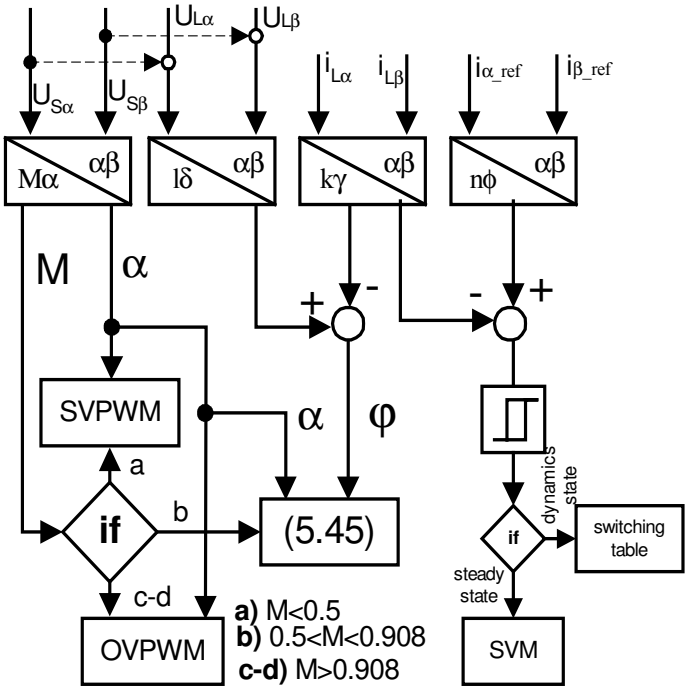


Fig. 4.26. Algorithm of *ASVM*

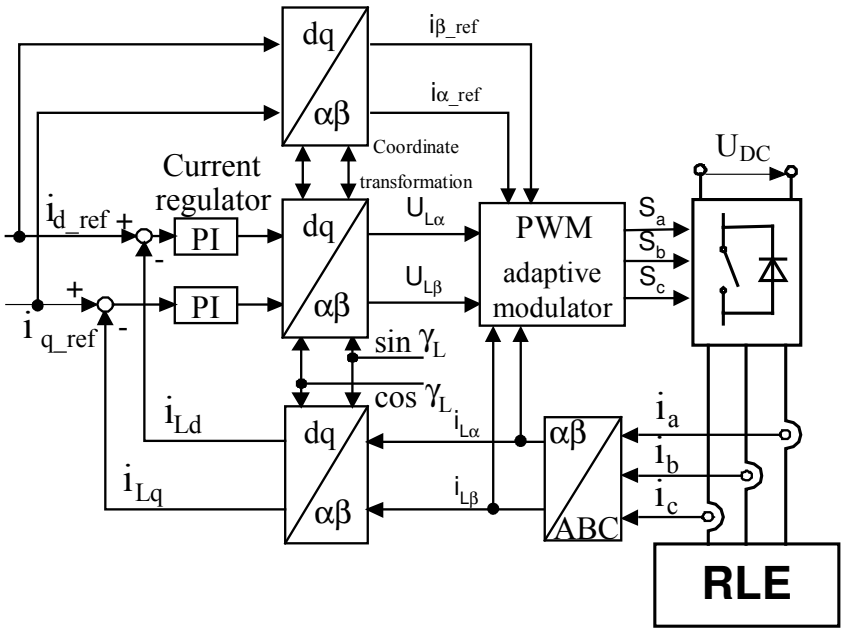


Fig. 4.27: *ASVM* in *PI* synchronous current controller.

4.4.8 Simulation and experimental results of modulation

Simulation of *CB-PWM* with additional *ZSS* was realized in *SIMULINK* [A.5]. Fig. 4.28 presents results of: sinusoidal modulation (*SPWM*), modulation with 3-th harmonic (amplitude 1/6), analogue *SVPWM* and *DPWM1*.
Simulations of *SVM* are made in the *DESIM*. Selected results which illustrate work of modulators with U_{N0} = 0, 3-th harmonic, three-phase modulation *SVPWM* and two-phase modulation with one zero states in sampling time are shown on Fig. 4.29-4.30.
Discussed method of *SVM* was implemented on the laboratory setup described in A.6. Investigation was done with 100μs sampling time and *dead-time* compensation algorithm [A.3]. Experimental results for different variants of *SVM* are shown in Fig. 4.29-4.30. Results presents that higher harmonic ripple at low modulation index is one disadvantage of *DPWM* compared to *SVPWM*. This drawback can be neglected for PWM rectifier, because under normal conditions the PWM rectifier operates, at high linear modulation index. Much more important is that *DPWM* provides lower switching losses in the converter.
ASVM is an universal solution for different kind of PWM converters, therefore investigation was carried-out both for PWM rectifier using Voltage Oriented Control (*VOC*) [44] and PWM inverter using Indirect Field Oriented Control (*IFOC*) [4]. Experimental results of *ASVM* are presented in Fig. 4.31-4.32. Fig. 4.33 presents comparison of phase currents at step change of load.
Moreover, it was found that ASVM in Cartesian coordinates is three-times less time-consuming than its counterpart in polar coordinates [A.3].

MODULATION WITH ADDITIONAL ZSS (SIMULATION)

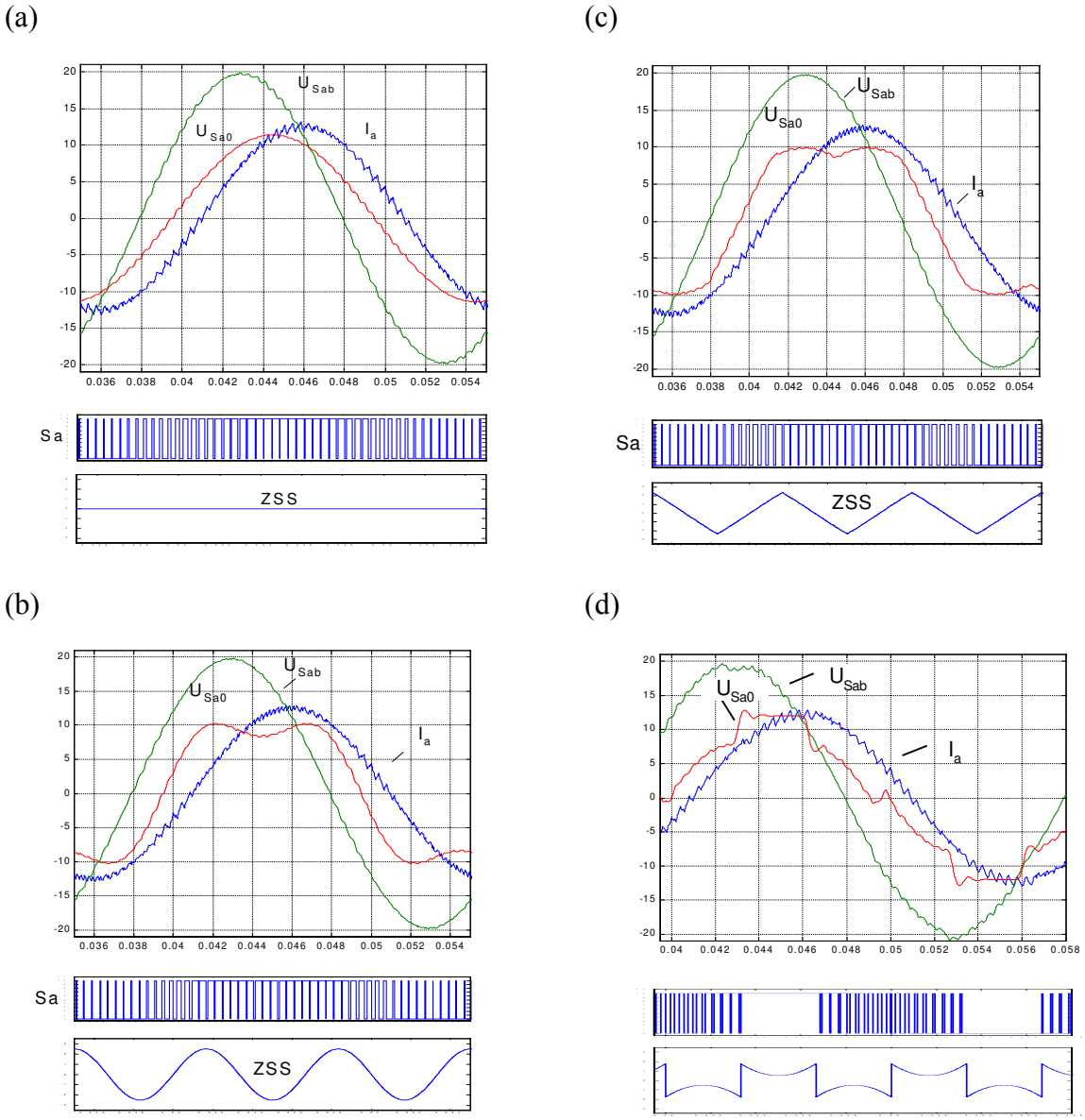


Fig. 4.28. Simulation results for CB-PWM with additional ZSS (Fig. 4.9): *a) SPWM* b) *with 3-th harmonic c) analogue SVPWM d) DPWM1.* Each of cases presents : $u_{Sab,}$ - filtered line to line voltage of converter, u_{Sa0} – filtered pole voltage, i_a - phase current, pulses S_a and *ZSS*; *(m=0.95)*

SPACE VECTOR MODULATION

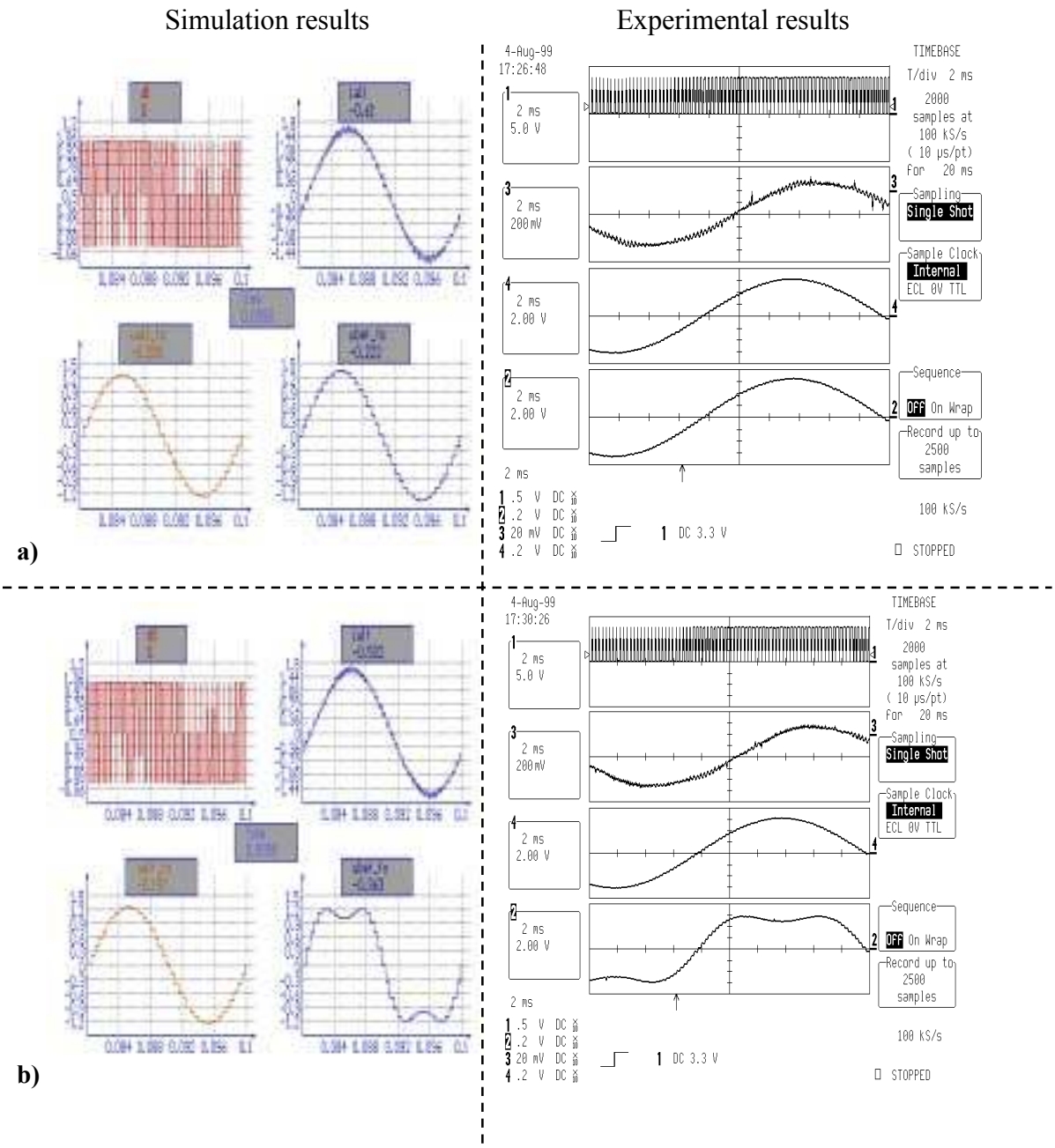


Fig. 4.29. Simulation and experimental results for various *SVM* (Fig. 4.12b):
a) with $U_{N0} = 0$ (*SPWM*) b) with 3-th harmonic.
Each of cases presents: pulses S_a, phase current i_a, phase voltage u_{SaN}
and pole voltage u_{Sa0} (estimated from U_{dc} and switching state).

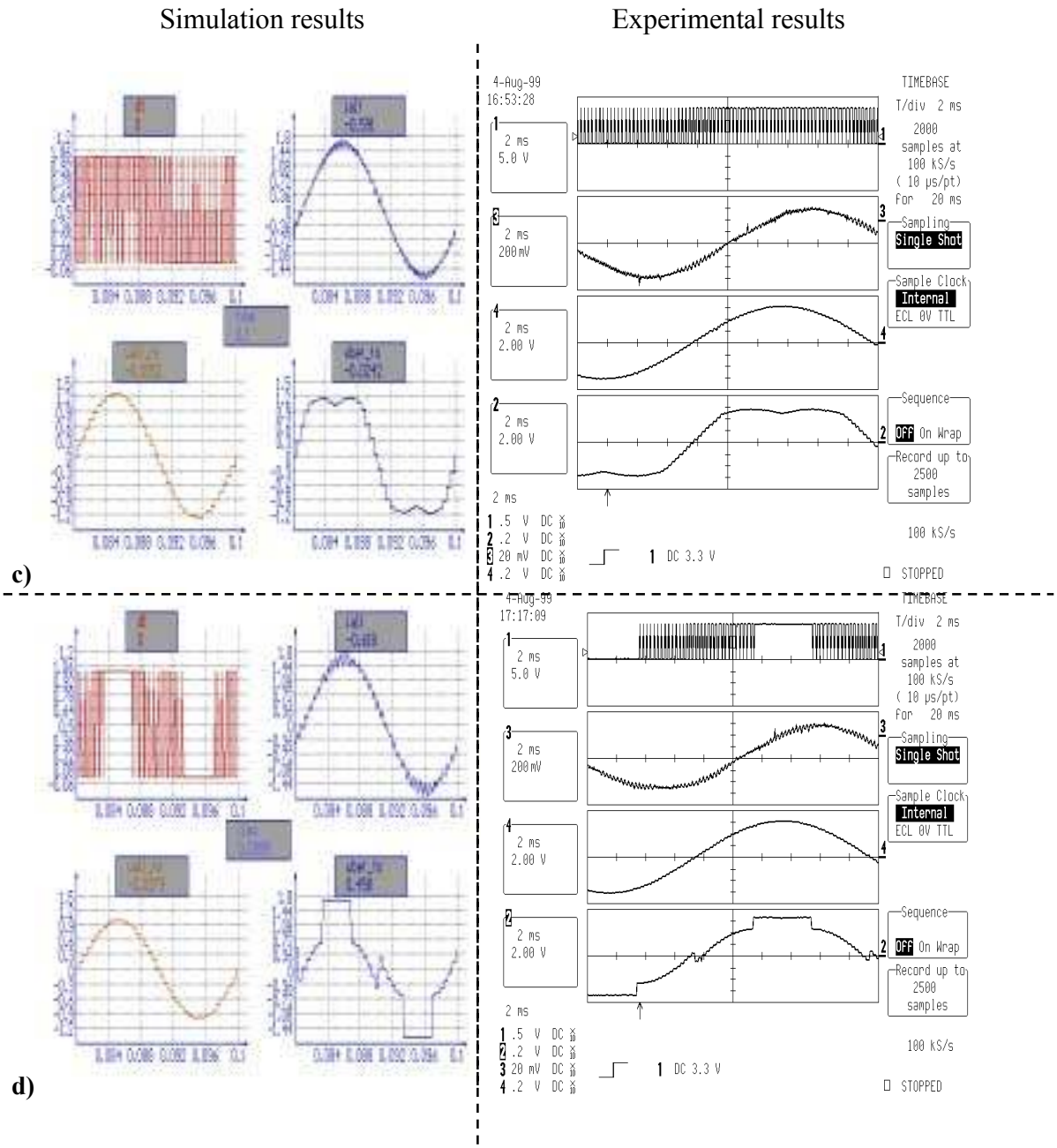


Fig. 4.30. Simulation and experimental results for various *SVM (Fig. 4.12)*:
c) three-phase *SVM* with symmetrical zero states (*SVPWM*) d) two-phase *SVM* (*PWM(1))*.
Each of cases presents: pulses S_a, phase current i_a, phase voltage u_{SaN}
and pole voltage u_{Sa0} (estimated from U_{dc} and switching state).

ADAPTIVE SPACE VECTOR MODULATION (ASVM)

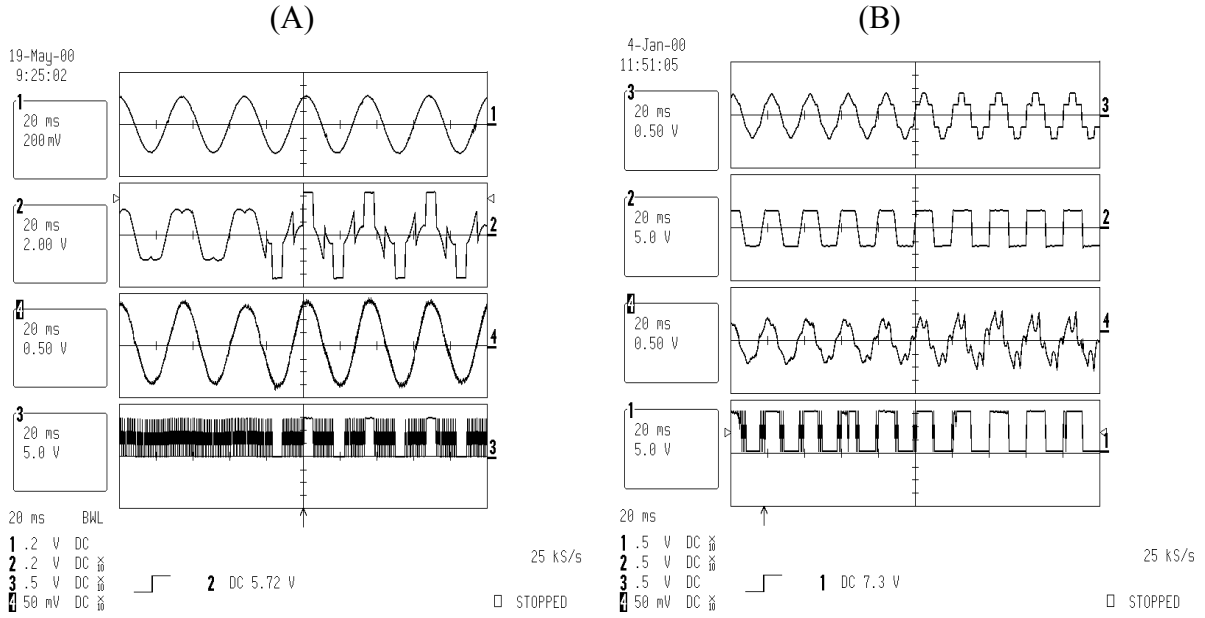


Fig. 4.31. Experimental waveforms of *VS* converter with adaptive modulation
(A) transition from three to two – phase *SVM*,
(B) transition from overmodulation to six–step operation.
From the top: phase voltage u_{SaN} and pole voltage u_{Sa0}
(estimated from U_{dc} and switching state), current i_a, pulses S_a.

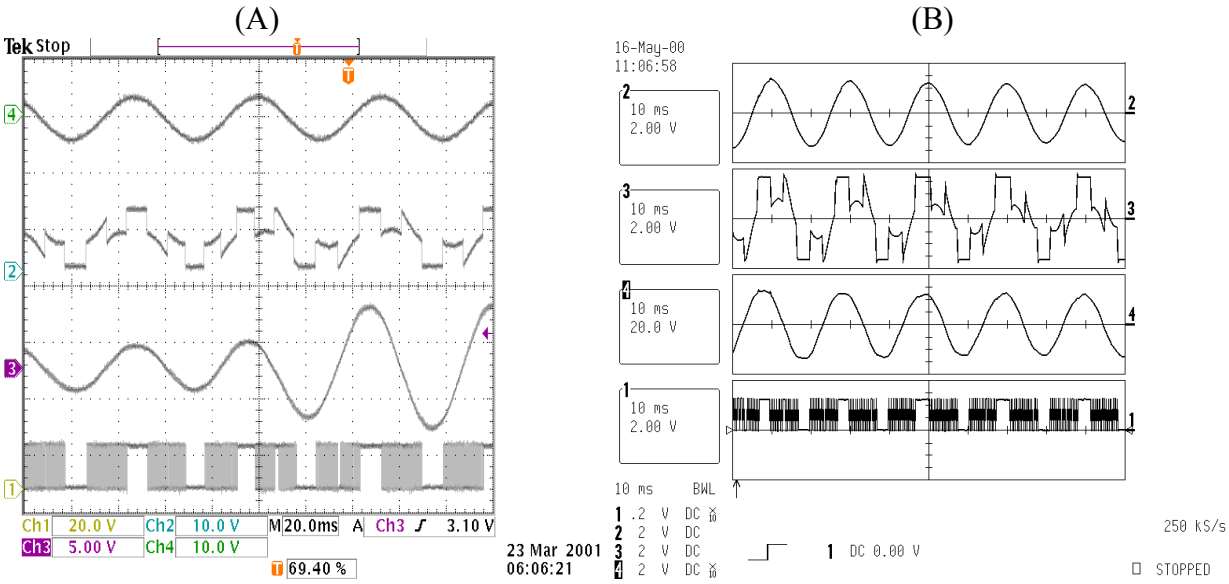


Fig. 4.32. Experimental waveforms of (A) *VS* converter with adaptive modulation for two - phase *SVM* – peak current tracing during load change, (B) *VS* line rectifier with adaptive modulation: two–phase *SVM* – peak current tracing during reactive power change.
From the top: phase voltage u_{SaN} and pole voltage u_{Sa0}
(estimated from U_{dc} and switching state), current i_a, pulses S_a.

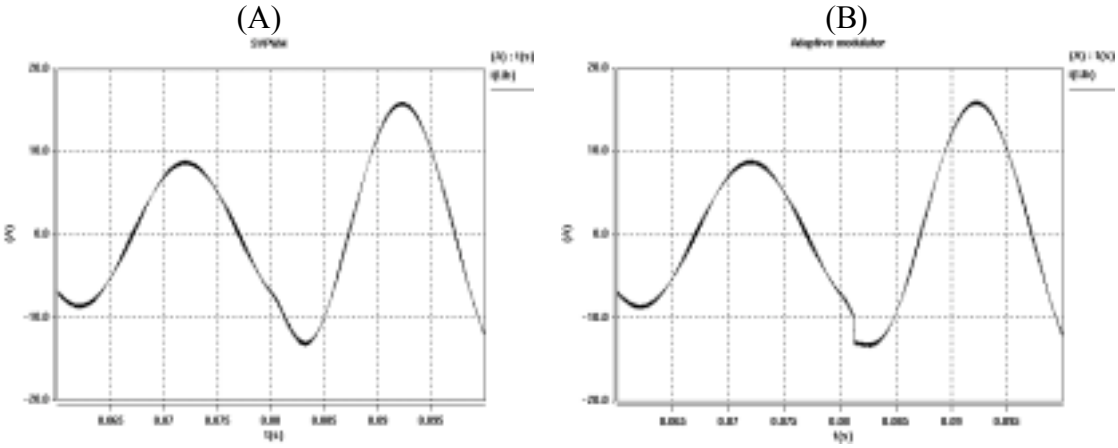


Fig. 4.33: Simulation results of phase current response at 100% step change of load for PWM rectifier with A) *SVPWM* B) *ASVM*

4.4.9 Summary of modulation

This chapter has shown many of the *PWM* techniques developed during recent years. Most important conclusions can be summarized as below:

- parameters of *PWM* converter (linear range of operation, current harmonic and switching losses in power components) depends on:
  - zero vectors placement in *SVM*,
  - shape of zero sequence signal (*ZSS*) in *CB-PWM*.
- there is no one method of *PWM*, which provide minimal current distortion in whole range of control (Fig. 4.23),
- three-phase *SVM* with symmetrical zero states *(SVPWM)* should be used in low range of modulation index, two-phase *SVM* with one zero state in sampling time *(DPWM)* should be used in high range of modulation index,
- maximal reduction of switching losses in *DPWM* is achieved when the peak of the line current is located in the centre of clamped (not switching) region (Fig. 4.22),
- *SVPWM* and *DPWM* should be applied for industrial applications, because both methods have low time-consuming algorithms and high linearity,
- Adaptive Space Vector Modulation (*ASVM*) is a universal solution for three-phase PWM converter, among its main features are: full control range including overmodulation and six-step operation, tracking of peak current for instantaneous selection of two-phase PWM (this guarantees maximal reduction of switching losses up to 50%), higher efficiency of the converter and high dynamics by switching table application,
- *ASVM* with simplified switching time calculation provide low time consuming algorithm based on implementation in Cartesian coordinates, it gives three times less time consuming algorithm than it's counterpart in polar coordinates.

4.5 SIMULATION AND EXPERIMENTAL RESULTS

The main parameters of the system under consideration are summarized in Table A.4.1 and Table A.6.2. The research has been carried out for two cases:

- ideal line voltage (balanced and sinusoidal),
- distorted line voltage with 5% 5^{th} harmonics and 4.5% unbalance [see A.1].

A PWM rectifier with the presented control schemes has been simulated using *SABER* [A4]. The simulated waveforms for *VOC* with *SVPWM* and *VOC* with *DPWM* under purely sinusoidal line voltage are presented in Fig. 4.34 and Fig. 4.35 respectively. The switching and sampling frequency is 5kHz for *VOC-SVPWM*. The current has only a total harmonic distortion (*THD*) of 4.5 %, and the estimated line voltage is very close to the real supply voltage. The simulation results for the *VOC* with *DPWM* presents that the current *THD* is only 2.6 %. The difference to the classical control with *SVPWM* is mainly because of a higher sampling and switching frequency. In *DPWM* the switching frequency can be twice as high with the same switching losses what can reduce the size of the input filter. A more practical advantages for the industry is shown by [99]. Therefore the simulations are made with a sampling frequency of 10 kHz. The estimated line voltage is very close to the real supply voltage.

Fig. 4.36 shows the simulation results for the *VOC* with *SVPWM* where the supply voltage is pre-distorted and unbalanced. The *THD* of the line current is 11.8% because of a high content of 5^{th} harmonic current. The estimated line voltage is still very close to the real supply voltage and the current follows the voltage very well. Fig. 4.37 shows the simulation results for the classical control with *DPWM* where the supply voltage is pre-distorted and unbalanced. The *THD* of the line current is 10.1%. The estimated line voltage is still very close to the real supply voltage and the current follows the voltage well. These oscillograms are obtained for the same operation conditions. Note, that the estimated line voltage follows the actual line voltage very close for both under pre-distorted and unbalanced conditions as well as under ideal conditions. There is a small time delay of one sample because the old value of the rectifier voltage reference is added to the estimated voltage drop across the inductance. In classical control the voltage is not as important as the angle γ between the fixed reference frame and the rotating reference frame. The angle γ can be feed-forward compensated by adding $\Delta\gamma$. $\Delta\gamma$ can be calculated as a function of the line frequency and the sampling frequency.

The experimental results for the conventional *VOC* strategy and no *AC*-line voltage sensors with *SVPWM* and *DPWM* modulation techniques were realized on laboratory setup presented in A.7 and they are presented in Fig. 4.34-Fig. 4.37. The simulation and experimental results for the *VFOC* and no AC-line voltage sensors with *SVPWM* are presented in Fig. 4.38. The current has only 4.5% of *THD* at purely sinusoidal voltage (similarly to *VOC*). For non-sinusoidal line voltage the *THD* of current for *VFOC* is lower than *VOC*.

The current total harmonic distortion factor (*THD*) together with the different operating conditions for the two control schemes are summarized in Table 5.1.

Transient of the step change of the load for *VOC* are presented in Fig. 4.39 (current controllers without decoupling) and Fig. 4.40 (current controllers with decoupling). Results show that decoupled control system of PWM rectifier possess better performance.

STEADY STATE BEHAVIOUR

➢ *RESULTS UNDER PURELY SINUSOIDAL LINE VOLTAGE OF VOC*

(a) SIMULATION (b) EXPERIMENT

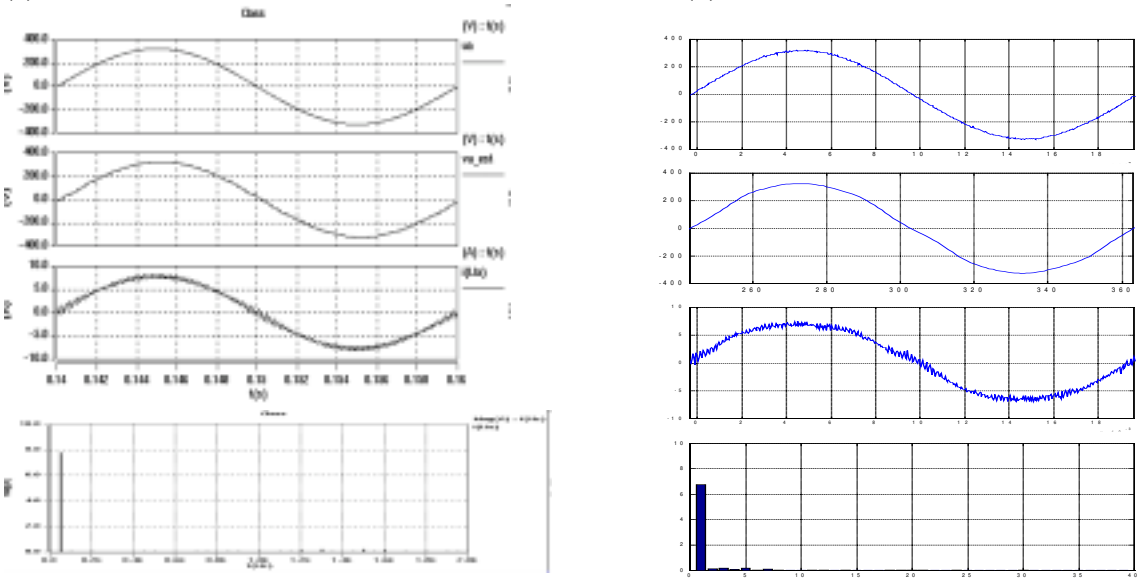


Fig. 4.34: Line voltage, estimated line voltage and input current, together with the harmonic spectrum of the input current for the *VOC* with *SVPWM*: a) simulation results (the current *THD* = 4,5 %); b) experimental results (the current *THD* = 6,1 %).

(a) (b)

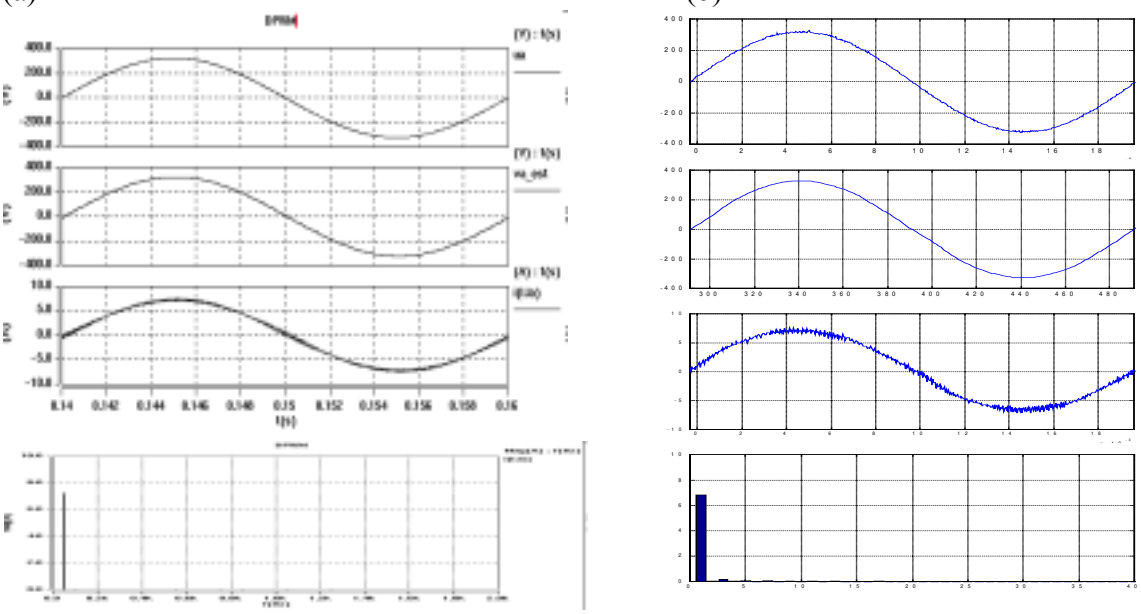


Fig. 4.35: Line voltage, estimated line voltage and input current, together with the harmonic spectrum of the input current for the *VOC* with *DPWM*: a) simulation results (the current *THD* = 2,6 %.); b) experimental results (the current *THD* = 3,1 %).

➢ *RESULTS UNDER NON SINUSOIDAL LINE VOLTAGE OF VOC*

(a) SIMULATION (b) EXPERIMENT

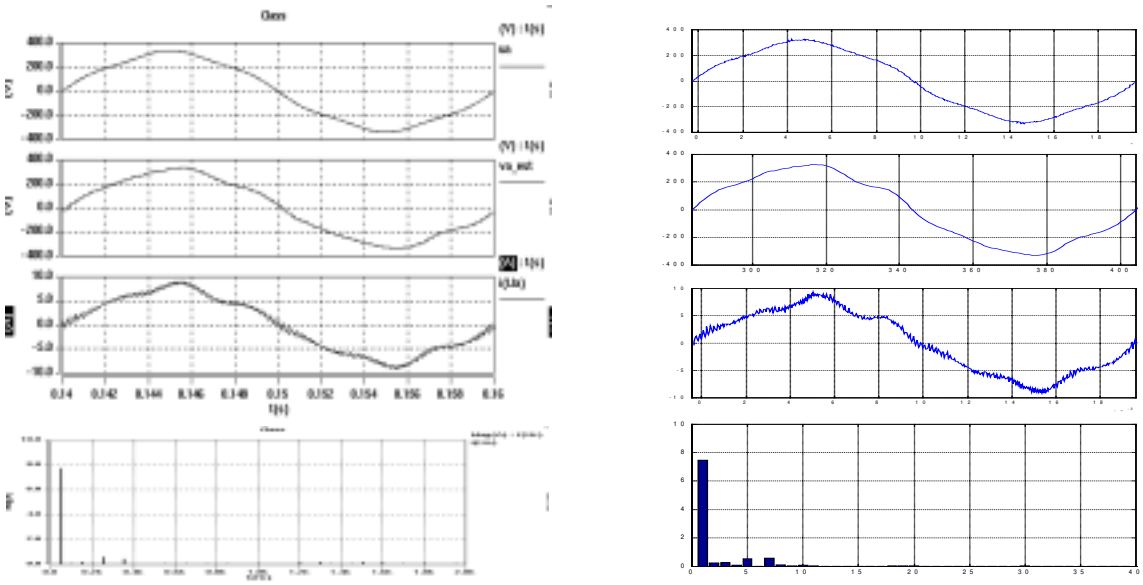


Fig. 4.36: Line voltage, estimated line voltage and input current, together with the harmonic spectrum of the input current for the *VOC* with *SVPWM* and 4.5% voltage unbalance and 5% 5th harmonic voltage: a) simulation results (the current *THD* = 9,2 %); b) experimental results (the current *THD* = 11,8 %).

(a) (b)

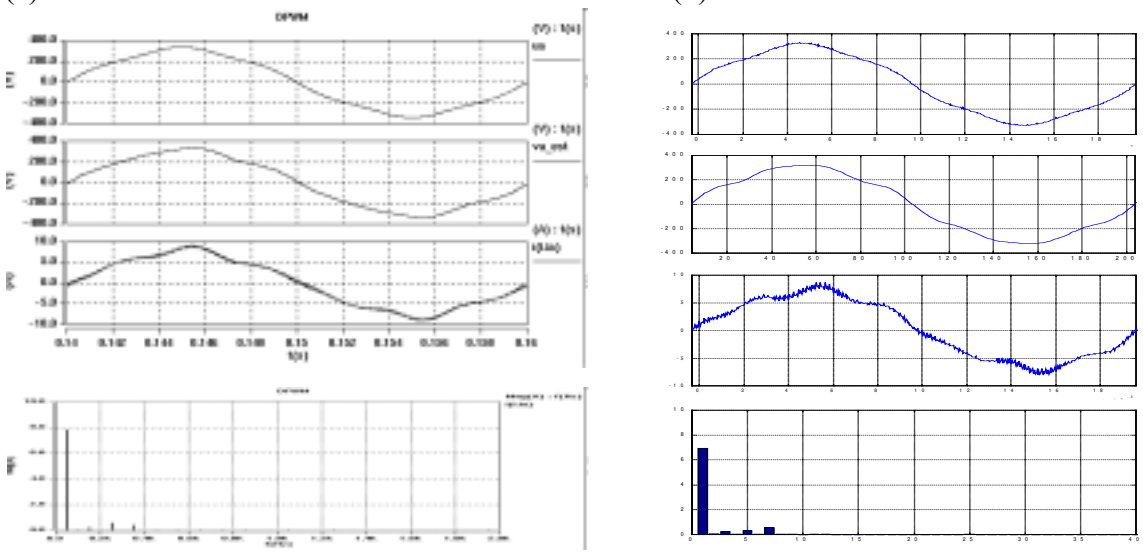
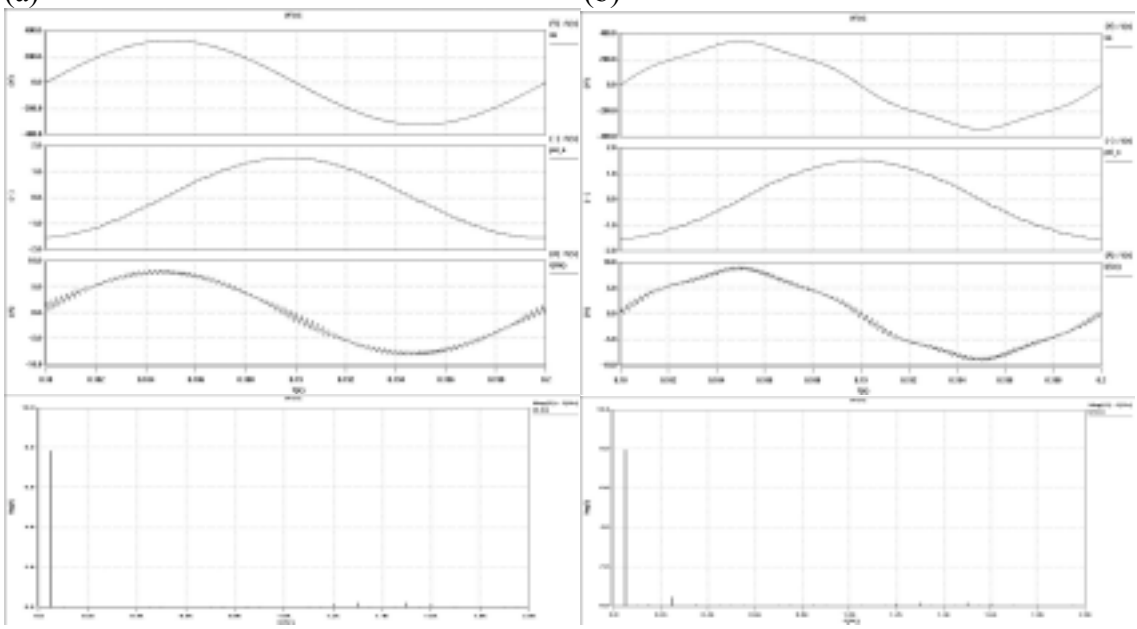


Fig. 4.37: Line voltage, estimated line voltage and input current, together with the harmonic spectrum of the input current for the *VOC* with *DPWM* and 4.5% voltage unbalance and 5% 5th harmonic voltage: a) simulation results (the current *THD* = 7.1 %); b) experimental results (the current *THD* = 10.1 %).

➢ *RESULTS UNDER PURELY SINUSOIDAL AND NON SINUSOIDAL LINE VOLTAGE OF VFOC*

SIMULATION

(a) (b)



EXPERIMENT

(c)

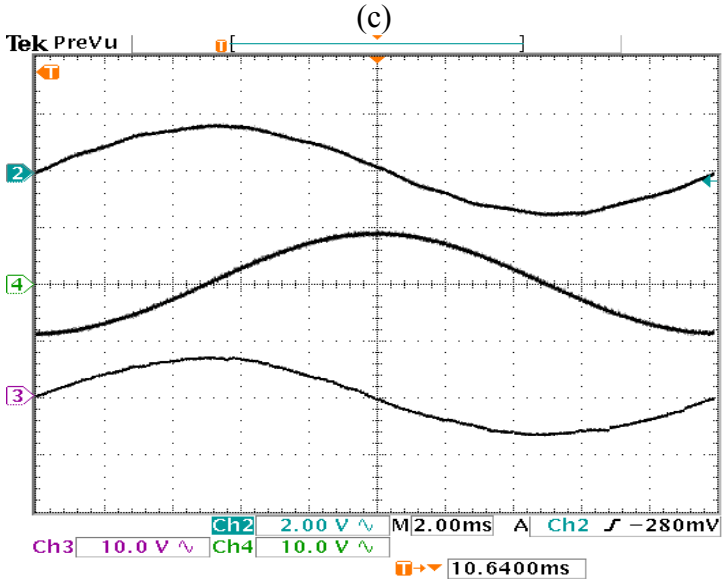


Fig. 4.38: Line voltage, estimated virtual flux and input current, together with the harmonic spectrum of the input current for the *VFOC* with *SVPWM*: a) simulation results for purely sinusoidal line voltage (the current *THD* = 4,5%); b) simulation results for 4.5% voltage unbalance and 5% 5th harmonic voltage (the current *THD* = 8,7 %); c) experimental results (the current *THD* = 10,5 %).

DYNAMIC BEHAVIOUR

- *RESULTS UNDER PURELY SINUSOIDAL LINE VOLTAGE (SIMULATION)*

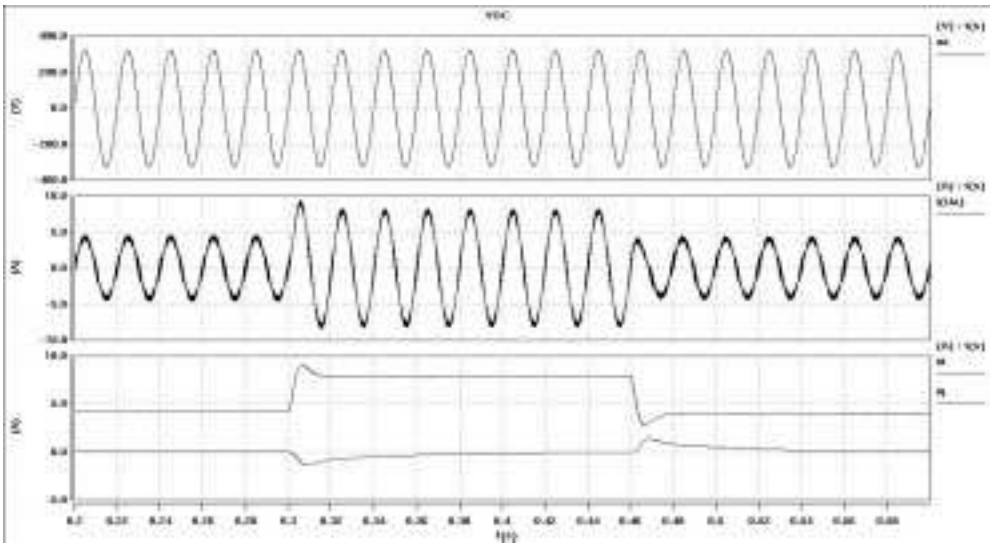


Fig. 4.39. Transient of the step change of the load for *VOC* (current controllers without decoupling). From the top: line voltage, line currents, i_{Ld} and i_{Lq} currents.

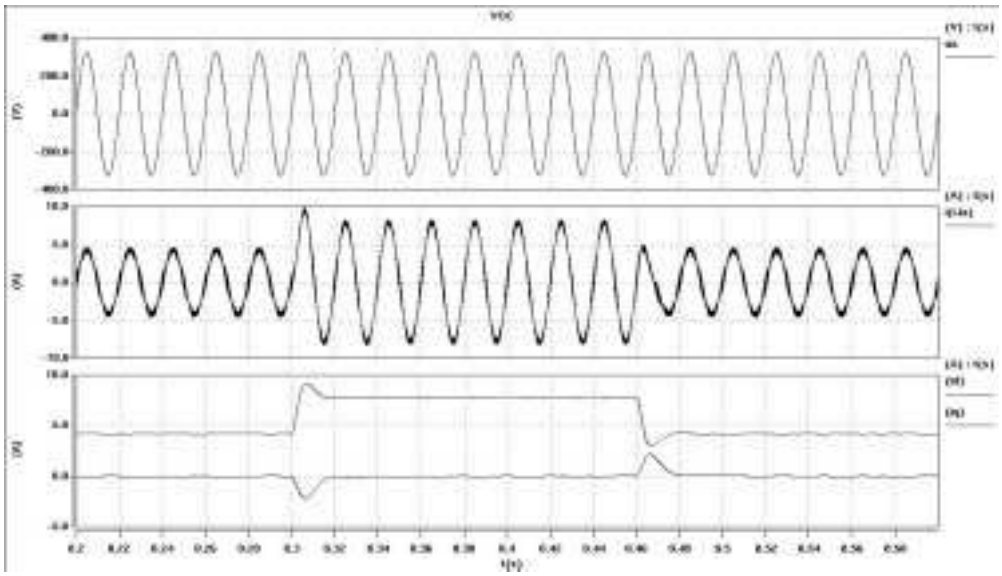


Fig. 4.40. Transient of the step change of the load for *VOC* (current controllers with decoupling). From the top: line voltage, line currents, i_{Ld} and i_{Lq} currents.

4.6 SUMMARY

It is shown by simulations and experimental results that line voltage estimators perform very well even under unbalanced and pre-distorted conditions. Furthermore, the current follows the voltage fairly well with *VOC* control strategies what provide high value of total power factor. However, sometimes sinusoidal currents are desired even under unbalanced and pre-distorted conditions because sinusoidal current do not produce non-sinusoidal voltage drops across the line impedance's. For the conventional *VOC* scheme some compensating algorithms exists [35,55,62,63,107] or concept of Virtual Flux *VF* can be applied to improve *VOC* scheme.

The *VOC* with line voltage estimation and *VFOC* with virtual flux estimator, compared to *DPC*, exhibit some advantages:

- low sampling frequency (cheaper A/D converters and micro-controllers) can be used for good performance, e.g. 5kHz,
- fixed switching frequency (easier design of the input filter),
- possible implementation of modern *PWM* techniques (see Section 4.4.7).

Moreover the *VFOC* provide improved rectifier control under non-ideal line voltage condition, because *AC* voltage sensorless operation is much less noisy thanks to the natural low-pass behaviour of the integrator used in the flux estimator.

There are also some disadvantages for both control strategies:

- exist coupling between active and reactive components and some decoupling solution is required,
- coordinate transformation and *PI* controllers are required.

5. COMPARATIVE STUDY

5.1 INTRODUCTION

For better assessment of the individual rectifier control techniques presented, a comparative investigation of these techniques has been carried out. This issue is of great importance to designers and manufacturers of *AC ASD*s. PWM rectifiers have been increasingly employed as front-end converters in these drives (e.g., Siemens or ABB). Results of the investigation are presented below.

5.2 PERFORMANCE COMPARISON

➢ *Condition of study*

All the four control schemes have been simulated using the SABER software [A.4]. Values of the sampling and switching frequency, respectively, were as follows: (a) *VOC* – 5 kHz, 5 kHz, (b) *DPC* – 80 kHz, 5 kHz (average), (c) *VFOC* – 5 kHz, 5 kHz, and (d) *VF-DPC* – 50 kHz, 4 kHz (average). Other parameters of power circuit are given in Table A.4.1. For fairness of the comparison, no outer-loop voltage controller was used in the dynamic investigation. The comparative study was conducted with respect to the complexity of control algorithms, operation with unbalanced and distorted line voltages, parameter sensitivity, and dynamic performance.

➢ *Complexity of control algorithms*

To illustrate differences between the techniques with respect to the computational effort, the number of instructions per sampling cycle is shown in Fig. 5.1. The control strategies utilizing the virtual flux enjoy certain edge over their voltage-based counterparts. Computation intensity, that is, the processor load per sampling cycle, is illustrated in Fig. 5.2 for all methods under consideration. It can be seen that the direct power control strategies require distinctly faster processors than the *VOC* and *VFOC* techniques.

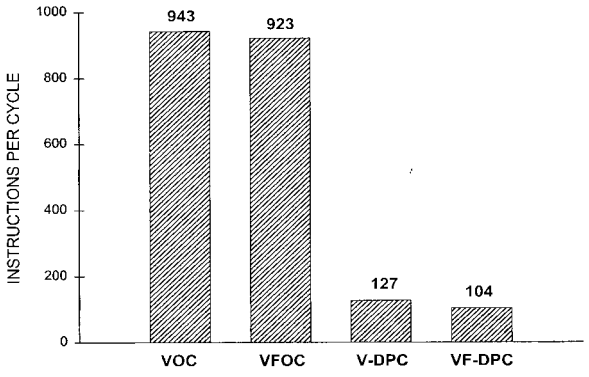


Fig. 5.1 Computational effort (number of instructions per sampling cycle).

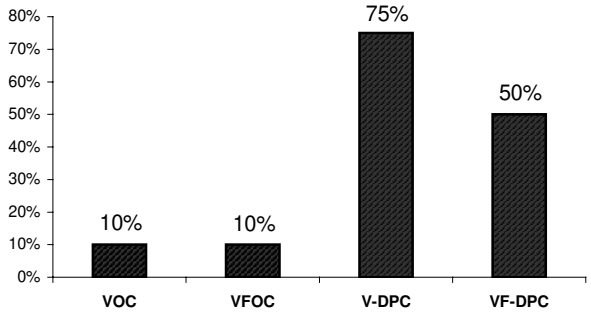


Fig. 5.2 Computation intensity (*dSpace 1103*)

- ***Influence of unbalanced and distorted line voltage***

Under ideal conditions the PWM rectifier should provide sinusoidal line current. However there are three major reasons of disturbances, which may distort the current waveform:

- voltage unbalance,
- voltage distortion,
- distortion of reference instantaneous active power and current (because ripple on u_{dc} created by unbalanced and distorted condition).

With unbalanced line voltage the second harmonic appear in control structure (100Hz). Another two distortion produce most significant harmonic as: 5^{th}, 7^{th}, 11^{th}, 13^{th} and 17^{th}. Fig. 5.3 shows the influence of unbalanced and distorted line voltage on DC-link voltage and reference angle in control structure. Figure 5.3(a) shows basic waveforms of signals, when a ideal voltage is applied. On the other hands, Fig 5.3(b) shows the same waveforms, when the three-phase line voltage is unbalanced and distorted.

(a) Sinusoidal and balanced supply voltage *(b) Distorted and unbalanced supply voltage*

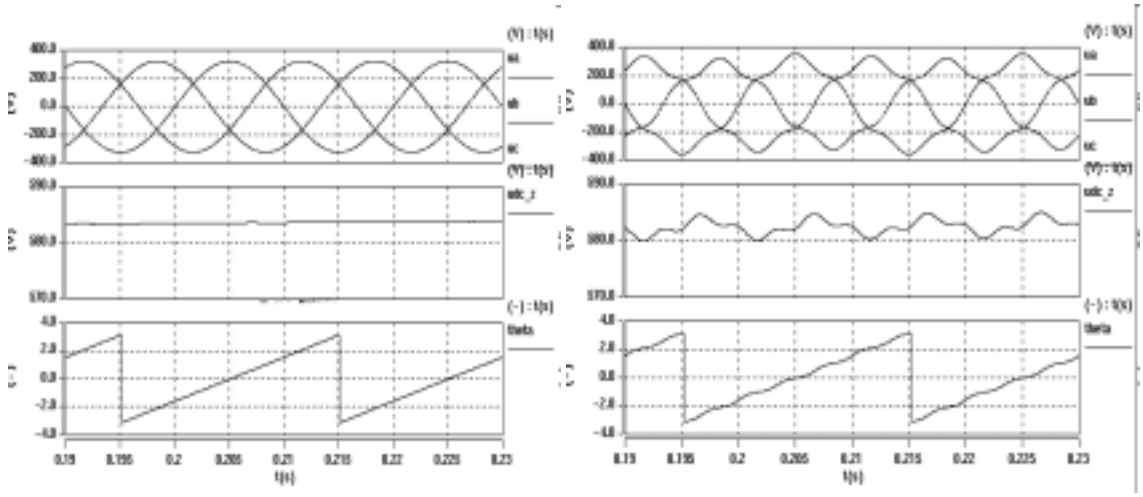


Fig.5.3. Waveforms of basic signals in the *VOC* scheme.
From the top: -line voltages, *DC*-link voltage, reference angle of line voltage.

Figs. 5.4 and 5.5 illustrate the effect of non-ideal line voltage on the current drawn by a rectifier under various control options. Specifically, the total harmonic distortion (*THD*) of the current is shown as a function of the coefficient of imbalance (Fig. 5.4) and magnitude of the 5th harmonic (Fig. 5.5). Again, the *VFOC* and *VF-DPC* strategies display distinct superiority over the *VOC* and *DPC* schemes.

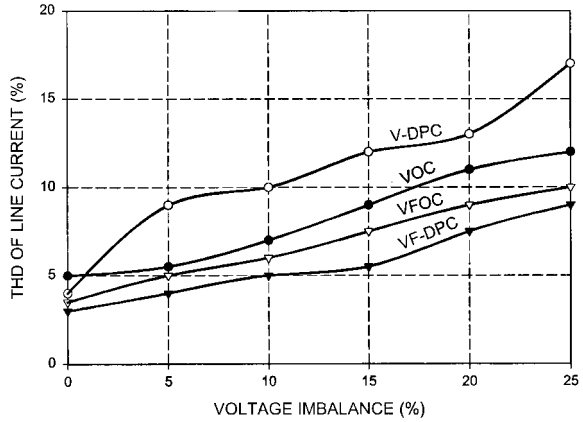


Fig. 5.4. *THD* of the line current as a function of voltage imbalance.

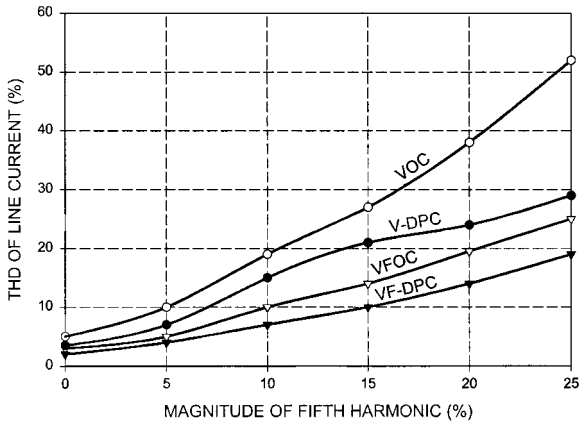


Fig. 5.5.*THD* of the line current as a function of the magnitude of fifth harmonic of the line voltage.

The line current (*THD*) factor for the different control schemes are summarized in Table 5.1 together with the different operating conditions and experimental results.

TABLE 5.1. Simulation and experimental results

Control strategy	Sampling frequency	Switching frequency	THD of line current			
			Sinusoidal voltage		Unbalanced and distorted line voltage	
			Simulation	Experimental	Simulation	Experimental
VOC with SVPWM and AC voltage sensors	5 kHz	5 kHz	4.3 %	6.0 %	9.0 %	11.7 %
VOC with SVPWM	5 kHz	5 kHz	4.5 %	6.1 %	9.2 %	11.8 %
VOC with DPWM	10 kHz	6.66 kHz	2.6 %	3.1 %	8.0 %	10.1 %
VFOC with SVPWM	5 kHz	5 kHz	4.5%	-	8.7 %	10.5%
V-DPC	80 kHz	5 kHz (average)	5.6 %	-	8.9 %	-
VF-DPC	50 kHz	3.5 kHz (average)	5.2 %	-	5.6 %	5.6%

➢ ***Parameter sensitivity***

Figure 5.6 shows the dependence of the line current *THD* on variations of the line inductance. As expected, the *VOC* and *VFOC* techniques are insensitive to these variations, because the line inductance affects only the estimated angular position of the line voltage or virtual flux vectors. Therefore, it influences the input power factor but not the *THD* of the current. To the contrary, in the *DPC* schemes, the line inductance directly affects the estimated active and reactive power values, which in the closed control loop define switching instants and, as a result, the current *THD*. However, the impact of inaccurate line inductance estimation on the performance of a *VF-DPC* rectifier is considerably lower than that of a *DPC* rectifier. This is so because in the former rectifier no line current differentiation is performed (see (3.8) and (3.9)) and the integrator used in flux calculation (see (2.42a) and (2.42b)) displays a low-pass filter behaviour.

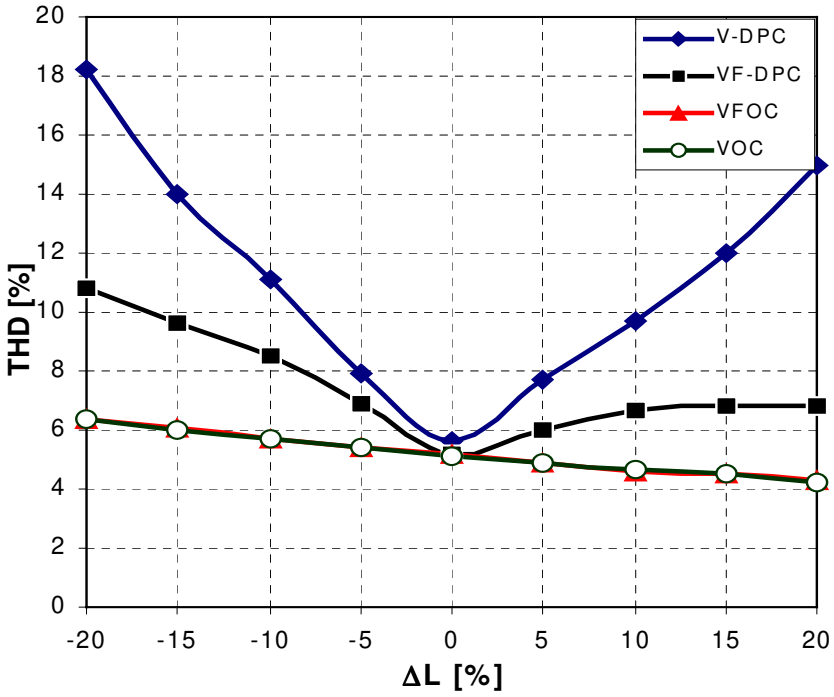


Fig. 5.6 Current *THD* versus error in estimation of the line inductance.

➢ ***Dynamic performance***

A simulated response to a step change in the active power in the virtual-flux based control systems under consideration is shown in Fig. 5.7. As seen in Fig. 5.7a, to reduce the control error, the *VF-DPC* scheme selects directly an appropriate voltage vector, providing very fast power control. Contrastingly, the dynamic response of a *VFOC* rectifier, illustrated in Fig. 5.7b, is determined by the performance of current controllers. With PI controllers, the rectifier's reaction is slower than that with hysteresis controllers.

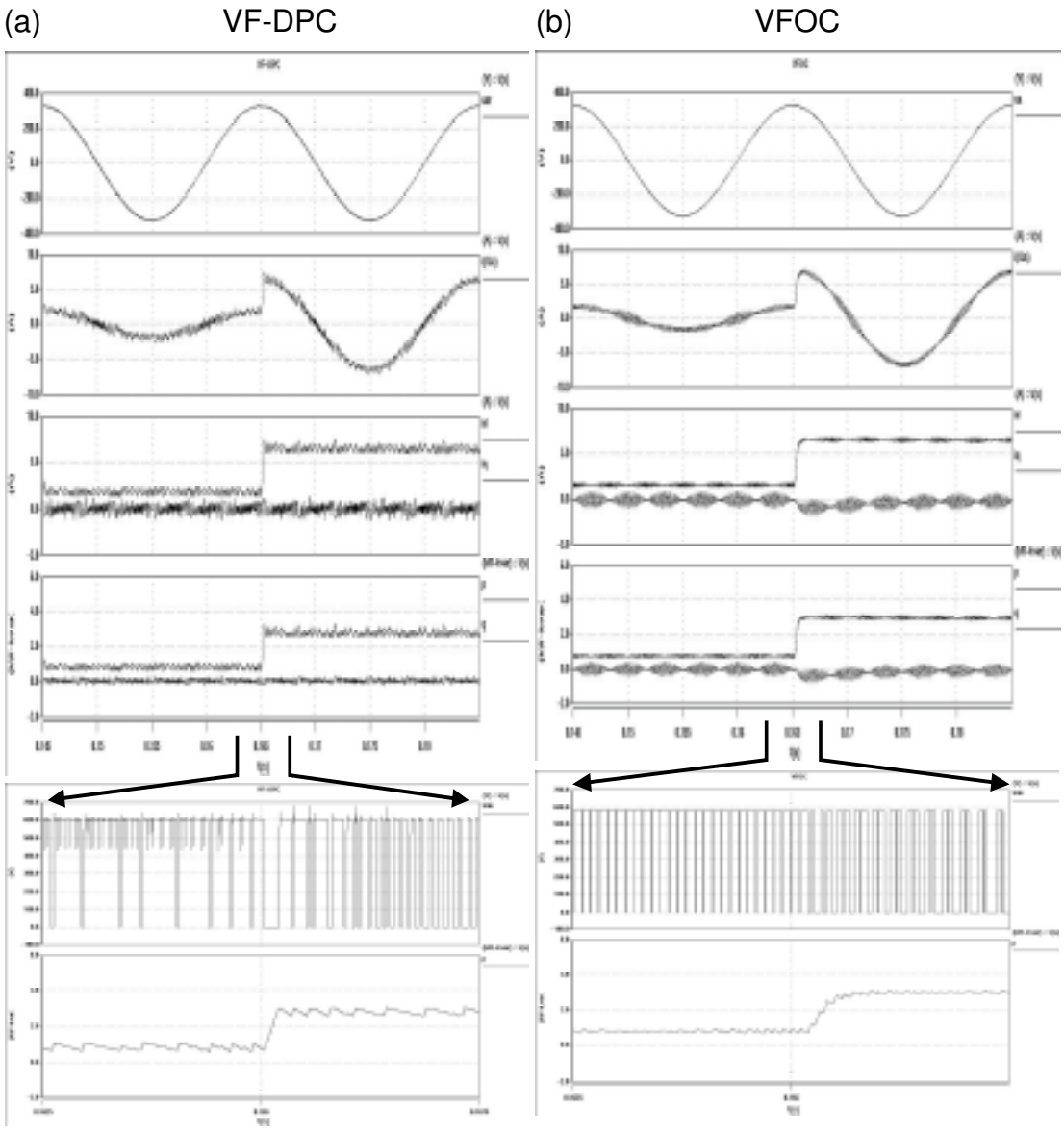


Fig. 5.7 Response of the *VF-DPC* and the *VFOC* rectifiers to a step change in active power. From the top: line voltage u_a, line current i_a, i_{Ld} current, i_{Lq} current, instantaneous active power p, instantaneous reactive power q, line to line voltage u_{ab} and instantaneous active power p.

5.3. SUMMARY

Advantages and disadvantages of the control schemes compared are listed in Table 5.2. Taking into account all operational features, the *VF-DPC* technique seems to be the most advantageous of all.

TABLE 5.2: Advantages and disadvantages of control techniques for PWM rectifiers

TECHNIQUE	ADVANTAGES	DISADVANTAGES
VOC	• Fixed switching frequency (easier design of the EMI input filter) • Advanced PWM strategies can be used • Cheaper A/D converters • No sensitivity for inductance variation	• Coordinate transformation and decoupling between active and reactive current is required • Complex algorithm • Input power factor lower than that for DPC
DPC	• No separate voltage modulation block • No current regulation loops • No coordinate transformation • Good dynamics • Simple algorithm • Decoupled active and reactive power control • Instantaneous variables with all harmonic components are estimated (improvement of the power factor and efficiency)	• Variable switching frequency • High values of the inductance and sampling frequency are needed (important point for the estimator, because smooth shape of the current waveform is required) • Power and voltage estimation should be avoided at the moment of switching (it yields high errors) • Fast microprocessor and A/D converters required
VFOC	• Fixed switching frequency • Advanced PWM strategies can be used. • Cheaper A/D converters • No sensitivity for inductance variation	• Coordinate transformation and decoupling between active and reactive components is required • Complex algorithm • Input power factor lower than that for DPC
VF-DPC	• Simple and noise-resistant power estimation algorithm, easy to implement in a DSP • Lower sampling frequency than that for DPC • Low THD of line currents at a distorted and unbalanced line voltage (sinusoidal line currents) • No separate voltage modulation block • No current regulation loops • No coordinate transformation • Good dynamics • Simple algorithm • Decoupled active and reactive power control	• Variable switching frequency • Fast microprocessor and A/D converters required

6. CONCLUSION

The theses formulated in the Chapter 1 has been proved by simulation and experimental investigation. It was shown that application of virtual flux (*VF*) based control yields lower current distortion for both the Voltage Oriented Control (VOC) and Direct Power Control (DPC) scheme (see Fig. 5.5 and 5.6). Also, the *VF* estimation is much less noisy than that of the line voltage (see Fig 3.21). Moreover, a line voltage or virtual flux estimator can replace AC-line voltage sensors without deterioration in protection and performance of PWM rectifiers. Therefore, taking into account all operational features (see Table 5.2), the Virtual Flux Based Direct Power Control (VF-DPC) technique seems to be the most advantageous of all. Other most important results of the work can be summarized as below:

VF-DPC versus DPC

- lower sampling frequency,
- simple and noise robust power estimation algorithm,
- sinusoidal line currents (low THD) even under unbalanced and distorted line voltage,

VF-DPC versus VOC and VFOC

- simpler algorithm,
- no current control loops,
- coordinate transformation and PI controllers are not required,
- no separate PWM voltage modulation block,
- decoupled active and reactive power controls,
- sinusoidal line currents (low THD) even under unbalanced and distorted line voltage,
- good dynamic performance,
- power estimation gives possibility of obtaining instantaneous variables with all harmonic components, which have an impact on improvement of the total power factor and efficiency.

Additionally, it has been shown that for implementation of VOC and VFOC schemes, one of the most important blocks is the voltage modulator. Therefore, special attention was paid to various PWM techniques. As result the new concept of Adaptive Space Vector Modulation (ASVM) was developed. Investigation shows that ASVM is a universal solution for three-phase PWM converters. Among its main features are: full control range including overmodulation and six-step operation, tracking of peak current for instantaneous selection of two-phase PWM (this guarantees maximal reduction of switching losses up to 50%), good dynamic performance by the switching table application. ASVM with simplified switching time calculation provide a time efficient algorithm based on implementation in Cartesian coordinates. It consumes one third of the time required by it's counterpart in polar coordinates.

Appendices

A.1 PER UNIT NOTIFICATION

$Z_B = \frac{U_{LL}^2}{S_{nom}}$; $\qquad Z_{PU} = \frac{Z_{50Hz}}{Z_B}$
U_{LL} - Input line-line rms voltage (U_{ab} = *1 per unit*) S_{nom} - Fundamental apparent input power (S_1 = *1 per unit)* Z_B - Base impedance (S_1 = *1 per unit (100%))*

The voltage unbalance is defined as: $u = \frac{e_n}{e_p}$
e_p - positive sequence of input voltage vector e_n - negative sequence of input voltage vector

A.2 HARMONIC DISTORTION IN POWER SYSTEM

The specification of power system harmonic, conventional and instantaneous power theories will be reviewed under ideal and distorted conditions. A waveform is distorted when a voltage or current in power system contains other frequencies than the fundamental frequency of the mains. The distorting components of waveforms under steady state conditions are usually integer multiples of the fundamental power frequency.

Specification of power system distortion
When the periodical function performs a Dirichlet conditions (the conditions are performed almost by all real electrical signals) then it can be represented as an infinite concurrent Fourier series. The sum of this series is equal *f(x)* function

$$f(x) = \frac{a_0}{2} + \sum_{n=1}^{\infty} F_n \sin(nx + \psi_n) \qquad \text{(A.2.1a)}$$

or

$$f(\omega_s t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} F_n \sin(n\omega_s t + \psi_n) \qquad \text{(A.2.1b)}$$

where:
F_n- trigonometric Fourier series coefficient with physical meaning of *n* harmonic amplitude
$a_0/2$ – average component
$F_1 \sin(\omega_s t + \psi_1)$ – fundamental harmonic
$F_n \sin(n\omega_s t + \psi_n)$ – harmonic of *n* order
ψ_n – initial phase of n order harmonic

$\omega_s = 2\pi/T_s = \omega_1$
T_s – period

If we describe:

$$F_n \sin(n\omega_s t + \psi_n) = F_n(\sin n\omega_s t \cos\psi_n + \cos n\omega_s t \sin\psi_n) \qquad \text{(A.2.2)}$$

and with notation (Fig. A.2.1)

$$F_n \sin\psi_n = b_n,\ F_n \cos\psi_n = a_n \qquad \text{(A.2.3)}$$

and

$$tg\psi_n = \frac{b_n}{a_n},\ F_n = \sqrt{a_n^2 + b_n^2} \qquad \text{(A.2.4)}$$

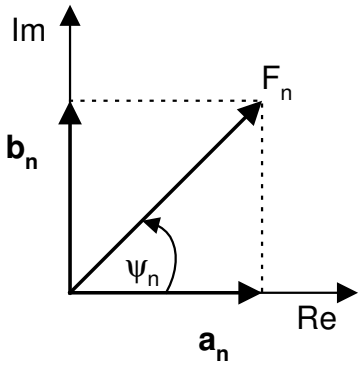


Fig. A.2.1 F_n decomposition into a_n and b_n

with this consideration the series can be represented as

$$f(\omega_s t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos n\omega_s t + \sum_{n=1}^{\infty} b_n \sin n\omega_s t \qquad \text{(A.2.5)}$$

or

$$f(\omega_s t) = \frac{a_0}{2} + \sum_{n=1}^{\infty}\left(a_n \cos\left(\frac{2\pi nt}{T_s}\right) + b_n \sin\left(\frac{2\pi nt}{T_s}\right)\right) \qquad \text{(A.2.6)}$$

The coefficient a_0 represents the average value of *f(x)* and the coefficients a_n and b_n represents the orthogonal components of the *n*th harmonic. The coefficients are determined as follows:

$$a_0 = \frac{2}{T_s}\int_0^{T_s} f(\omega_s t)dt \qquad \text{(A.2.7a)}$$

$$a_n = \frac{2}{T_s}\int_0^{T_s} f(\omega_s t)\cos n\omega_s t dt = \frac{2}{T_s}\int_0^{T_s} f(\omega_s t)\cos\left(\frac{2\pi nt}{T_s}\right)dt \qquad \text{(A.2.7b)}$$

$$b_n = \frac{2}{T_s}\int_0^{T_s} f(\omega_s t)\sin n\omega_s t dt = \frac{2}{T_s}\int_0^{T_s} f(\omega_s t)\sin\left(\frac{2\pi nt}{T_s}\right)dt \qquad \text{(A.2.7c)}$$

Most of periodical signals perform some of symmetry conditions. Elements of Fourier series disappear in this case.

- Symmetry to abscissa axis

Area over and under axis are equal. It means that $a_0 = 0$ and expansion of Fourier series will be an infinity series about uneven harmonics.

- Symmetry to ordinate axis

Sinus expression disappears from Fourier series because sinus function is uneven.

- Symmetry to beginning of coordinate system

The function is uneven. Therefore $a_0 = 0$ and cosinus expression disappears from Fourier series, because cosinus function is even.

When symmetry to abscissa axis and symmetry to beginning of coordinate system occur, the Fourier series will have only uneven expression with sinus. Therefore, we can describe:

$$f(\omega_s t) = \sum_{n=1,3,5...}^{\infty} b_n \sin n\omega_s t \tag{A.2.8}$$

Conventional decomposition of voltage, currents and powers

According to the above description periodical signal of voltage, current and power can be represented as Fourier series

$$u(t) = \sum_{n=0}^{\infty} \sqrt{2} U_n \sin(\omega_n t + \psi_n) \tag{A.2.9}$$

$$i(t) = \sum_{n=0}^{\infty} \sqrt{2} I_n \sin(\omega_n t + \psi_n - \varphi_n) \tag{A.2.10}$$

where $\varphi_n = \angle(U_n, I_n)$ - phase angle between *n-th* voltage and current harmonics

$\omega_n = n\omega_1$; ω_n is the angular frequency of the *n*th harmonic

$$\omega_n = 2\pi n f_1 = \frac{2\pi n}{T_1} \tag{A.2.11}$$

U_n and I_n are the rms (root mean square) value of the *n*th harmonic voltage and current respectively:

$$X_n = \sqrt{\frac{1}{T}\int_0^T x_n^2(t)dt} \tag{A.2.12}$$

based on Parseval theorem the rms value of the distorted voltage and current is given by:

$$U_{rms} = \sqrt{\frac{1}{T}\int_0^T u(t)^2 dt} = \sqrt{\sum_0^{\infty} U_n^2} = \sqrt{U_0^2 + U_1^2 + U_2^2 + ...} \tag{A.2.13}$$

$$I_{rms} = \sqrt{\frac{1}{T}\int_0^T i(t)^2\,dt} = \sqrt{\sum_0^\infty I_n^2} = \sqrt{I_0^2 + I_1^2 + I_2^2 + \ldots} \qquad \text{(A.2.14)}$$

The total harmonic distortion factor (*THD*) is most commonly used to characterize the magnitude of the distorted signals. The *THD* gives the ratio between the geometric sum of the magnitudes or rms of the harmonics and the magnitude (or rms value) of the fundamental component:

$$THD = \frac{\sqrt{\sum_{n=2}^\infty X_n^2}}{X_1}. \qquad \text{(A.2.15)}$$

The main disadvantage of the *THD* is that the detailed information about harmonic spectrum is lost.

The instantaneous power is defined as:

$$p(t) = u(t)\, i(t) \qquad \text{(A.2.16)}$$

Classical approaches define that active power is an average value of instantaneous power

$$P = \frac{1}{T}\int_0^T p(t)dt = \frac{1}{T}\int_0^T u(t)\cdot i(t)dt = \sum_{n=0}^\infty P_n = U_0 I_0 + \sum_{n=1}^\infty U_n I_n \cos\gamma_n$$
$$S = U_{rms}\cdot I_{rms} = \sqrt{\frac{1}{T}\int_0^T u(t)^2\,dt}\sqrt{\frac{1}{T}\int_0^T i(t)^2 dt} = \sqrt{\sum_{n=0}^\infty U_n^2 \sum_{n=0}^\infty I_n^2} \qquad \text{(A.2.17)}$$
$$Q = \sqrt{S^2 - P^2}$$

For a typical three-phase system without neutral wire, $U_0 I_0$ will be zero since a zero sequence components of the current system do not exists. Therefore, the equations (A.2.17) posses only *AC* components:

$$P = \sum_{n=1}^\infty P_n = \sum_{n=1}^\infty U_n I_n \cos\gamma_n \qquad \text{(A.2.18)}$$

$$S = \sqrt{\sum_{n=1}^\infty U_n^2 \sum_{n=1}^\infty I_n^2} \qquad \text{(A.2.19)}$$

$$Q = \sum_{n=1}^\infty Q_n = \sum_{n=1}^\infty U_n I_n \sin\gamma_n \qquad \text{(A.2.20)}$$

Where the active power *P* will thus represent a measure of the average energy flow even in a disturbed power system. The apparent power *S* is usually used to specify the size of required power system equipment. The apparent power *S* is considered as representing the maximum active power, which can be delivered by a voltage source while the line losses are maintained constant. The reactive power *Q* is of interest for specifying the

size of compensation equipment in power system such as PWM converters and active power filters.

From the comparison of Eqs. (A.2.18), (A.2.20) with (A.2.19) can be seen that as distinct from sinusoidal signals the square sum of active and reactive power is not equal to apparent power. Therefore, to complete the definitions a "distortion power" *D* has been introduced (Fig. A.2.2). The separate power are connected in equation

$$D = \sqrt{S^2 - P^2 - Q^2} \tag{A.2.21}$$

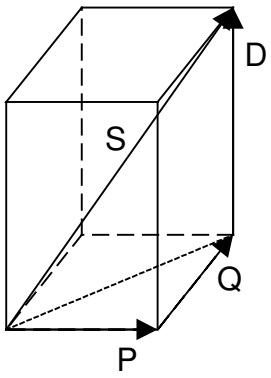


Fig. A.2.2 Graphical representation of power components

Instantaneous decomposition of powers

Many theories of instantaneous power exist in scientific literature [8-10,13-15] and it is in detail described in [7,11-12]. The extension of the reactive power to non-sinusoidal waveforms is now a subject of controversy. Many new theories have been proposed and they are not accepted for all researchers around the world. However, the definition of this topic is still confusing and it is difficult to find a general and unified definition of power components under non-sinusoidal conditions, particularly when three-phase systems are analyzed. The most popular definition for instantaneous reactive (imaginary) and active (real) power has been proposed by Takahashi and by Akagi [8,9,13]. However, the instantaneous imaginary power proposed by Akagi does not have a clear physical meaning.

Furuhashi presents a new definition of instantaneous reactive power [13], which is generated by compensating equipment such as an active filter. In author opinion most clear presentation of instantaneous components of active and reactive power was presented by Peng [14].

Instantaneous power for three-phase system are usually considered in orthogonal coordinates α-β-*0* then in three phase coordinate *a*-*b*-*c*. Therefore, the Clarke transformation $\underline{C}$ and its reverse transformation $\underline{C}^{-1}$ define the relationship between the three-phase system *a*-*b*-*c* and the stationary reference frame α-β-*0* are described as:

$$\begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{A.2.22a}$$

where x denotes currents or voltages

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & 1/\sqrt{2} \\ -1/2 & \sqrt{3}/2 & 1/\sqrt{2} \\ -1/2 & -\sqrt{3}/2 & 1/\sqrt{2} \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} \qquad \text{(A.2.22b)}$$

The α-β components can be represented in the Cartesian plane by a space vector $\underline{x}_{\alpha\beta}$:

$$\underline{x}_{\alpha\beta} = x_\alpha + jx_\beta \qquad \text{(A.2.23)}$$

where the α-axis and the a-axis have the same orientation. The β-axis leads the a-axis with 90^0.
For a three-phase power system, instantaneous voltages u_a, u_b, u_c and instantaneous currents i_a, i_b, i_c are expressed as instantaneous space vectors $\underline{u}$ and $\underline{i}$

$$\underline{u} = \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \quad \text{and} \quad \underline{i} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \qquad \text{(A.2.24)}$$

For three-phase voltages and currents u_a, u_b, u_c and i_a, i_b, i_c the α, β and 0 components are expressed as:

$$\begin{bmatrix} u_\alpha \\ u_\beta \\ u_0 \end{bmatrix} = [C] \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \quad \text{and} \quad \begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = [C] \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \qquad \text{(A.2.25)}$$

For the typical three-phase system without neutral wire, zero sequence component i_0 of the current system does not exist $(i_a + i_b + i_c = 0)$. It gives finally simple realization of signal processing thanks to only two signals in α-β coordinate what is the main advantage of $abc/\alpha\beta$ transformation. With this assumption the equations (A.2.25) can be described as:

$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \qquad \text{(A.2.26)}$$

and

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \qquad \text{(A.2.27)}$$

General three-phase four-wire system is represented as separated: three-phase three-wire system and a single-phase system, which represents the zero sequence components.

$$p_{\Sigma} = \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix}^T \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} u_\alpha \\ u_\beta \\ u_0 \end{bmatrix}^T \begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = p(t) + p_0(t) \tag{A.2.28}$$

The instantaneous zero sequence power $p_0(t)$ is only observable if exist both zero sequence components (u_0, i_0).

$$p_0(t) = v_0 \cdot i_0 \tag{A.2.29}$$

The Takahashi define the instantaneous active power p as *scalar product* between the three-phase voltages and currents and instantaneous reactive power q as *vector product* between them:

$$p = \underline{u}_{(abc)} \cdot \underline{i}_{(abc)} = u_a i_a + u_b i_b + u_c i_c \tag{A.2.30}$$

$$q = \underline{u}_{(abc)} \times \underline{i}_{(abc)} = u_a^{'} i_a + u_b^{'} i_b + u_c^{'} i_c \tag{A.2.31}$$

where $u_a^{'}$, $u_b^{'}$, $u_c^{'}$ is 90^0 lag of u_a, u_b, u_c respectively. The same equations can be described in matrix form as:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} u_a & u_b & u_c \\ u_a^{'} & u_b^{'} & u_c^{'} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}, \tag{A.2.32}$$

where

$$\begin{bmatrix} u_a^{'} \\ u_b^{'} \\ u_c^{'} \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} u_c - u_b \\ u_a - u_c \\ u_b - u_a \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} u_{ca} \\ u_{ac} \\ u_{ba} \end{bmatrix}. \tag{A.2.33}$$

Additional information can be obtained by defining an instantaneous complex power $\underline{p}(t)$ in the Cartesian plane:

$$\begin{aligned} \underline{p}(t) &= \underline{u}(t) \cdot \underline{i}(t)^* = \mathrm{Re}\{\underline{p}(t)\} + \mathrm{Im}\{\underline{p}(t)\} = p(t) + jq(t) = \\ &= u_a i_a + u_b i_b + u_c i_c + j\frac{1}{\sqrt{3}}[(u_b - u_c)i_a + (u_c - u_a)i_b + (u_a - u_b)i_c] \end{aligned} \tag{A.2.34}$$

The most frequently referred power theory was proposed by Akagi [9] when the three-phase voltages and currents are transformed into α-β coordinates, and additionally the three-phase voltages and currents excluding zero-phase sequence components. Therefore, instantaneous power on the three-phase circuit can be defined as follows:

$$p = \underline{u}_\alpha \underline{i}_\alpha + \underline{u}_\beta \underline{i}_\beta \tag{A.2.37}$$

where p is equal to the conventional equation (A.2.30). In order to define the instantaneous reactive power, Akagi introduced the instantaneous imaginary power space vector defined by:

$$\underline{q} = \underline{u}_\alpha \times \underline{i}_\beta + \underline{u}_\beta \times \underline{i}_\alpha \tag{A.2.38}$$

(imaginary axis vector is perpendicular to the real plane on the α-β coordinates)
From equation (A.2.37) the conventional instantaneous power p and the above defined instantaneous imaginary power q, which is the amplitude of space vector $\underline{q}$ are expressed by:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} u_\alpha & u_\beta \\ -u_\beta & u_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{A.2.39}$$

$u_\alpha i_\alpha$ and $u_\beta i_\beta$ obviously mean instantaneous power because they are defined by product of the instantaneous voltage in one axis and the instantaneous current in the same axis. Therefore, p is the real power in the three-phase circuit and its dimension is [W]. Conversely, $u_\alpha i_\beta$ and $u_\beta i_\alpha$ are not instantaneous power, because they are defined by the product of the instantaneous voltage in one axis and instantaneous current not in the same axis but in the perpendicular axis.
The α-β currents can be obtained by the equations inverse to (A.2.39):

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} u_\alpha & u_\beta \\ -u_\beta & u_\alpha \end{bmatrix}^{-1} \begin{bmatrix} p \\ q \end{bmatrix} \tag{A.2.40}$$

and gives finally

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{u_\alpha^2 + u_\beta^2} \begin{bmatrix} u_\alpha & -u_\beta \\ u_\beta & u_\alpha \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix} \tag{A.2.41}$$

The theory proposed by Peng [14] base on equations (A.2.30), (A.2.31) and defines vector $\underline{q}$ designated as the instantaneous reactive (or nonactive) power vector of the three-phase circuit. The magnitude (or the length) of $\underline{q}$ is designated as the instantaneous reactive power that is

$$\mathbf{q} = \begin{bmatrix} q_a \\ q_b \\ q_c \end{bmatrix} = \begin{bmatrix} \begin{vmatrix} u_b & u_c \\ i_b & i_c \end{vmatrix} \\ \begin{vmatrix} u_c & u_a \\ i_c & i_a \end{vmatrix} \\ \begin{vmatrix} u_a & u_b \\ i_a & i_b \end{vmatrix} \end{bmatrix} \tag{A.2.43}$$

and

$$q = \left|\underline{q}\right| = \sqrt{q_a^2 + q_b^2 + q_c^2} \tag{A.2.44}$$

Next the instantaneous active current vector $\underline{i}_p$, the instantaneous reactive current vector $\underline{i}_q$, the instantaneous apparent power s and the instantaneous power factor λ are defined as:

$$\underline{i}_p = \begin{bmatrix} i_{ap} \\ i_{bp} \\ i_{cp} \end{bmatrix} \overset{def}{=} \frac{p}{\underline{u} \cdot \underline{u}} \underline{u} \tag{A.2.45}$$

$$\underline{i}_q = \begin{bmatrix} i_{aq} \\ i_{bq} \\ i_{cq} \end{bmatrix} \overset{def}{=} \frac{\underline{q} \times \underline{u}}{\underline{u} \cdot \underline{u}} \tag{A.2.46}$$

$$s \overset{def}{=} ui \qquad \text{and} \qquad \lambda \overset{def}{=} \frac{p}{s} \tag{A.2.47}$$

where

$$u = |\underline{u}| = \sqrt{u_a^2 + u_b^2 + u_c^2} \quad \text{and} \quad i = |\underline{i}| = \sqrt{i_a^2 + i_b^2 + i_c^2} \tag{A.2.48}$$

are the instantaneous magnitudes (or norms) of the three-phase voltage and current, respectively.

Moreover, following interesting properties can be observed:

- a three-phase current vector $\underline{i}$ is always equal to the sum of $\underline{i}_p$ and $\underline{i}_q$ i.e. $\underline{i} \equiv \underline{i}_p + \underline{i}_q$
- $\underline{i}_q$ is orthogonal to $\underline{u}$, and $\underline{i}_p$ parallel to $\underline{u}$ namely $\underline{u} \cdot \underline{i}_q \equiv 0$ and $\underline{u} \times \underline{i}_p \equiv 0$
- all properties of the conventional reactive power theory still hold true for new theory such as: $i^2 \equiv i_p^2 + i_q^2$, $s^2 \equiv p^2 + q^2$, and $i^2 \equiv (p^2 + q^2)/u^2$, where $i_p = |\underline{i}_p|$ and $i_q = |\underline{i}_q|$
- for a three-phase system without zero sequence voltage and current i.e. $u_a + u_b + u_c = 0$ and $i_a + i_b + i_c = 0$, it is true that:
  $q = q_a = q_b = q_c = u_b i_c - u_c i_b = u_c i_a - u_a i_c = u_a i_b - u_b i_a$
  $p = 2(u_a i_a + u_b i_b) + u_a i_b + u_b i_a = 2(u_b i_b + u_c i_c) + u_b i_c + u_c i_b = 2(u_c i_c + u_a i_a) + u_c i_a + u_a i_c$

The definitions of the instantaneous reactive components are all based on the direct quantities of three-phase voltages and currents. If necessary these newly defined quantities can be expressed in any other coordinates.

$$p = \underline{u}_{(abc)} \cdot \underline{i}_{(abc)} = \underline{u}_{(\alpha\beta 0)} \cdot \underline{i}_{(\alpha\beta 0)} \tag{A.2.49}$$

$$\underline{q}_{(abc)} = \begin{bmatrix} q_a & q_b & q_c \end{bmatrix}^T = \underline{u}_{(abc)} \times \underline{i}_{(abc)} = \underline{u}_{(\alpha\beta 0)} \times \underline{i}_{(\alpha\beta 0)} \tag{A.2.50}$$

After $\alpha\beta$ transformation all equations proposed by Peng are identical to definition described in [9].

Other popular theory was proposed by Furuhashi [13], especially, for active filters because the new instantaneous reactive power q_k is defined with the power of each line of the active filter (active filter does not generate the instantaneous active power) as:

$$q_k = u_k * i_{Fk} \qquad (k = 1,2,...,n) \tag{A.2.51}$$

where u_k – phase voltage i_{Fk} – phase current of active filter.

Since the active filter does not generate the instantaneous active power, the following constraint is imposed on the power in (A.2.51):

$$\sum_{k=1}^{n} q_k = 0 \qquad \text{(A.2.52)}$$

All of researchers only agree with definition that the instantaneous active and reactive power „*p*" and „*q*" can be decomposed into average DC components $\overline{q}, \overline{p}$ corresponding to the fundamental of the load current and an oscillating (ripple) components $\widetilde{q}, \widetilde{p}$ corresponding to the harmonics:

$$p_{3-phase} = p + q = \overline{p} + \widetilde{p} + \overline{q} + \widetilde{q} \qquad \text{(A.2.53)}$$

$$p = \overline{p} + \widetilde{p} \quad \text{and} \quad q = \overline{q} + \widetilde{q} \qquad \text{(A.2.54)}$$

where:

$p_{3-phase}$ -total three-phase instantaneous power demanded by the load

p-instantaneous active components of $p_{3-phase}$

q- instantaneous reactive components of $p_{3-phase}$

$\overline{p}$ - direct (average) components of *p* associated to the fundamental frequency active components of load current

$\widetilde{p}$ - alternating (ripple) components of *p* associated to the harmonic active components of load current

$\overline{q}$ - direct (average) components of *q* associated to the fundamental frequency reactive components of load current

$\widetilde{q}$ - alternating (ripple) components of *q* associated to the harmonic reactive components of load current

Only in the Peng's definition $\widetilde{p}$ and $\widetilde{q}$ can additionally be split into two parts (2ω components and harmonic components) as

$$\widetilde{p} = p_{2\omega} + p_h \qquad \text{(A.2.55)}$$

$$\widetilde{q} = q_{2\omega} + q_h \qquad \text{(A.2.56)}$$

where $p_{2\omega}$ and $q_{2\omega}$ are the negative-sequence active and reactive power (2ω components) originating from asymmetrical fundamental (negative sequence) components of the load current, and p_h and q_h are the harmonic active and reactive power (harmonic components) originating from harmonic components of load current.

A.3 IMPLEMENTATION OF SVM

Simplified switching time calculation for SVM

This point presents an approach, which allows simplified calculations and the algorithm in real time implementation is much faster, compare to the conventional method. The new algorithm is based on the assumption, that the conduction times in each phase are calculated directly using only information about command phase voltages. In classical

SVM techniques the polar coordinate system is used to calculate these times, whereas in presented method the Cartesian coordinate system is used.
The description is based on the simple equations [101]. It is easy to show that the average values of output voltages with respect to neutral point of converter (Fig. 4.7) are calculated as:

$$u_{a0} = \frac{U_{dc}}{T_s} \cdot T_a - \frac{U_{dc}}{2},\ u_{b0} = \frac{U_{dc}}{T_s} - \frac{U_{dc}}{2} \cdot T_b,\ u_{c0} = \frac{U_{dc}}{T_s} \cdot T_c - \frac{U_{dc}}{2} \tag{A.3.1}$$

where T_a, T_b, T_c are the conduction times in each phase of the converter.
Note, that in balanced system, the neutral point voltage is expressed as:

$$u_{N0} = \frac{1}{3} \cdot \frac{U_{dc}}{T_s}(T_a + T_b + T_c) - \frac{U_{dc}}{2} \tag{A.3.2}$$

After simple calculations we can obtain the relationship between phase voltages and conduction times in the form:

$$\begin{bmatrix} u_{aN} \\ u_{bN} \\ u_{cN} \end{bmatrix} == \frac{1}{3} \cdot \frac{U_{dc}}{T_s} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} T_a \\ T_b \\ T_c \end{bmatrix} \tag{A.3.3}$$

Note, that the matrix used in the above equation is singular, and that is no unique solution, if we want to calculate conduction times from phase voltages. This one degree of freedom gives us possibility to construct different modulation methods. The only limitation is that all these times should be in the range $[0, T_s]$. It is easy to conclude that lower voltage gives lower conduction time. So, the minimum time is for the minimum voltage (Fig. A.3.1a).

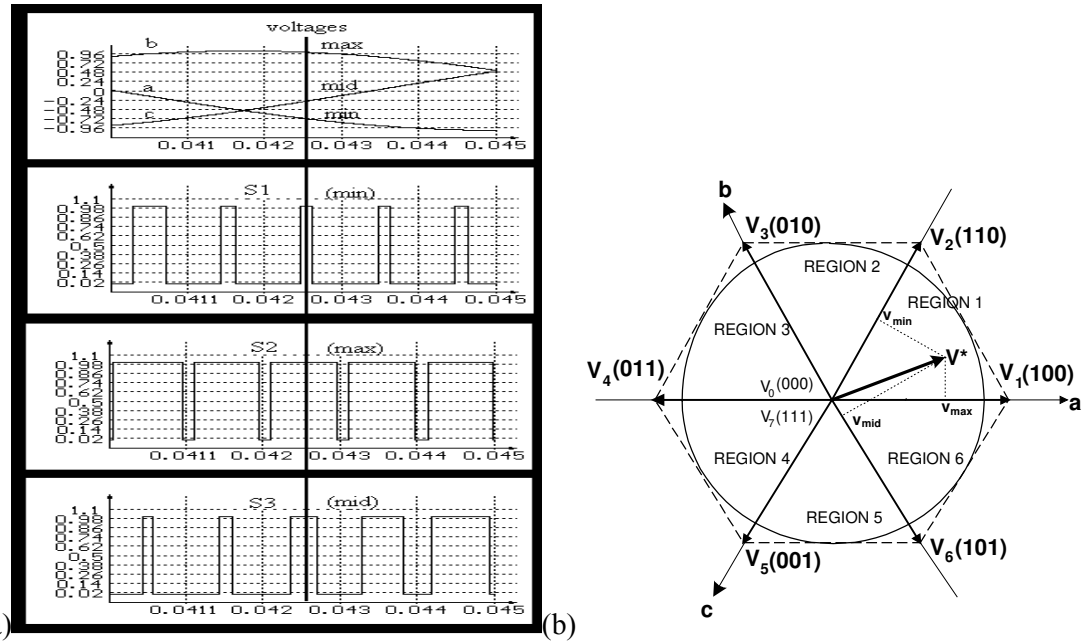


Fig. A.3.1 a) Correspondence between phase voltages and conduction times.
From the top: phase voltages and pulses.
b) Space vector representation of three-phase converter in natural *a, b, c* coordinate.

If we introduce the following notation (Fig. A.3.1b):

$$u_{min} = min(u_{ao}, u_{bo}, u_{co}),$$
$$u_{max} = max(u_{ao}, u_{bo}, u_{co}),$$
$$u_{min} < u_{mid} < u_{max}.$$

and assume that T_{min}, T_{mid}, T_{max}, are the conduction times in phases for which the voltages are u_{min}, u_{mid}, u_{max} respectively. The minimum value, which can be taken for T_{min}, is zero. In this case we can calculate another conduction times using equation:

$$\begin{bmatrix} T_{\max} \\ T_{mid} \\ T_{\min} \end{bmatrix} = \frac{T_s}{U_{dc}} \begin{bmatrix} u_{\max} - u_{\min} \\ u_{mid} - u_{\min} \\ 0 \end{bmatrix} \tag{A.3.4}$$

If we rewrite this formula with phase indexes we can obtain the following equivalent form:

$$\begin{bmatrix} T_a \\ T_b \\ T_c \end{bmatrix} = \frac{T_s}{U_{dc}} \begin{bmatrix} u_{aN} - u_{\min} \\ u_{bN} - u_{\min} \\ u_{cN} - u_{\min} \end{bmatrix} \tag{A.3.5}$$

The algorithm using the above equation is the discontinues modulation algorithm, and each phase in the period 120° is not switched. Generally any modulation algorithm can be described by the equation:

$$\begin{bmatrix} T_a \\ T_b \\ T_c \end{bmatrix} = \frac{T_s}{U_{dc}} \begin{bmatrix} u_{aN} - u_{\min} \\ u_{bN} - u_{\min} \\ u_{cN} - u_{\min} \end{bmatrix} + k \begin{bmatrix} T_0 \\ T_0 \\ T_0 \end{bmatrix} \tag{A.3.6}$$

where

$$T_0 = T_s - \frac{T_s}{U_{dc}}(u_{\max} - u_{\min}) \tag{A.3.7}$$

and $0 \le k \le 1$. Note, that for $k = 0.5$, the algorithm correspond to the modulation with symmetrical zero states (*SVPWM*).

Adaptive Modulation with simplified switching time calculation

The new idea of *ASVM* [93] bases on assumption that modulator should provide maximal reduction of switching losses in linear range of modulation [see Section 4.4.7]. Therefore, modulator use $k = 0.5$ for low values of modulation index, what gives good performance at start-up condition and, moreover, guarantees low current harmonic distortion. In the discontinues modulation method zero vectors could be chosen as $U_0(0,0,0)$ or $U_7(1,1,1)$. In the first case in the described algorithm Eqs. A.3.8 $k = 0$ in the second case $k = 1$. The selection, which method is used depends on the following condition:

$$if\ u_{max}+u_{min} < 0\ then\ k = 0\ else\ k = 1 \tag{A.3.8}$$

This algorithm describes the discontinues modulation method without current tracking. If we want take into account the phase values of the current, the algorithm is modified. We must additional made sorting of current values

$$i_{min} = min(i_a,i_b,i_c),$$
$$i_{max} = max(i_a, i_b, i_c),$$
$$i_{min} < i_{mid} < i_{max.}$$

and use instead of algorithm Eq. A.3.8, the adaptive algorithm based on the condition presented below:

$$if\ i_{max}+i_{min} < 0\ then\ k = 0\ else\ k = 1 \qquad \text{(A.3.9)}$$

Dead time compensation

One of the main problems encountered in open-loop *PWM* voltage-source converter is the nonlinear voltage gain caused by the nonideal characteristics of the power converter. The most important nonlinearity is introduced by the necessary *dead time* (T_d) to avoid the shoottrought of the DC-link. In most cases, the compensation techniques are based on an average value theory, the lost volt seconds are averaged over an entire period and added vectorially to the commanded voltage. Regardless of the used method, all *dead time* compensation techniques are based on information of the polarity of the current, hence current detection becomes an important issue. This is particularly important around the zero crossings, where an accurate current measurement is needed to exactly compensate for the *dead-time*. In this case the compensation is added to pulse, before the dead time generation for positive current, and subtracted from the pulse for negative current [71][91]. Simple algorithm of *dead time* compensation is presented below:

$$if\ (0 < i_a < i_{min})\ \{T_a = T_a + T_d/T_s;\}$$
$$if\ (0 > i_a > -i_{min})\ \{T_a = T_a - T_d/T_s;\}$$
$$if\ (0 < i_b < i_{min})\ \{T_b = T_b + T_d/T_s;\}$$
$$if\ (0 > i_b > -i_{min})\ \{T_b = T_b - T_d/T_s;\}$$
$$if\ (0 < i_c < i_{min})\ \{T_c = T_c + T_d/T_s;\}$$
$$if\ (0 > i_c > -i_{min})\ \{T_c = T_c - T_d/T_s;\}$$

A.4 SABER MODEL

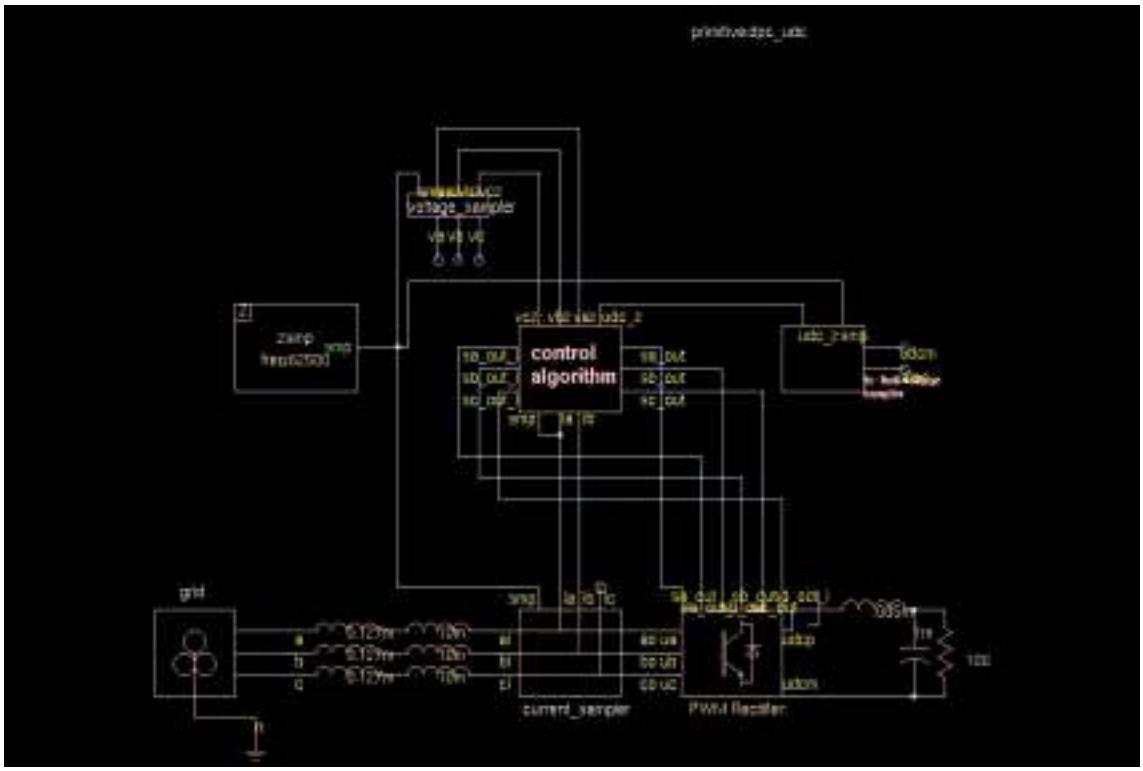


Fig. A.4.1 Example of Saber model

The control algorithms of PWM rectifier was implemented in *SABER*, which provides analysis of the complete behavior of analog and mixed-signal systems, including electrical subsystems. The main electrical parameters of the power circuit and control data are given in the Table A.4.1. The example of PWM rectifier model is shown in Fig. A.4.1. The electrical elements are taken from library, but control algorithm has been written in *MAST* language. The example of *VF-DPC* algorithm implemented in *SABER* is shown below.

Table A.4.1 Parameters used in simulation

Sampling frequency (DPC):	80kHz
Sampling frequency (VF-DPC):	50kHz
Sampling frequency (VOC, VFOC):	5kHz
Resistance of reactors R:	100mΩ
Inductance of reactors L:	10mH
DC-link capacitor:	1mF
Load resistance R_L:	100Ω
Switching frequency (DPC) f:	5kHz
Switching frequency (VF_DPC) f:	3.5kHz
Switching frequency (VOC, VFOC) f:	5kHz
Phase voltage V:	230 RMS
Source voltage frequency:	50 Hz
DC-link voltage:	620V
Resistance of source R:	8mΩ
Inductance of source L:	0.127mH
Inductance per unit notification:	8.7%

```
#*************************************************************************#
#*                        Direct Power Control for Saber - MM                        *#
#*************************************************************************#
element template dpc_udc smp,ia,ib,Sa_out,Sb_out,Sc_out,Sa_out_i,Sb_out_i,Sc_out_i,vaz,vbz,vcz,udc_z

state nu smp,ia,ib,udc_z,vaz,vbz,vcz
state logic_4 Sa_out,Sb_out,Sc_out,Sa_out_i,Sb_out_i,Sc_out_i
{
<consts.sin

state nu ic,ialf,ibet,L=0.013,hh=1,Kp=0.0,Ti=0.0,pi=math_pi,T_in =0.1, Ts=10u
state nu Theta,delta_Udc,p,q,delta_q,delta_p,p_old,q_old, I_ref_old, delta_Udc_old
state nu i,Sq,Sq_old,Sp,Sp_old,sector,udc_ref=610,p_ref,q_ref=0,pdc=1
state nu ui,up,I_ref,ie,Sa,Sb,Sc,Sa_old,Sb_old,Sc_old
state nu Psi_alf,Psi_bet, usa, usb, usc, Psi_alf_s=-1.0, Psi_bet_s=0.0, Psi_alf_c, Psi_bet_c
number  pi_r=0.7,ti_r=5m

state nu tab_11[1:12]=[1, 1, 1, 1, 1, 1, 0, 0, 0, 0, 0, 0]
state nu tab_12[1:12]=[0, 0, 0, 0, 1, 1, 1, 1, 1, 1, 0, 0]
state nu tab_13[1:12]=[1, 1, 0, 0, 0, 0, 0, 0, 1, 1, 1, 1]
state nu tab_21[1:12]=[1, 1, 0, 0, 0, 1, 0, 0, 1, 1, 1, 0]
state nu tab_22[1:12]=[1, 1, 1, 0, 1, 1, 0, 0, 0, 1, 0, 0]
state nu tab_23[1:12]=[0, 1, 0, 0, 1, 1, 1, 0, 1, 1, 0, 0]
state nu tab_31[1:12]=[1, 1, 1, 1, 1, 1, 0, 0, 0, 0, 0, 1]
state nu tab_32[1:12]=[0, 0, 0, 1, 1, 1, 1, 1, 1, 0, 0, 0]
state nu tab_33[1:12]=[1, 0, 0, 0, 0, 0, 0, 1, 1, 1, 1, 1]
state nu tab_41[1:12]=[1, 1, 1, 0, 0, 0, 0, 0, 0, 1, 1, 1]
state nu tab_42[1:12]=[0, 1, 1, 1, 1, 1, 1, 0, 0, 0, 0, 0]
state nu tab_43[1:12]=[0, 0, 0, 0, 0, 1, 1, 1, 1, 1, 1, 0]

when(time_init){
schedule_event(time,Sa_out,l4_0)
schedule_event(time,Sa_out_i,l4_0)
schedule_event(time,Sb_out,l4_0)
schedule_event(time,Sb_out_i,l4_0)
schedule_event(time,Sc_out,l4_0)
schedule_event(time,Sc_out_i,l4_0)
}
when(event_on(smp)){
                                                                    #*Transformacje wspolrzednych
ic=-(ia+ib)                                                         #* "ic" calculation
ialf=ia                                                             #*abc/alfa_beta transformation
ibet=(1/sqrt(3))*(ia+2*ib)

                                                                    #*Virtual flux estimation
usa=1.0/3.0*udc_z*(2.0*Sa_old-Sb_old-Sc_old);
usb=1.0/3.0*udc_z*(-Sa_old+2.0*Sb_old-Sc_old);
usc=1.0/3.0*udc_z*(-Sa_old-Sb_old+2.0*Sc_old);
Ualf=usa;
Ubet=(1/sqrt(3))*(usa+2.0*usb);

Psi_alf_c=Psi_alf_s+Ts*(Ualf-(1/T_in)*Psi_alf_c)
Psi_alf_s=Psi_alf_c
Psi_alf=Psi_alf_c+ialf*L

Psi_bet_c=Psi_bet_s+Ts*(Ubet-(1/T_in)*Psi_bet_c)
Psi_bet_s=Psi_bet_c
Psi_bet=Psi_bet_c+ibet*L
                                                                    #*Instantaneous power estimation
p= 3/2*314*(Psi_alf*ibet - Psi_bet*ialf)
q= 314*(Psi_alf*ialf + Psi_bet*ibet)

if(Psi_alf<0 & Psi_bet>0) Theta = atan(Psi_bet/( Psi_alf+0.000001p))+math_pi
        else if(Psi_alf<0 & Psi_bet< 0) Theta = atan(Psi_bet/( Psi_alf+0.000001p))-math_pi
        else Theta=atan(Psi_bet/( Psi_alf+0.000001p))
                                                                    #*Sector selection
if ((0 <= Theta) & (Theta < pi/6))          sector = 2  #*  0 <= Theta < 30 *#
if ((pi/6 <= Theta) & (Theta < pi/3))       sector = 3  #* 30 <= Theta < 60 *#
if ((pi/3 <= Theta) & (Theta < pi/2))       sector = 4  #* 60 <= Theta < 90 *#
if ((pi/2 <= Theta) & (Theta < 2*pi/3))     sector = 5  #* 90 <= Theta < 120*#
if ((2*pi/3 <= Theta) & (Theta < 5*pi/6))   sector = 6  #*120 <= Theta < 150*#
if ((5*pi/6 <= Theta) & (Theta <= pi))      sector = 7  #*150 <= Theta < 180*#
if ((-pi <= Theta) & (Theta < -5*pi/6))     sector = 8  #*180 <= Theta < 210*#
```

```
if ((-5*pi/6 <= Theta) & (Theta < -2*pi/3))    sector = 9  #*210 <= Theta < 240*#
if ((-2*pi/3 <= Theta) & (Theta < -pi/2))      sector = 10 #*240 <= Theta < 270*#
if ((-pi/2 <= Theta) & (Theta < -pi/3))        sector = 11 #*270 <= Theta < 300*#
if ((-pi/3 <= Theta) & (Theta < -pi/6))        sector = 12 #*300 <= Theta < 330*#
if ((-pi/6 <= Theta) & (Theta < 0))            sector = 1  #*330 <= Theta < 360*#

delta_Udc=udc_ref-udc_z                                                    #*voltage control
I_ref= I_ref_old + pi_r*delta_Udc + pi_r*((Ts/ti_r)-1)*delta_Udc_old       #* regulator PI
p_ref=I_ref*udc_z
I_ref_old=I_ref
delta_Udc_old=delta_Udc
                                                                           #* Control Structure
delta_p=p_ref-p
delta_q=q_ref-q
#*************************************************************************#
if (delta_p>hh)     Sp = 1                  #* p histeres *#
if (delta_p<(-hh))  Sp = 0
if ((delta_p<hh) & (delta_p>(-hh)))  Sp=Sp_old
 Sp_old=Sp
#*************************************************************************#
if (delta_q>hh)     Sq = 1                  #* q histeres *#
if (delta_q<(-hh))  Sq = 0
if ((delta_q<hh) & (delta_q>(-hh)))  Sq=Sq_old
Sq_old=Sq
#*************************************************************************#
if((Sp==1) & (Sq==0)){
        Sa=tab_11[sector],    Sb=tab_12[sector],    Sc=tab_13[sector]
        }
if((Sp==1) & (Sq==1)){
        Sa=tab_21[sector],    Sb=tab_22[sector],    Sc=tab_23[sector]
        }
if((Sp==0) & (Sq==0)){
        Sa=tab_31[sector],    Sb=tab_32[sector],    Sc=tab_33[sector]
        }
if((Sp==0) & (Sq==1)){
        Sa=tab_41[sector],    Sb=tab_42[sector],    Sc=tab_43[sector]
        }
Sa_old=Sa
Sb_old=Sb
Sc_old=Sc
#*************************************************************************#
if(Sa==0){
schedule_event(time+Ts,Sa_out,l4_0)
schedule_event(time+Ts,Sa_out_i,l4_1)
}
if(Sa==1){
schedule_event(time+Ts,Sa_out,l4_1)
schedule_event(time+Ts,Sa_out_i,l4_0)
}
if(Sb==0){
schedule_event(time+Ts,Sb_out,l4_0)
schedule_event(time+Ts,Sb_out_i,l4_1)
}
if(Sb==1){
schedule_event(time+Ts,Sb_out,l4_1)
schedule_event(time+Ts,Sb_out_i,l4_0)
}
if(Sc==0){
schedule_event(time+Ts,Sc_out,l4_0)
schedule_event(time+Ts,Sc_out_i,l4_1)
}
if(Sc==1){
schedule_event(time+Ts,Sc_out,l4_1)
schedule_event(time+Ts,Sc_out_i,l4_0)
}
schedule_next_time(time)
        }
}
```

A.5 SIMULINK MODEL

Different modulation techniques with additional Zero Sequence Signal (*ZSS*) has been simulated using *MATLAB-SIMULINK* program. The model is presented on Fig. A.5.1.

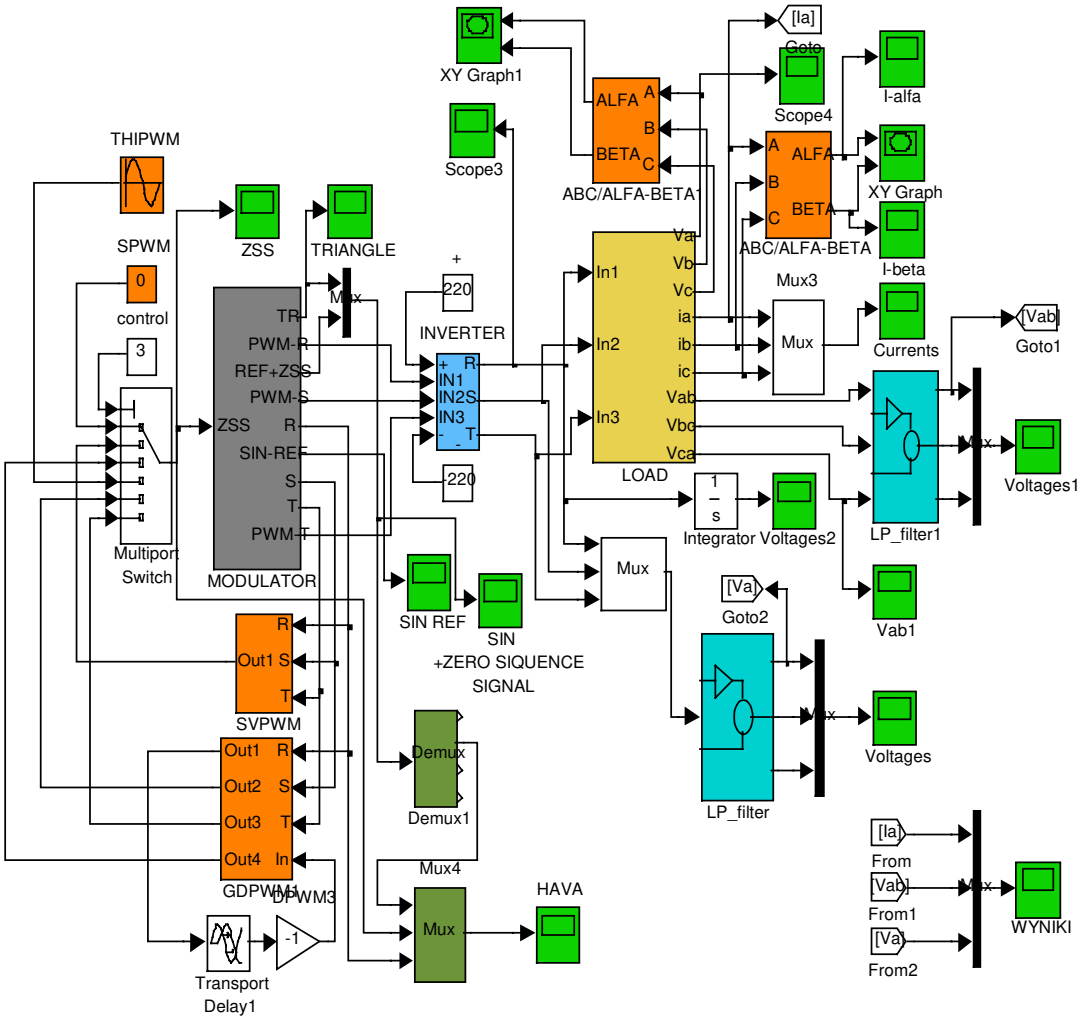


Fig. A.5.1. PWM model in Simulink

A.6 LABORATORY SETUP BASED ON DS1103

Laboratory setup consist of two parts:

- power circuit,
- control and measurement systems.

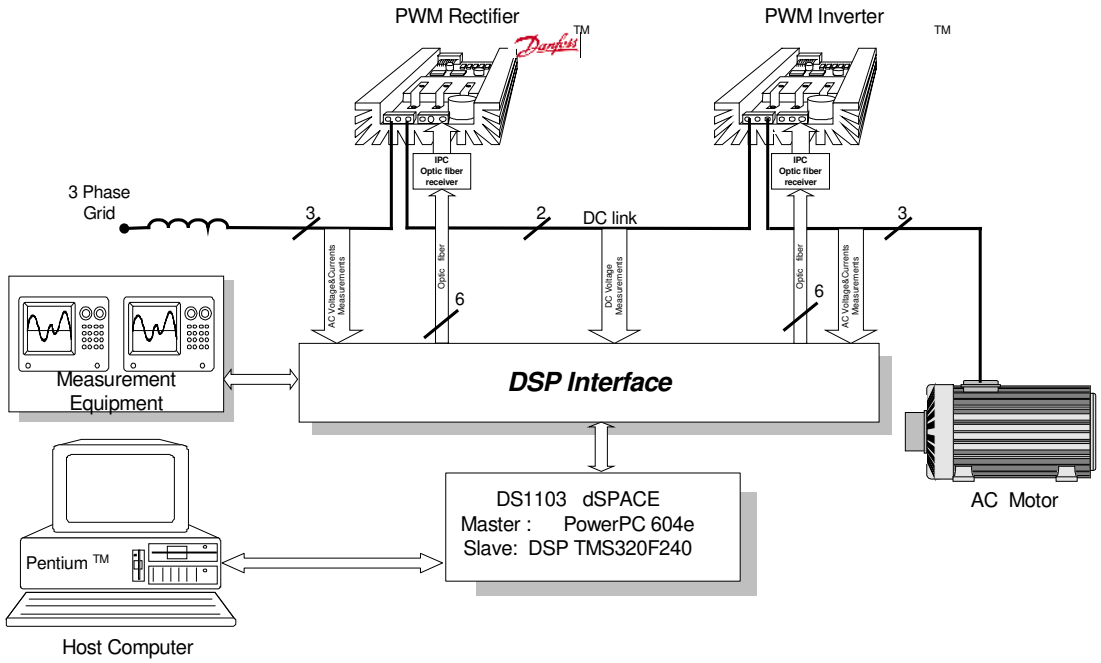


Fig. A.6.1. Configuration of laboratory setup

Power circuit

The laboratory setup (Fig. A.6.1) consists of two commercial Danfoss inverters *VLT 5000* series (Table A.6.1)[122] and a 3kW induction motor as active and resistor as a passive load. The main electrical parameters of the power circuit and control data are given in the Table A.6.2.

Table A.6.1 General parameters of VLT5005 inverter

U_{LN}	I_{LN}	$I_{VLT,N}$	$S_{VLT,N}$	$P_{VLT,N}$	Efficiency
[V]	[A]	[A]	[kVA]	[kW]	-
380	7	7,2	5,5	3,0	0,96

where:
U_{LN} - line voltage, I_{LN} - line current, $I_{VLT,N}$ - output current, $S_{VLT,N}$ - output power, $P_{VLT,N}$ - power on shaft.

Table A.6.2 Parameters used in experiment

Sampling frequency (DPC, VF-DPC):	50kHz
Sampling frequency (VOC, VFOC):	5kHz
Resistance of reactors R:	100mΩ
Inductance of reactors L:	10mH
DC-link capacitor:	470μF
Load resistance R_L:	100Ω
Switching frequency (DPC, VF-DPC) f:	3.5 kHz
Switching frequency (VOC, VFOC) f:	5 kHz
Phase voltage V:	230 RMS
Source voltage frequency:	50 Hz
DC-link voltage:	620V

Control and measurement systems

This part of system consists of following elements (Fig. A.6.2):

- dSpace *DS1103* board inserted into a PC-Pentium,
- interface board and measurement system,
- software.

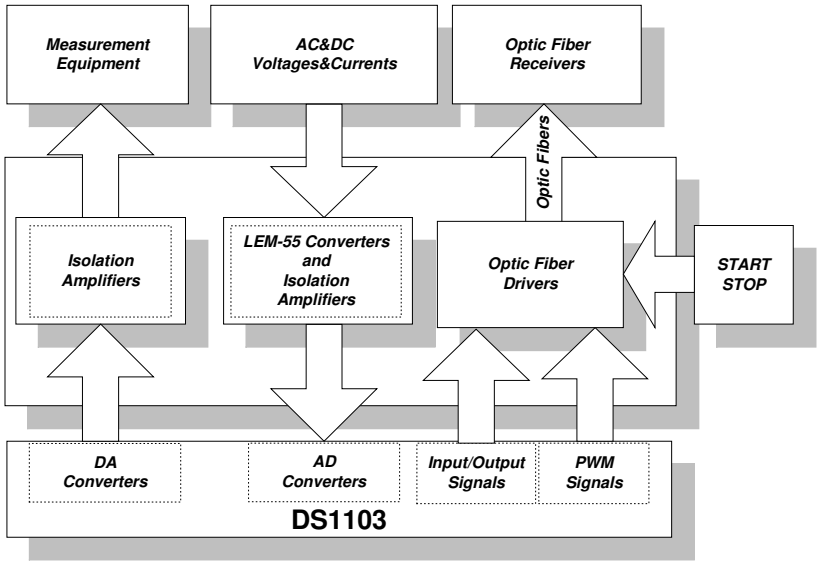


Fig. A.6.2. Block diagram of DSP interface

The power converters are controlled by the dSpace *DS1103* board inserted into a PC-Pentium (Fig. A.6.3). The mixed *RISC/DSP/CAN* digital controller based on two microprocessors (PowerPC604e – 333MHz and TMS320F240 – 20MHz) and four high-resolution analog-to-digital (A/D) converters (0.8μs - 12 bit) provide a very fast processing for floating point calculations. It makes possible real time control.

Fig. A.6.3 *DS1103* inside the Pentium PC

Basic parameters of DS1103[125-126]:

- master processor - Motorola PowerPC604e/333MHz
- slave processor – fixed point DSP of TI's TMS320F240
- 16 channels of ADC – 16 bit (resolution) – 4 μs (sampling time), $\pm$10V
- 4 channels of ADC – 12 bit – 0.8 μs, $\pm$10V

- 8 channels of DAC – 14 bit - 5 μs, ±10V
- incremental Encoder Interface – 7 channels
- 32 digital I/O lines
- ControlDesk software

The *DSP* subsystem, based on the Texas Instruments *TMS320F240* fixed point processor, is especially designed for control of power electronics. Among other I/O capabilities, the *DSP* provides one three-phase *PWM* generator and four single phase *PWM* generators. The other *CAN* subsystem based on Siemens 80C164 microcontroller is used for connection to a *CAN* bus.
The *PPC* has access to both the *DSP* and the *CAN* subsystems. The *PPC* is the master, whereas the *DSP* and the *CAN* microcontroller are slaves. The following figures give an overview of the functional units of the *DS1103 PPC*.

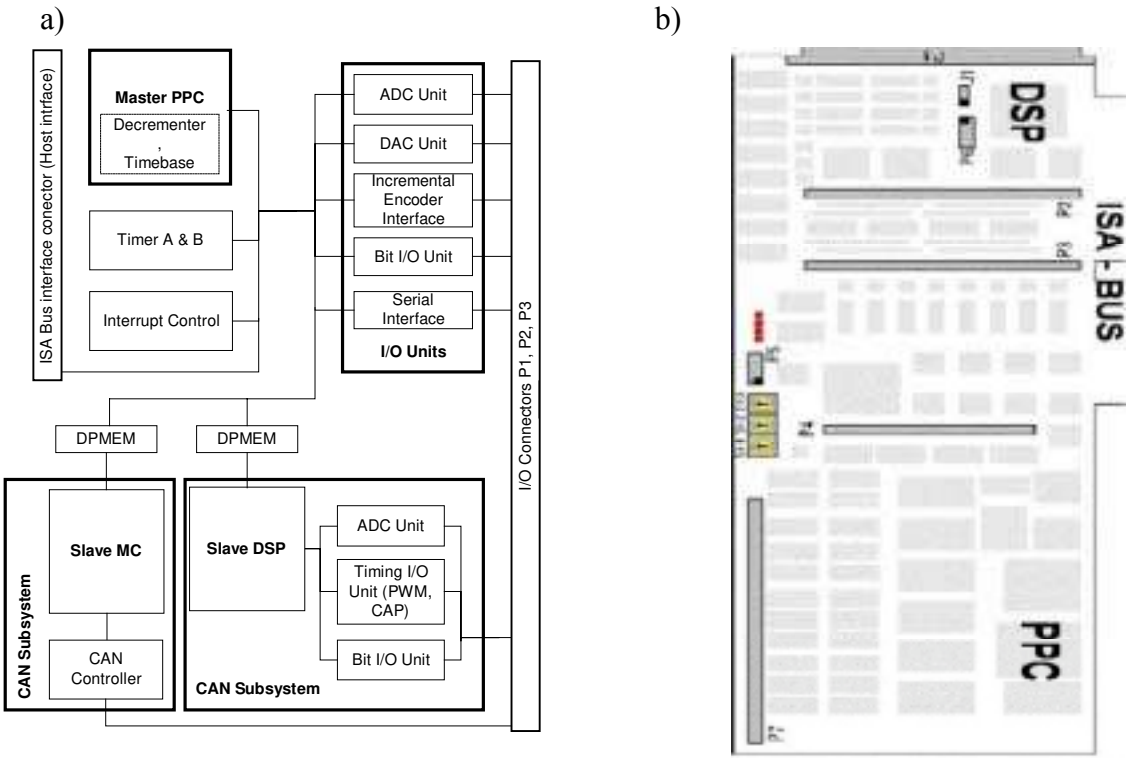


Fig.A.6.4. a) Block scheme of *DS1103*; b) Placement of main components.

DSP interface provide galvanic isolation between control board *DS1103* and power circuit. All *PWM* signals are generated by *DS1103* and send using optic fibers to the Interface and Protection Card *IPC* [124] that is mounted on the front panel of the inverter, instead of original Danfoss control board. The *IPC* includes: optic fiber receivers, 4MHz modulation of gate signals and protective function required by the *VLT*, i.e. short-circuit, shoot-trough of the DC link, over voltage and over temperature.

Software

Operation on *DS1103* is provided by an integrated *ControlDesk* program (Fig. A.6.5) [123]. Thanks to this application it is possible to change structure and parameters in real time. For algorithms application it is possible to use: *assembler*, *C language* (see the next page) and *Simulink* (Fig. A.6.6).

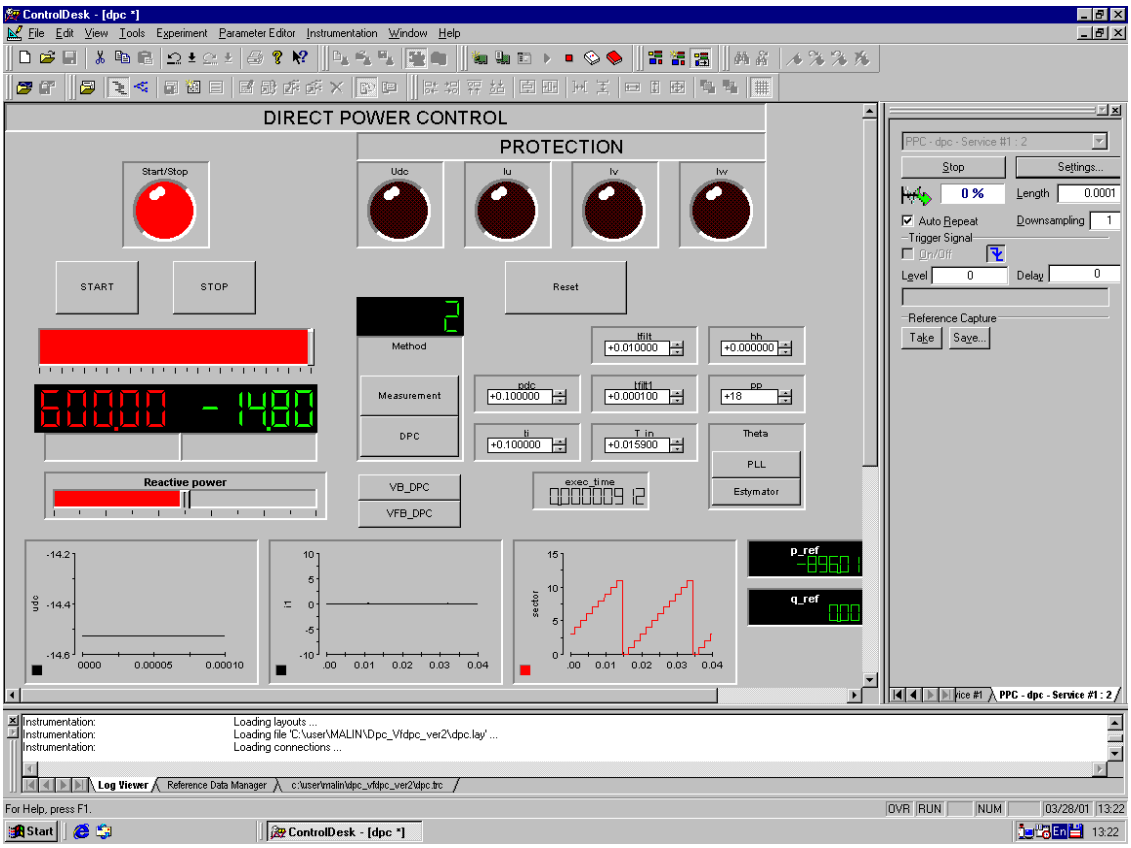


Fig. A.6.5 Screen of ControlDesk

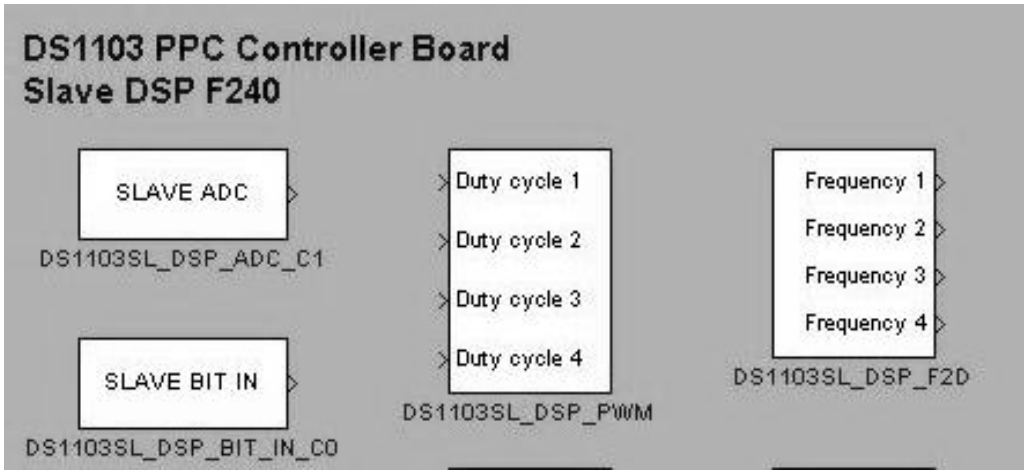


Fig. A.6.6 Some functional blocks for Simulink *RTI* interface.

```
/*DPC for dSpace 1103 - written by Mariusz Malinowski*/
#include <Brtenv.h>
#include <math.h>
//#include <Io1103.h>
/*-------------------------------------------------------------*/
#define DT 20e-6
#define _1_sqrt3 0.57735                                        /* Constants */
#define sqrt2 1.414213562
                                                                /* variables for communication with Slave DSP */
Int16 task_id = 0;                                              /* communication channel */
Int16 index = -1;                                               /* slave DSP command index */
Float64 deadband = 2e-6;                                        /* deadband period */
UInt16 sync_mode = SLVDSP1103_PWM3_SYNC_LEFT;                   /* sync mode */
Float64 exec_time, total_time;                                  /* variables for TRACE and COCKPIT */
Float64 period = 20e-6;                                         /* PWM period */
                                                                /* variables for PWM rectifier */
Float64 L=0.010,Kp=0.0,Ti=0.0,Ts=DT,pi=PI, ia, ib, ic, i_alf, i_bet, psi_alf,psi_bet,psi_alf_c,psi_bet_c;
Float64 Theta,delta_Udc,u_alf,u_bet,delta_udc_old=0.0,udc, udc_old=0.0,ualf,ubet;
Float64 p,q,delta_q,delta_p,p_old=0.0,q_old=0.0,p_ref, I_ref,I_ref_old=0.0,I_ref_max=10.0;
int sector,Sa_old,Sb_old,Sc_old,Sq,Sq_old,Sp,Sp_old, _Ts,_T_in;
volatile Float64 hh=0; udc_ref=600.0; q_ref=0.0; pdc=0.1; ti=0.1; T_in=0.0159; ku1=1435.0; ki1=18.55; ki2=18.55;

unsigned int tab_11[12]={1, 1, 1, 1, 1, 1, 0, 0, 0, 0, 0, 0};
unsigned int tab_12[12]={0, 0, 0, 0, 1, 1, 1, 1, 1, 1, 0, 0};
unsigned int tab_13[12]={1, 1, 0, 0, 0, 0, 0, 0, 1, 1, 1, 1};
unsigned int tab_21[12]={1, 1, 0, 0, 0, 1, 0, 0, 1, 1, 1, 0};
unsigned int tab_22[12]={1, 1, 1, 0, 1, 1, 0, 0, 0, 1, 0, 0};
unsigned int tab_23[12]={0, 1, 0, 0, 1, 1, 1, 0, 1, 1, 0, 0};
unsigned int tab_31[12]={1, 1, 1, 1, 1, 0, 0, 0, 0, 0, 0, 1};
unsigned int tab_32[12]={0, 0, 0, 1, 1, 1, 1, 1, 1, 0, 0, 0};
unsigned int tab_33[12]={1, 0, 0, 0, 0, 0, 0, 1, 1, 1, 1, 1};
unsigned int tab_41[12]={1, 1, 1, 0, 0, 0, 0, 0, 0, 1, 1, 1};
unsigned int tab_42[12]={0, 1, 1, 1, 1, 1, 1, 0, 0, 0, 0, 0};
unsigned int tab_43[12]={0, 0, 0, 0, 0, 1, 1, 1, 1, 1, 1, 0};

void measure(void);
void control(void);
void da_converter(void);
void PWM_sync_interrupt(void);
/*-------------------------------------------------------------*/
void measure(void)
{
ds1103_adc_start(DS1103_ADC_CH17);                              /* specifies channels to be started */
ds1103_adc_start(DS1103_ADC_CH18);
ds1103_adc_start(DS1103_ADC_CH19);

udc= ds1103_adc_read_ch(17);                                    /* read converter 17*/
 ia= ds1103_adc_read_ch(18);
 ib= ds1103_adc_read_ch(19);

udc=udc-0.0025; ia=ia+0.002; ib=ib+0.003;                       /*scaling signals */
udc=ku1*udc;  ia=ki1*ia;  ib=ki2*ib;
}

void control(void)
 {
ic=-(ia+ib); uc=-(ua+ub);                                       /*Transformations*/
i_alf = sqrt23*(ia-0.5*ib-0.5*ic);
i_bet = sqrt23*(_sqrt3to2)*(ib-ic);
                                                                /*  Flux, instantaneous active and reactive power estimator  */
ualf=0.6666*udc*(Sa_old-0.5(Sb_old+Sc_old));                    /*Converter Voltage*/
ubet=_1sqrt3*udc*(Sb_old- Sc_old);
psi_alf_c += Ts*(ualf-_T_in*psi_alf_c);                         /*Converter Flux*/
psi_bet_c += Ts*(ubet-_T_in*psi_bet_c);
psi_alf = psi_alf_c + i_alf*L;                                  /* Line Flux */
psi_bet = psi_bet_c + i_bet*L;
p= 2*314*(psi_alf*i_bet - psi_bet*i_alf);                       /* Instantaneous power estimations*/
q= 314*(psi_alf*i_alf + psi_bet*i_bet);
Theta_est=atan2(psi_bet,psi_alf);
                                                                /*          Sector detection          */
if ((0 <= Theta) & (Theta < pi_6))          {sector = 1;}  /*  0 <= Theta < 30 */
if ((pi_6 <= Theta) & (Theta < _1pi3))      {sector = 2;}  /* 30 <= Theta < 60 */
if ((_1pi3 <= Theta) & (Theta < pi_2))      {sector = 3;}  /* 60 <= Theta < 90 */
```

```
if ((pi_2 <= Theta) & (Theta < _2pi3))       {sector = 4;}  /* 90 <= Theta < 120*/
if ((_2pi3 <= Theta) & (Theta < _5pi_6))     {sector = 5;}  /*120 <= Theta < 150*/
if ((_5pi_6 <= Theta) & (Theta <= pi))       {sector = 6;}  /*150 <= Theta < 180*/
if ((-pi <= Theta) & (Theta < -_2pi3))       {sector = 7;}  /*180 <= Theta < 210*/
if ((-_5pi_6 <= Theta) & (Theta < -_2pi3))   {sector = 8;}  /*210 <= Theta < 240*/
if ((-_2pi3 <= Theta) & (Theta < -pi_2))     {sector = 9;}  /*240 <= Theta < 270*/
if ((-pi_2 <= Theta) & (Theta < -_1pi3))     {sector = 10;} /*270 <= Theta < 300*/
if ((-_1pi3 <= Theta) & (Theta < -pi_6))     {sector = 11;} /*300 <= Theta < 330*/
if ((-pi_6 <= Theta) & (Theta < 0))          {sector = 0;}  /*330 <= Theta < 360*/
                                                                                    /*Control structure*/
delta_Udc=udc_ref-udc;
I_ref=I_ref_old+pdc*delta_Udc+pdc*((Ts/ti)-1)*delta_udc_old;
p_ref=I_ref*udc;
delta_p=p_ref-p;
if (delta_p>hh)     Sp = 1;                                                         /* p histeres */
if (delta_p<(-hh))  Sp = 0;
if ((delta_p<hh) & (delta_p>(-hh)))  Sp=Sp_old;
/*********************************************************************/
delta_q=q_ref-q;
if (delta_q>hh)     Sq = 1;                                                         /* q histeres */
if (delta_q<(-hh))  Sq = 0;
if ((delta_q<hh) & (delta_q>(-hh)))  Sq=Sq_old;
/*********************************************************************/
if((Sp==1) & (Sq==0)){D_R=tab_11[sector]; D_S=tab_12[sector]; D_T=tab_13[sector]; }
if((Sp==1) & (Sq==1)){D_R=tab_21[sector]; D_S=tab_22[sector]; D_T=tab_23[sector]; }
if((Sp==0) & (Sq==0)){D_R=tab_31[sector]; D_S=tab_32[sector]; D_T=tab_33[sector]; }
if((Sp==0) & (Sq==1)){D_R=tab_41[sector]; D_S=tab_42[sector]; D_T=tab_43[sector];}

udc_old=udc; p_old=p; q_old=q;                                                      /*Old values*/
Sp_old=Sp; Sq_old=Sq; Sa_old=D_R; Sb_old=D_S; Sc_old=D_T; I_ref_old=I_ref; delta_udc_old=delta_Udc; ;
break;                                          /*END*/
 }
 }

void da_converter(void)
{
ds1103_dac_write(1,ia*0.1);                                         /* output via DS1103 on-board DAC channel 1 */
ds1103_dac_write(2,px*0.001);
ds1103_dac_write(3,qx*0.001);
ds1103_dac_strobe();
}

void PWM_sync_interrupt(void)                                       /* interrupt service routine for PWM sync interrupt */
{
 host_service(1, 0);                                                                /* TRACE service */
 ds1103_tic_start();                                                              /* start time measurement */
measure();
control();
ds1103_slave_dsp_pwm3_duty_write(task_id, index,D_R,D_S,D_T);
da_converter();
exec_time = ds1103_tic_read();
}

main()
{
ds1103_init();                                                                  /* basic initialization of DS1103 */
ds1103_tic_delay(2.0e-6);                                                          /* ensure 2 us settling time */
ds1103_dac_init(DS1103_DACMODE_LATCHED);                                      /* init D/A converter in latched mode */
ds1103_slave_dsp_communication_init();                                  /* initialization of slave DSP communication */
ds1103_slave_dsp_pwm3_init(task_id, period,D_R,D_S,D_T, deadband, sync_mode);   /* init and start of 3-phase PWM on DSP */
ds1103_slave_dsp_pwm3_start(task_id);
ds1103_slave_dsp_pwm3_duty_write_register(task_id, &index);             /* registration of PWM duty cycle update command */
ds1103_set_interrupt_vector(ds1103_int_slave_DSP_PWM,(DS1103_Int_Handler_Type)&PWM_sync_interrupt,save_regs_on);
ds1103_enable_hardware_int(DS1103_INT_SLAVE_DSP_PWM);
ds1103_GLOBAL_INTERRUPT_ENABLE();

 while(1)
 {
                        master_cmd_server();
                        host_service(0, 0);                                                         /*
COCKPIT service */
 }
}
```

(a) (b)

Fig. A.6.7. View of the laboratory setup
(a) Danfoss converters, (b) interface, measurements and PC with *DS1103* card.

A.7 LABORATORY SETUP BASED ON ADSP 21062 (SHARC)

Some experiments concern VOC was carried-out at experimental setup of the Institute of Energy Technology at Aalborg University (Denmark) (Fig.A.7.1). The laboratory setup consists of a three-phase 30 kVA programmable power supply (Fig.A.7.2), two commercial inverters controlled by two *DSP's* (*ADSP 21062*) and a motor-generator setup as active load.

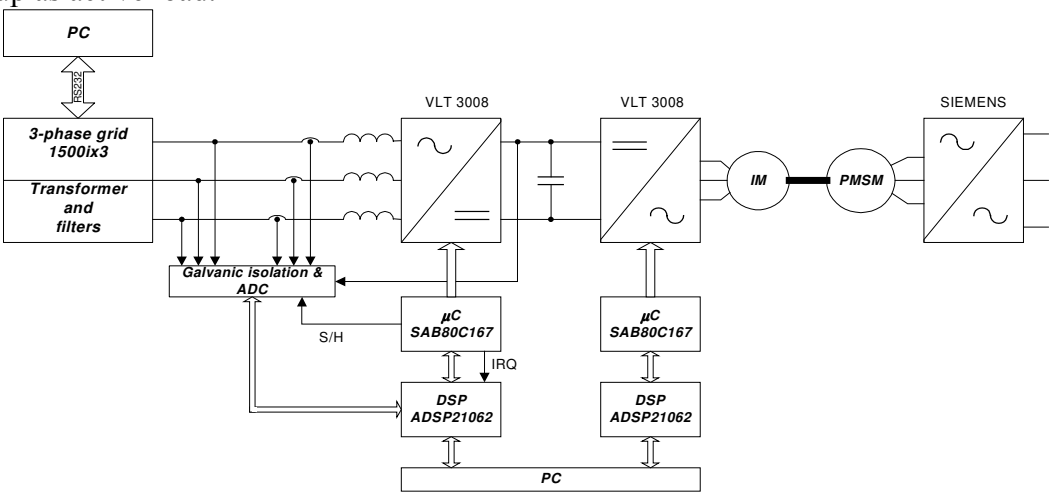


Fig. A.7.1. Laboratory setup based on sharc *ADSP 21062*

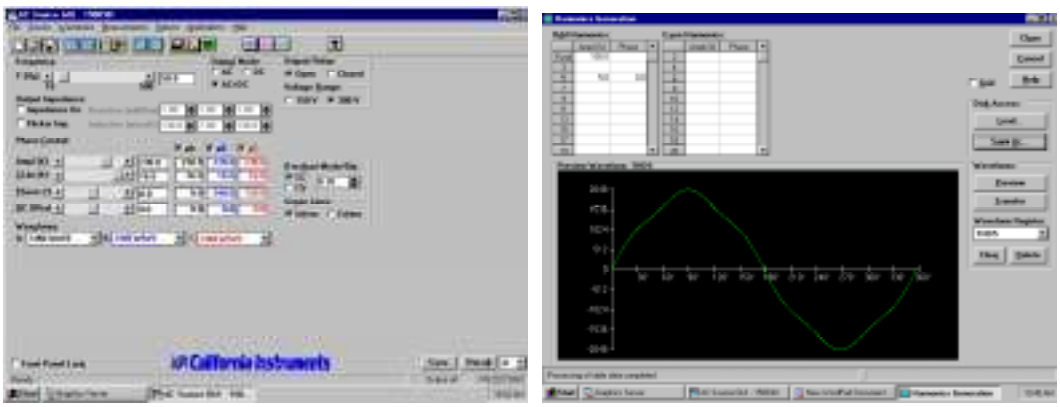


Fig.A.7.2. Three-phase 30 kVA programmable power supply of California Instruments (1500ix3)

A.8 HARMONIC LIMITATION

IEEE 519-1992
Sets limits for harmonic voltage and currents at the Point of Common Coupling (PCC). It places responsibility on large commercial and industrial consumers.

Voltage Distortion Limits		
Bus Voltage at PCC	**Individual voltage distortion [%]***	**Total voltage distortion [%]**
below 69kV	3.0	5.0
69kV to 138kV	1.5	2.5
Above 138kV	1.0	1.5

* maximum for individual harmonic

Current Distortion Limits						
Maximum odd harmonic current distortion in percent of I_L for general distribution systems (120V – 69kV)						
I_{SC}/I_L	<11	11≤n<17	17≤n<23	23≤n<35	35≤n	TDD
<20	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

I_{SC}- maximum short circuit current at the PCC
I_L- fundamental of the average (over 12 months) maximum monthly demand load current at PCC
TDD – total demand distortion, harmonic current distortion in % of maximum demand load current (15 or 30 minute demand)

IEC 61000-3-2 (IEC 1000-3-2)
It is addresses for small customer equipment. Emphasis on *public, low-voltage and household.*

IEC 1000-3-2 Limits for Class D Equipment		
Harmonic order	**Maximum permissible harmonic current per watt**	**Maximum permissible harmonic current**
N	mA/W	A
3	3.4	2.3
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
13≤n≤39 (odd har. only)	3.85/n	Refer to class A

IEC 61000-3-4 (IEC 1000-3-4)
It's addresses for larger customers (single and three-phase harmonic limits). It gives a consideration of the short circuit ratio R_{SCC}.

IEC 1000-3-4 limits for three-phase equipment						
Minimal R_{SCC}	**Upper limits for harmonic distortion factors**		**Limits for individual harmonic in % of I_1**			
	THD	*PWHD*	I_5	I_7	I_{11}	I_{13}
66	17	22	12	10	9	6
120	18	29	15	12	12	8
175	25	33	20	14	12	8
250	35	39	30	18	13	8
350	48	46	40	25	15	10
450	58	51	50	35	20	15
>600	70	57	60	40	25	18

$$PWHD = \sqrt{\sum_{n=14}^{40}\left(\frac{I_n}{I_1}\right)^2}$$

A.9 EQUIPMENT

Instrument	Type
Digital oscilloscope	LeCroy 9314AM 400MHz
Digital oscilloscope	Oscyloskop Tektronix TDS3014 100MHz
Analyzer	NORMA D6000 - Goerz Instruments
Voltage differential probe	Tektronix P5200
Current probe	LEM PR30
Simualtion program	SABER - Analogy
Simualtion program	Matlab6.0, Simulink and Real Time Workshop
Simualtion program	DESIM

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Books and Overview Papers

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