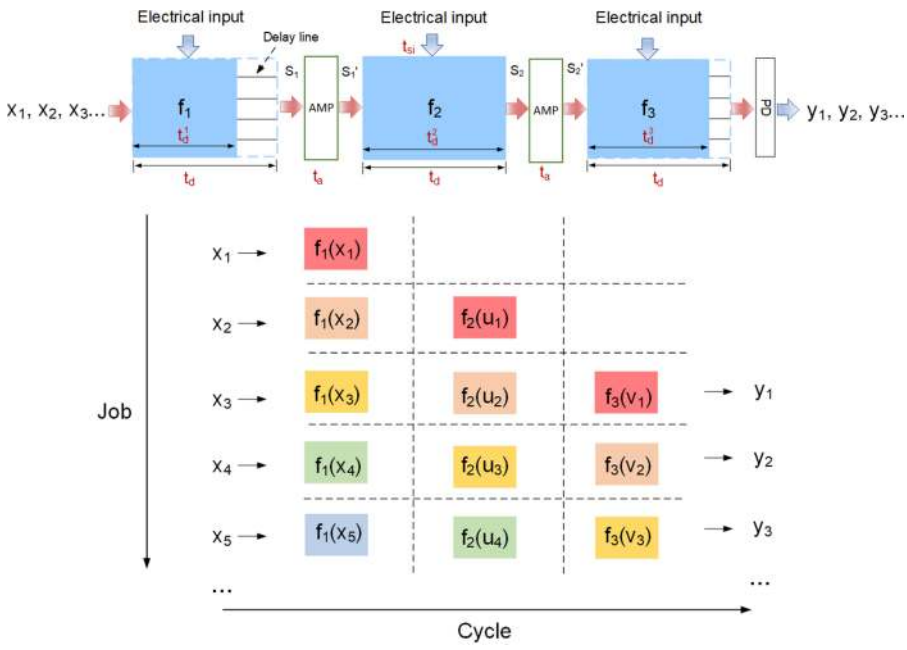
IEEE Photonics Journal
An IEEE Photonics Society Publication

Open Access

Sequential Logic and Pipelining in Chip-Based Electronic-Photonic Digital Computing

Volume 12, Number 6, December 2020

Zhoufeng Ying
Chenghao Feng
Zheng Zhao
Jiaqi Gu
Richard Soref, *Life Fellow, IEEE*
David Z. Pan, *Fellow, IEEE*
Ray T. Chen, *Fellow, IEEE*



DOI: 10.1109/JPHOT.2020.3031641

Sequential Logic and Pipelining in Chip-Based Electronic-Photonic Digital Computing

Zhoufeng Ying,[1] **Chenghao Feng**,[1] **Zheng Zhao**,[2] **Jiaqi Gu**,[2] **Richard Soref**,[3] ***Life Fellow, IEEE***, **David Z. Pan**,[2] ***Fellow, IEEE***, **and Ray T. Chen**,[1] ***Fellow, IEEE***

[1]Microelectronics Research Center, The University of Texas at Austin, Austin, Texas 78758 USA
[2]Computer Engineering Research Center, The University of Texas at Austin, Austin, Texas 78705 USA
[3]Department of Engineering, University of Massachusetts Boston, Boston, MA 02125 USA

DOI:10.1109/JPHOT.2020.3031641

Manuscript received September 7, 2020; accepted October 12, 2020. Date of publication October 16, 2020; date of current version October 30, 2020. This work was supported by the Multidisciplinary University Research Initiative (MURI) program through the Air Force Office of Scientific Research (AFOSR) under Grants FA 9550-17-1-0071, FA9550-19-1-0341. Corresponding author: Ray T. Chen (email: chenrt@austin.utexas.edu).

Abstract: The recent rapid progress in integrated photonics has catalyzed the development of integrated optical computing in this post-Moore's law era. Electronic-photonic digital computing, as a new paradigm to achieve high-speed and power-efficient computation, has begun to attract attention. In this paper, we systematically investigate the optical sequential logic and pipelining in electronic-photonic computing, which together offer a solution to potential problems in latency and power budget as the size of electronic-photonic computing circuits scales up considerably to achieve much more complex functions. Pipelining and sequential logic open up the possibility of high-speed very-large-scale electronic-photonic digital computing.

Index Terms: Optical computing, logic circuits, pipeline processing, optical logic devices, electro-optic devices.

1. Introduction

Integrated photonics has been evolving and maturing rapidly in this decade, which not only revolutionizes the optical interconnects industry [1]–[8], but also provides a solid foundation for the exploration of optical computing in this post-Moore's-law era [9]–[11]. The emergence of various components in integrated photonics with satisfying performances, such as high bandwidth and low power consumption, has made the electronic-photonic digital computing (EPDC) become one of the most promising candidates to improve the computation capability of chips further. Wide investigations of EPDC have been carried out these years, ranging from fundamental logic gates [12]–[15] to functional circuits [11], [16]–[19] and logic synthesis algorithms [20]–[22]. However, the specifications and requirements of very-large-scale EPDC circuits have not been discussed yet.

Several concerns will emerge as the circuit size of EPDC scales up significantly. First, the latency accumulates along the propagation path, which at some point may wipe out the advantage of EPDC in speed over the electronic counterpart as the size of computing circuits becomes much

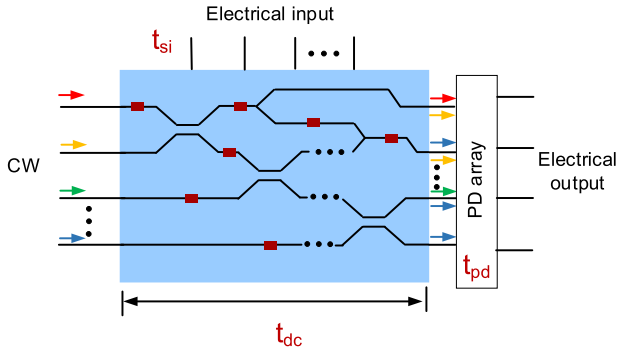


Fig. 1. A typical optical combinational circuit. At each clock cycle, the electrical inputs will first be injected into these electro-optic modulators (red rectangles) to set the circuit into a stable state after a period of time t_{si}. Then optical beams of continuous wave (CW) start to propagate through the circuit at the speed of light and it takes time t_{dc} to finally arrive at the photodetector (PD) array, which may induce an additional delay of t_{pd}.

larger. Second, the circuit will also suffer from propagation loss as the light goes through more components. Unlike the electronic transistors whose signals can be normalized to the supply voltage or ground easily, there are no efficient and compact integrated optical amplifiers suitable for computing available up to now. These factors will finally limit the size of the circuits and thus narrow its applications.

In this paper, we bring in the sequential logic and pipelining that have been widely used and developed in electronic very-large-scale integration (VLSI) into EPDC in order to resolve the problems of latency and loss. Optical sequential logic (OSL) and amplified sequential logic (ASL) are proposed and discussed. The comparison of combinational logic and sequential logic is then conducted, followed by a thorough calculation of the latency and loss improvement with the assist of optical memory units and optical amplifiers as well as the pipelining.

2. Optical Combinational Logic

EPDC uses sophisticated electronics to control the circuits while allowing photons to go through their waveguided circuits at the speed of light to process the information [10], [11]. Up to now, most of the demonstrations on the EPDC, including logic gates and functional circuits [11], [12], [14], [16], [23]–[31], can be categorized as optical combinational logic (OCL). Fig. 1 shows a typical on-chip EPDC circuit that can cover most of these proposed structures. Electrical inputs are fed into these electrical-optical (EO) modulators first to set the circuit into a stable state after a period of time t_{si}. Light beams with a single wavelength or multiple wavelengths (or even with different polarization or modes) start to propagate through the circuit, which take a time t_{dc} to arrive at the other end before being received by photodetectors (sometimes photodetectors are not required). The latency of the photodetectors is marked as t_{pd}. The longest path of the combinational circuit that determines t_{dc} is called the critical path. Normally, there are three ways to present combinational logic, namely circuit diagrams, truth tables, and Boolean expressions, which are widely used in the researches of EPDCs [32], [33].

The following are the characteristics of the optical combinational logic. First, the output signals of the optical combinational logic are only a function of its input signals. In other words, $output = f(electrical\ inputs)$. Second, output signals are valid after a certain period once the input signals become valid. Third, the circuit does not contain any kind of information-storing elements. Fourth, no kind of feedback loops exists in the circuits. The last two characteristics mean that optical combinational logic is also a time-independent logic. The circuit depicted in Fig. 1 shows these characteristics of a combinational circuit perfectly. No information-storing devices or feedback loops exist in the circuit. During each clock cycle, all the electrical inputs will be applied simultaneously

into the circuit and the output will be valid after a short period of time. The requirement for this delay, in other words the clock period t_c, can be written as

$$t_c \geq t_{si} + t_{dc} + t_{pd} \tag{1}$$

where t_{si} is the set-up time of the combinational circuit, t_{dc} is the propagation latency of a combinational circuit, and t_{pd} is the set-up time of the photodetector array. Fortunately, the state-of-the-art modulators [34]–[36] and photodetectors [37], [38] are capable of providing ultrasmall t_{si} and t_{pd}, for example 10 ps or even less. It also costs only sub-picoseconds for light to go through one gate in EPDC. Therefore, after adding all of them up, as long as the circuit size stays small, it is still possible to achieve an ultrahigh computing clock rate in the tens-of-GHz range, a rate faster than the clock rate of commercial central processing units (CPUs) and graphic processing units (GPUs). However, as the photonic circuit size scales up with more components and certainly longer critical path, t_{dc} may dominate the entire latency and limit the computing speed significantly, wiping out an essential advantage of the EPDC. Another limitation that the EPDC has to face during scaling is the optical propagation loss, which may result in an exponential increase in the optical input power requirement and which may cause difficulties in detection. In addition, there are not yet any suitable integrated amplifiers for computing with high bandwidth, low power consumption, high efficiency, and small footprint in integrated photonics. The reason that the size requirement of amplifiers is mentioned here is that it will induce additional propagation latency as well.

In summary, optical combinational logic, as the most straightforward form of the EPDC, has an intrinsic limitation in circuit size due to latency and loss. Switching from combinational logic to sequential logic is a natural step, as we can tell from the successful experience of the development of VLSI.

3. Optical Sequential Logic

Unlike optical combinational logic circuits that only depend on currently present inputs, optical sequential logic (OSL) circuits have some built-in information-storing elements. It means that OSL circuits are able to take into account the current inputs as well as the previous input sequences or the previous outputs that have been stored. Here are some characteristics of optical sequential logic. First, optical sequential circuits are constructed with combinational circuits and optical memory unit, as shown in Fig. 2(a), where the new memory unit is shown in Fig. 2(c). Second, the circuit output signals are a function of its input signals and of its stored signals. Third, the memory units in an optical sequential logic circuit are normally trigged and controlled by a clock signal as we will talk only about the synchronous sequential logic hereinafter. Forth, the validity time of the sequential circuit is determined by both the clock signal and the type of the memory unit, such as edge-sensitive or level-sensitive.

OSL with memory units provides an additional degree of freedom for us to use in order to achieve large-scale computing circuits. For example, as shown in Fig. 2(b), a large combinational logic circuit can now be divided into multiple small circuits, marked as f_1, f_2, f_3 and so on, connected with memory units. The internal output signals from each combinational circuit will be stored in the memory unit and regenerated at the trigger by the next clock signal. In other words, a complex function can be separated into multiple subfunctions and distributed into several time slots in a row, rather than being squeezed into a single circuit and finished in one clock cycle. OSL disentangles the direct correlation of complexity of the function with the circuits. In addition, these memory units also serve as pump stations for the light to be boosted after a short distance periodically because each memory employs a sufficiently strong CW optical input to its EO modulator.

Fig. 2(d) shows the timing diagram. Within each clock cycle, all electrical signals will be fed into the circuit through EO modulators and this process takes a time t_{si} to get stabilized. Meanwhile, memory units will be trigged by the clock signal as well to send out the stored signals within the period of time t_{qr}. After all of the circuits are set successfully by the electrical signals, as well as the input optical signals are ready, then the light beams will propagate through the combinational circuit, which takes a time t_d before they arrive at the next memory unit, there to be stored within t_{sr}.

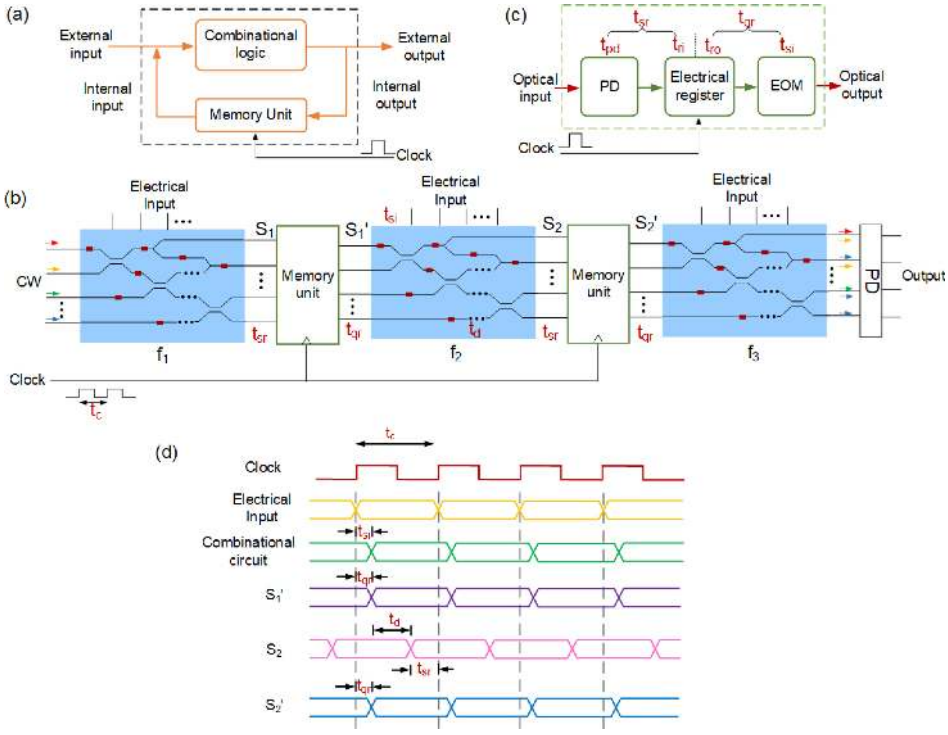


Fig. 2. (a) Diagram of sequential logic, consisting of optical combinational logic and optical memory units. (b) A typical optical sequential circuit with multiple combinational logic circuits connected with register arrays. (c) One possible realization of the optical memory unit, one line within the memory bank: PD: photodetector; EOM: electro-optic modulator. (d) Timing diagram of optical sequential logic.

Therefore, the timing requirement for this sequential circuit with pipelining will be

$$t_c \geq \max\{t_{qr}, t_{si}\} + t_d + t_{sr} \tag{2}$$

where t_d is the maximum delay time of all the combinational circuits, t_{qr} is the clock-to-output delay time of the memory unit, t_{sr} is the set-up time of the memory unit, and t_{si} is the set-up time of the combinational circuit.

The memory units that store and retrieve optical signals at the same pace with the clock serve as critical building blocks in the OSL. Since integrated all-optical memory devices for this purpose are not off-the-shelf yet, mature electrical memory units, especially the electrical registers, are adopted here in cooperation with photodetectors and electro-optical modulators, as shown in Fig. 2(b). Fortunately, nowadays, the CMOS-compatible fabrication technology for integrated photonics has reached a high state of development that has enabled the electronic-photonic hybridization in the same chip with few constraints [39], [40]. In other words, electronics transistors can be fabricated anywhere in the same chip with photonic components such as adjacent to photodetectors and modulators. Advanced packaging technique [41] to integrate electronic chips with photonic chips will be a promising method to achieve the hybridization of the components mentioned above. The fabrication of these integrated photonic components including PDs and EOMs are already available in most of the integrated photonics foundries with acceptable cost and stable performance [42]. While the hybridization of photonic and electronic components is still under development in industry and we believe the cost will be low enough after they are widely adopted in many applications.

It is worth mentioning that there are many optical sequential logic gates and circuits reported in the all-optical logic area, such as optical binary counter [43], [44], circulating shift register [45], and pattern recognition circuit [46]. As an important paradigm of optical computing, all-optical logic

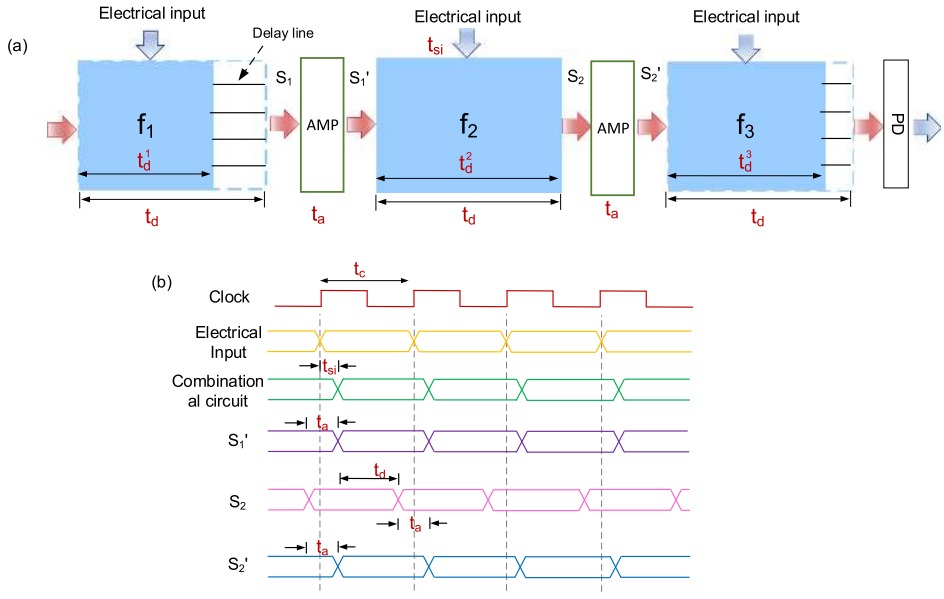


Fig. 3. (a) Diagram of the amplified sequential logic. The delay of each combinational logic circuit is fine-tuned using delay lines to be the same. Optical amplifier banks (AMP) are used to connect these circuits. (b) Timing diagram of amplified sequential logic.

normally uses semiconductor optical amplifier (SOAs) as active elements to switch the optical output by light, which differs from how EPDC does. However, it should be accepted that the combination of these two may bring in more attractive functions in the future.

4. Amplified Sequential Logic

One advantage of synchronizing the entire OSL circuit using a universal clock is that the delay of each small OCL circuit does not have to be the same, which eases the effort of adjusting precisely the size and latency of each circuit.

In electronic domain, due to the tedious delay adjustment in VLSI as well as the easy accessibility of mature electronic registers, the universal clock for sequential logic is adopted naturally. However, in optical domain, the latency actually could be controlled more easily and precisely using waveguides/delay lines. For instance, 1 μm long waveguide will induce only $\sim$10 fs delay. By using this approach, the amplified sequential logic (ASL) is proposed and discussed here.

Fig. 3 depicts the diagram of the ASL. The delay of each combinational logic circuit ($t_d^1,\ t_d^2,\ t_d^3 \cdots$) is fine-tuned to be the same ($t_d = \max(t_d^1,\ t_d^2,\ t_d^3 \cdots)$) using delay lines. Therefore, it is guaranteed that the internal outputs will arrive at the amplifiers simultaneously, and then be boosted and sent out at the same time if the amplifiers are identical. Thus, the electrical inputs can be injected at the right timing. This uniform pace produces the same effects as a universal clock does.

The optical amplifiers inserted in the circuits continue to boost the signals to tackle with the propagation loss. Although the all-optical amplifier in integrated photonics for computing has yet to be developed, the progress in optical-to-electrical-to-optical (OEO) devices that are compact, high-speed, and power-efficient makes the proposed ASL more achievable [47], [48] since the OEO repeater provides optical gain. Assuming the delay caused by the amplifier is t_a. Then the time requirement for the ASL, as shown in Fig. 3(b), can be written as

$$t_c \geq \max\{t_a, t_{si}\} + t_d \tag{3}$$

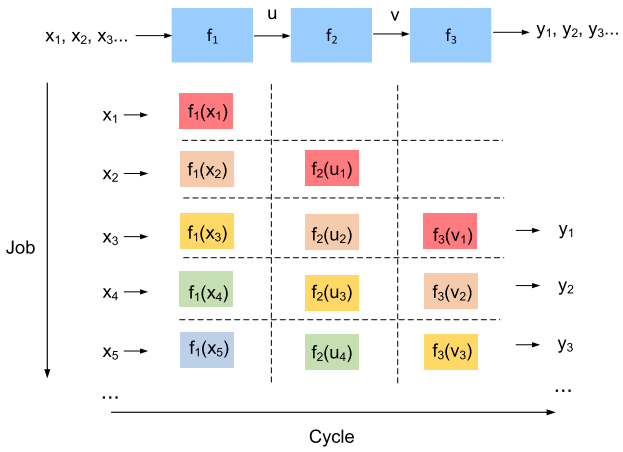


Fig. 4. Diagram of pipelining.

Compared to the OSL, one disadvantage of ASL is that the clock rate is not flexible since the delay for each small combinational logic circuit is fixed. On the contrary, the OSL can run at a lower clock rate for some power-saving purposes in some applications due to the memory unit that can hold signals much longer.

5. Pipelining

The precise and uniform pace for each combinational logic in OSL and ASL makes them well-prepared for pipelining. Pipelining is an essential and commonly-used concept in sequential logic to improve computing throughput. Partitioning of combinational circuits into N parts and operation as a sequential circuit is called pipelining with stages of *N*.

An example of pipelining with three stages is shown in Fig. 4. A large OCL is split into three smaller OCLs, marked as f_1, f_2 and f_3. The input/job sequences are x_1, x_2, x_3 and so on. After going through three circuits, those jobs will generate the internal outputs u_1, u_2, $u_3 \cdots$ and v_1, v_2, $v_3 \cdots$ as well as external outputs $y_1, y_2, y_3 \cdots$. At the first clock cycle, x_1 will be fed into the circuit first and processed by circuit f_1 and generates u_1. At the second clock cycle, u_1 will move forward to the second circuit f_2 to generate v_1 while at the same time x_2 can be fed into the first circuit to obtain u_2. At the third clock cycle, v_1 will move to the final block f_3 to generate the output y_1, and u_2 to the second block f_2, and at the same time x_3 will be fed into f_1. Since then, with the cycles going on, we will obtain an external output at each cycle. Unlike using a large combinational circuit where input sequence is fed only after previous output becomes available with two- thirds of the circuits idle, OSL and ASL can feed the input more frequently and keep all functional circuits performing calculation at its full speed without any idle time slots. We can draw a preliminary conclusion readily that N-fold pipelining improves the throughput by nearly a factor of *N* if the latency of the memory units or amplifiers is negligible as compared to the latency of each combinational circuit.

Now we will conduct a theoretical calculation of the latency, throughput, and propagation loss of the pipelined OSL and ASL as compared to the OCL without pipelining. Due to the similarity between the analysis of OSL and ASL in terms of pipelining, we will take ASL as an example.

5.1 Latency

The latency means the time required for a particular signal to travel from the beginning to the end. The total latency of OCL and ASL are

$$L_C = t_{si} + t_{dc} + t_{pd} \tag{4}$$

$$L_S = \max\{t_a, t_{si}\} \times N + t_d \times N + t_{pd} \tag{5}$$

respectively, where $t_d = \max\{t_d^i\}, i = 1, 2, \cdots N$.

5.2 Throughput

The throughput means the number of jobs it can process in a certain time period. The maximal total throughput of the OCL and ASL are

$$TP_C = [t_{si} + t_{dc} + t_{pd}]^{-1} \tag{6}$$

$$TP_S = [\max\{t_a + t_{si}\} + t_d]^{-1} \tag{7}$$

respectively. Assume $t_{di} = t_d = \frac{t_{dc}}{N}$, which means each small combinational logic circuit in the ASL has equal delay and no extra delay lines are required. Assume $t_a = 2t_{si} = 2t_{pd}$. Now the latency ratio (LR) and throughput ratio (TPR) can be calculated as

$$LR = \frac{L_S}{L_C} = \frac{(N + 0.5) \times t_a + N \times t_d}{t_a + N \times t_d} = \frac{(N + 0.5) \times k + N}{k + N} \tag{8}$$

$$TPR = \frac{TP_S}{TP_C} = \frac{N \times t_d + t_a}{t_d + t_a} = \frac{N + k}{1 + k} \tag{9}$$

where $k = \frac{t_a}{t_d}$, called the overhead factor (OF). It describes the additional latency of the memory unit or amplifier over the latency of the small combinational circuit.

5.3 Loss

For simplicity, we take the critical path, which has the longest latency, in order to do the following calculation. Assume each logic bit (one or more gates per bit) on average will have latency of t_g, and will encounter loss of α (in dB units). The memory unit or the amplifier is able to provide gain of G (in dB units). Therefore, if there are M bits in this critical path in each combinational logic circuit, then we have

$$G \geq M\alpha \tag{10}$$

$$t_d = Mt_g \tag{11}$$

Then we obtain a constraint for the overhead factor

$$k = \frac{t_a}{t_d} \geq \frac{\alpha t_a}{Gt_g} \tag{12}$$

Given the four parameters, the delay and loss of each bit along with the delay and gain of the memory unit or amplifier, we are easily able to know the overhead factor and thus the latency ratio and throughput ratio. Table 1 is a summary of all the symbols discussed.

6. Result

Fig. 5 shows the latency ratio (LR) and throughput ratio (TPR) versus the number of pipeline stages. It is worth mentioning that in the electronics domain, the pipeline stage depth ranges from a few to 30 or so, and sometimes over a thousand in some special applications [49]. In the Fig. 5, different curves represent different overhead factors k. It shows that the smaller the overhead factor is, the better the throughput improvement will we achieve at the cost of a little latency increase. For example, with the overhead factor of 0.5, then 20.3 times improvement of throughput will be seen while the latency ratio is only less than 1.5.

Some assumptions are then made to show a vivid comparison between the logic circuits with pipelining and those without pipelining. Table 2 shows four cases where the pipeline stages are either 10 or 30, and the amplifiers are either based on foundries' semiconductor optical amplifier

TABLE 1
Symbols and Definitions

Symbols	Definition
t_{dc}	The propagation latency of a combinational circuit
t_d^i	$i = 1,2,\cdots N$. The propagation latency of each small combinational circuit.
t_d	$t_d = \max\{t_d^i\}, i = 1,2,\cdots N$
t_{si}	The setup time of a combination circuit
t_{pd}	The setup time of a photodetector
t_{sr}	The setup time of a memory unit
t_{qr}	The clock-to-output delay of a memory unit
t_{ri}	The setup time of an electrical register
t_{ro}	The clock-to-output delay of an electrical register
t_a	The total delay of an amplifier
L_c	Total latency of a combinational circuit
L_s	Total latency of a sequential circuit
LR	Latency ratio of the entire circuit w/ and w/o pipeline
TP_c	Total throughput of a combinational logic circuit
TP_s	Total throughput of a sequential logic circuit or amplified sequential logic circuit
TPR	Throughput ratio of the entire circuit w/ and w/o pipeline
k	Overhead factor; $k = t_a/t_d$
N	Pipeline stages of a sequential circuit
M	number of bits in critical path in each combinational circuit
α	Loss of each bit, dB unit
t_g	Latency of each bit
G	Gain of the memory unit or amplifier, dB unit

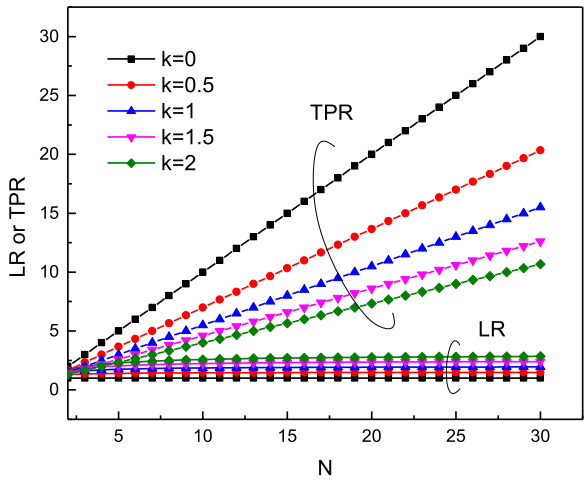


Fig. 5. The latency ratio (LR) and throughput ratio (TPR) with respect to the pipelining stage depth *N* for different overhead factors.

TABLE 2
Examples of the Specifications Based on Different Assumptions

	Parameter	Symbols	Unit	Specs with amplifiers		Specs with OEO	
Logic circuit characteristics	Loss per bit	α	dB	0.5		0.5	
	Latency per bit	t_g	ps	0.5		0.5	
Register characteristics	Gain	G	dB	20		~10	
	Latency	t_a	ps	20		~100	
Result with pipeline	Overhead factor	k		1		10	
	# of bits	M		40		20	
	Pipeline stage	N		**N=10**	**N=30**	**N=10**	**N=30**
	# of total bits	$M \times N \times 64$		25600	76800	12800	38400
	Throughput improvement	TPR		5.5	15.5	1.8	3.64
	Latency increase	LR		1.77	1.91	5.25	8.13
	Highest clock rate		GHz	25	25	9.1	9.1
	Loss		dB	20	20	10	10
Result w/o pipeline	Highest clock rate		GHz	4.55	1.61	4.55	1.61
	Loss		dB	180	580	90	290

(SOA) [50] or upon Soref's OEO [47]. Take the case of $N = 30$ and the ideal one as an example. The logic circuit is assumed to have 0.5 dB loss per bit and 0.5 ps latency per bit on average. The amplifier is able to provide 20 dB gain and introduces only $<$20 ps into the system [50]. Then we know that the maximum count of the bits in a critical path for each combinational circuit is 40 and the overhead factor is 1. Then we can obtain the data of TPR and LR from Fig. 5, which turn out to be 15.5 and 1.91, respectively at $k = 1$. It means that using pipelining will provide 15.5 times improvement in the throughput and only has less than 2 times latency increase. The circuit is able to run at a frequency as high as 25 GHz and the loss is 20 dB at the photodetector because amplifiers will boost the signals at each stage except the last one. On the contrary, the circuit without pipelining will suffer from 580 dB loss in total and can only run at 1.61 GHz. Assume the combinational circuit has 64-bit input and output ports in a processor with 64-bit data and address bus. Then the total count of bits is estimated to be 76800. Note that, thanks to the rapid development of integrated photonics, the components such as PDs and EOMs are able to provide an OE/EO bandwidth larger than 40 GHz [42], [51], [52]. Compared to the speed calculated in Table 2, the components bandwidth will not be the bottleneck. This approach provides a promising solution for EPDC to cascade tens of thousands of logic gates while still running at a very high clock rate.

Besides the loss and latency discussed above, there are other factors that should be considered in a real circuit. One example is the amplified spontaneous emission (ASE) from the amplifiers in ASL. As the number of amplifiers in Fig. 3 is increased, the optical signal quality measured by the signal noise ratio (SNR) will deteriorate due to the presence of noise amplified by each amplifier, which will put an upper boundary on the pipelining stage as well. Given the attenuation of each stage is A, the gain of each amplifier is G, and the ASE noise power of each stage is P_{ASE}, we can write the signal and noise output power as [53]:

$$P_s = P_{in} \prod_{i=1}^{N} A_i G_i \tag{13}$$

$$P_n = P_{ASE} \left(\sum_{j=1}^{N-1} \prod_{i=j}^{N-1} A_i G_i + 1 \right) \tag{14}$$

Assuming $A_i\ G_i = 1$, we have

$$SNR = \frac{P_s}{P_n} = \frac{P_{in}}{NP_{ASE}} \tag{15}$$

which indicates that the SNR will decrease with respect to the stage number. With all these parameters considered, this equation will give a requirement for the laser input and the amplifiers. For example, in the case where the input power is 10 dBm, the attenuation and gain of each stage are both 20 dB, we know from [54] that the ASE noise power will be less than -30 dBm. As a result, the SNR will still be larger than 25 dB even after 30 stages, which indicates that the ASE noise will not be the bottleneck in this case. The optical SNR for the OEO is generally higher than that of the SOA because the SOA gives an ASE noise not found in the OEO.

7. Conclusion

We have proposed optical sequential logic and amplified sequential logic together with pipelining to tackle with the latency and loss issues that the electronic-photonic digital computing will face when its circuit size scales up to include numerous components in order to achieve much more complex functions. The analysis shows that, with the help of pipelining, the electronic-photonic circuits could have multiple times of computing throughput improvement at the cost of a very small latency increase. Pipelining and optical amplifiers also enable the circuits to operate at a much higher clock rate, while at the same time easing the problem of propagation loss. Sequential logic and pipelining open up the possibility of very-large-scale electronic-photonic digital computing circuits.

References

[1] R. Soref, "The past, present, and future of silicon photonics," *IEEE J. Sel. Top. Quantum Electron.*, vol. 12, no. 6, pp. 1678–1687, Nov./Dec. 2006.
[2] D. A. B. Miller, "Device requirement for optical interconnects to silicon chips," *Proc. IEEE Spec. Issue Silicon Photon.*, vol. 97, no. 7, pp. 1166–1185, Jul. 2009.
[3] D. Miller, "Optical interconnects to electronic chips," *Appl. Opt.*, vol. 49, no. 25, pp. F59–F70, 2010.
[4] H. Subbaraman *et al.*, "Recent advances in silicon-based passive and active optical interconnects," *Opt. Express*, vol. 23, no. 3, pp. 2487–2510, 2015.
[5] P. Absil *et al.*, "Reliable 50 Gb/s silicon photonics platform for next- generation data center optical interconnects," in *Proc. IEEE Int. Electron. Devices Meet.*, 2017, pp. 761–764.
[6] M. Wade *et al.*, "A bandwidth-dense, low power electronic-photonic platform and architecture for multi-tbps optical i/O," in *Proc. Eur. Conf. Opt. Commun.*, 2018, pp. 1–3.
[7] A. H. Atabaki *et al.*, "Integrating photonics with silicon nanoelectronics for the next generation of systems on a chip," *Nature*, vol. 556, no. 7701, pp. 349–354, 2018.
[8] R. T. Chen *et al.*, "Fully embedded board-level guided-wave optoelectronic interconnects," *Proc. IEEE*, vol. 88, no. 6, pp. 780–793, Jun. 2000.
[9] D. A. B. Miller, "Attojoule optoelectronics for low-energy information processing and communications," *J. Light. Technol.*, vol. 35, no. 3, pp. 346–396, Feb. 2017.
[10] J. Hardy and J. Shamir, "Optics inspired logic architecture," *Opt. Express*, vol. 15, no. 1, pp. 150–165, 2007.
[11] Z. Ying *et al.*, "Electronic-photonic arithmetic logic unit for high-speed computing," *Nat. Commun.*, vol. 11, no. 2154, pp. 1–9, 2020.
[12] L. Zhang *et al.*, "Demonstration of directed XOR/XNOR logic gates using two cascaded microring resonators," *Opt. Lett.*, vol. 35, no. 10, pp. 1620–1622, 2010.
[13] Z. Ying, C. Feng, Z. Zhao, R. Soref, D. Pan, and R. T. Chen, "Integrated multi-operand electro-optic logic gates for optical computing," *Appl. Phys. Lett.*, vol. 115, no. 17, 2019, Art. no. 171104.
[14] Y. Tian, L. Zhang, Q. Xu, and L. Yang, "XOR/XNOR directed logic circuit based on coupled-resonator-induced transparency," *Laser Photon. Rev.*, vol. 7, no. 1, pp. 109–113, 2013.
[15] Y. Tian *et al.*, "Proof of concept of directed OR/NOR and AND/NAND logic circuit consisting of two parallel microring resonators," *Opt. Lett.*, vol. 36, no. 9, 2011, Art. no. 1650.
[16] Q. Xu and R. Soref, "Reconfigurable optical directed-logic circuits using microresonator-based optical switches," *Opt. Express*, vol. 19, no. 6, Mar. 2011, Art. no. 5244.
[17] Y. Tian *et al.*, "Experimental demonstration of a reconfigurable electro-optic directed logic circuit using cascaded carrier-injection micro-ring resonators," *Sci. Rep.*, vol. 7, no. 1, 2017, Art. no. 6410.
[18] C. Qiu, X. Ye, R. Soref, L. Yang, and Q. Xu, "Demonstration of reconfigurable electro-optical logic with silicon photonic integrated circuits," *Opt. Lett.*, vol. 37, no. 19, pp. 3942–3944, 2012.
[19] Z. Ying *et al.*, "Silicon microdisk-based full adders for optical computing," *Opt. Lett.*, vol. 43, no. 5, pp. 983–986, 2018.

[20] Z. Ying *et al.*, "Automated logic synthesis for electro-optic logic-based integrated optical computing," *Opt. Express*, vol. 26, no. 21, 2018, Art. no. 28002.
[21] Z. Zhao, Z. Wang, Z. Ying, S. Dhar, R. T. Chen, and D. Z. Pan, "Optical computing on silicon-on-insulator-based photonic integrated circuits," in *Proc. IEEE Int. Conf. ASIC (ASICON)*, 2017, pp. 472–475.
[22] R. Wille, O. Keszocze, C. Hopfmuller, and R. Drechsler, "Reverse BDD-based synthesis for splitter-free optical circuits," in *Proc. 20th Asia South Pacific Des. Automat. Conf.*, 2015, pp. 172–177.
[23] C. Qiu, X. Ye, R. Soref, L. Yang, and Q. Xu, "Demonstration of reconfigurable electro-optical logic with silicon photonic integrated circuits," *Opt. Lett.*, vol. 37, no. 19, pp. 3942–3944, 2012.
[24] Y. Tian *et al.*, "Directed optical half-adder based on two cascaded microring resonators," *IEEE Photon. Technol. Lett.*, vol. 24, no. 8, pp. 643–645, Apr. 2012.
[25] L. Zhang *et al.*, "Electro-optic directed logic circuit based on microring resonators for XOR/XNOR operations," *Opt. Express*, vol. 20, no. 11, pp. 11605–11614, 2012.
[26] Z. Liu *et al.*, "On-chip optical parity checker using silicon photonic integrated circuits," *Nanophotonics*, vol. 7, no. 12, pp. 1939–1948, 2018.
[27] Z. Ying *et al.*, "Electro-optic ripple-carry adder in integrated silicon photonics for optical computing," *IEEE J. Sel. Top. Quantum Electron.*, vol. 24, no. 6, pp. 1–10, Nov./Dec. 2018.
[28] D. Gostimirovic and W. N. Ye, "Ultracompact CMOS-compatible optical logic using carrier depletion in microdisk resonators," *Sci. Rep.*, vol. 7, no. 1, 2017, Art. no. 12603.
[29] Y. Tian, L. Zhang, J. Ding, and L. Yang, "Demonstration of electro-optic half-adder using silicon photonic integrated circuits," *Opt. Express*, vol. 22, no. 6, 2014, Art. no. 6958.
[30] S. Lin, Y. Ishikawa, and K. Wada, "Demonstration of optical computing logics based on binary decision diagram," vol. 20, no. 2, pp. 22484–22490, 2012.
[31] R. Soref and J. Hendrickson, "Proposed ultralow-energy dual photonic-crystal nanobeam devices for on-chip n x n switching, logic, and wavelength multiplexing," *Opt. Express*, vol. 23, no. 25, pp. 32582–32596, 2015.
[32] Z. Ying *et al.*, "Automated logic synthesis for electro-optic logic-based integrated optical computing," *Opt. Express*, vol. 26, no. 21, pp. 28002–28012, 2018.
[33] C. Condrat, K. Priyank, and S. Blair, "Logic synthesis for integrated optics," in *Proc. 21st Ed. Great Lakes Symp. Great Lakes Symp.*, 2011, no. c, pp. 13–18.
[34] C. Wang *et al.*, "Integrated lithium niobate electro-optic modulators operating at CMOS-compatible voltages," *Nature*, vol. 562, pp. 101–104, 2018.
[35] W. Heni *et al.*, "Plasmonic IQ modulators with attojoule per bit electrical energy consumption," *Nat. Commun.*, vol. 10, no. 1, 2019, Art. no. 1694.
[36] C. Haffner *et al.*, "Low-loss plasmon-assisted electro-optic modulator," *Nature*, vol. 556, no. 7702, pp. 483–486, 2018.
[37] Y. Shen, N. C. Harris, S. Skirlo, D. Englund, and M. Soljačić, "Deep learning with coherent nanophotonic circuits," *Nat. Photon.*, vol. 11, no. July, pp. 189–190, Oct. 2017.
[38] M. N. Sakib *et al.*, "A 112 Gb/s all-silicon micro-ring photodetector for datacom applications," in *Proc. Opt. Fiber Commun. Conf. Exhib.*, pp. 1–3, vol. 3, Paper. Th4A.2, 2020.
[39] A. H. Atabaki *et al.*, "Integrating photonics with silicon nanoelectronics for the next generation of systems on a chip," *Nature*, vol. 556, no. 7701, pp. 349–354, 2018.
[40] C. Sun *et al.*, "Single-chip microprocessor that communicates directly using light," *Nature*, vol. 528, no. 7583, pp. 534–538, 2015.
[41] B. Snyder *et al.*, "Packaging and assembly challenges for 50G silicon photonics interposers," in *Proc. Opt. Fiber Commun. Conf. Expo. (OFC)*, pp. 1–3, 2018.
[42] E. Timurdogan, *et al.*, "APSUNY process design kit (PDKv3.0): O, C and L band silicon photonics component libraries on 300mm wafers," in *Proc. Opt. Fiber Commun. Conf. Exhib.*, 2019, pp. 1–3.
[43] A. Poustie, R. J. Manning, A. E. Kelly, and K. J. Blow, "All-optical binary counter," *Opt. Express*, vol. 6, no. 3, pp. 69–74, 2000.
[44] J. Wang, G. Meloni, G. Berrettini, L. Potì, and A. Bogoni, "All-optical binary counter based on semiconductor optical amplifiers," *Opt. Lett.*, vol. 34, no. 22, Art. no. 3517, 2009.
[45] K. L. Hall, J. P. Donnelly, S. H. Groves, C. I. Fennelly, R. J. Bailey, and A. Napoleone, "40-Gbit/s all-optical circulating shift register with an inverter," *Opt. Lett.*, vol. 22, no. 19, 1997, Art. no. 1479.
[46] R. P. Webb *et al.*, "All-optical binary pattern recognition at 42 Gb/s," *J. Light. Technol.*, vol. 27, no. 13, pp. 2240–2245, Jul. 2009.
[47] R. Soref, F. De Leonardis, Z. Ying, V. M. N. Passaro, and R. T. Chen, "Silicon-Based Group-IV O-E-O devices for gain, logic, and wavelength conversion," *ACS Photon.*, vol. 7, no. 3, pp. 800–811, 2020.
[48] K. Nozaki *et al.*, "Femtofarad optoelectronic integration demonstrating energy-saving signal conversion and nonlinear functions," *Nat. Photon.*, vol. 13, pp. 454–459, 2019.
[49] "Instruction pipelining," [Online]. Available: https://en.wikipedia.org/wiki/Instruction_pipelining
[50] M. Smit *et al.*, "An introduction to InP-based generic integration technology," *Semicond. Sci. Technol.*, vol. 29, no. 8, 2014, Art. no. 083001.
[51] J. Sun *et al.*, "A 128 Gb/s PAM4 silicon microring modulator," in *Proc. Opt. Fiber Commun. Conf. Expo. (OFC)*, 2018, pp. 1–3.
[52] D. Gostimirovic, F. De Leonardis, R. Soref, V. M. N. Passaro, and W. N. Ye, "Ultrafast electro-optical disk modulators for logic, communications, optical repeaters, and wavelength converters," *Opt. Express*, vol. 28, no. 17, 2020, Art. no. 24874.
[53] D. M. Baney, P. Gallion, and R. S. Tucker, "Theory and measurement techniques for the noise figure of optical amplifiers," *Opt. Fiber Technol.*, vol. 6, no. 2, pp. 122–154, 2000.
[54] M. J. Connelly, "Wideband semiconductor optical amplifier steady-state numerical model," *IEEE J. Quantum Electron.*, vol. 37, no. 3, pp. 439–447, Mar. 2001.