SET and RESET Pulse Characterization in BJT-Selected Phase-Change Memories

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Abstract - **This paper presents program pulse characterization in an 8-Mb BJT-selected Phase-Change Memory test chip. Experimental results of the impact of the bit-line resistance over programming pulses efficiency are provided. Furthermore, in order to compensate for spreads in cell physical parameters in an array portion, a non-conventional staircase-down program pulse is proposed and experimentally evaluated.**

I. INTRODUCTION

Today high-performance portable equipments demand for non-volatile memories featuring higher and higher read/write speed and endurance. Indeed, in recent years, more and more research efforts are being devoted in order to find a new technology able to overcome performance and scalability limits of currently dominant Flash memories. Phase-Change Memory (PCM) technology [1], [2] is one of the most promising candidates for the next generation of non-volatile memory devices. PCMs offer direct write (any bit can be independently reprogrammed with no need for block erasing), improved write throughput versus NOR-based memories and random access time versus NAND-based memories, as well as the potential to be scalable beyond Flash technology. Moreover, PCMs ensure high endurance and good compatibility with standard CMOS fabrication processes.

To limit overall reprogramming time, an attractive approach is to perform write and erase operations without resorting to program&verify and erase&verify techniques [3], [4]. It is therefore apparent that an experimental characterization of pulses used to carry out program operations is of vital importance. In this paper, program pulse characterization in an 8-Mb BJT-selected Phase-Change Memory test chip [5] is presented. In particular, experimental results of the impact of the bit-line resistance over programming pulses are provided. Furthermore, in order to compensate for spreads in cell physical parameters, a non-conventional staircase-down program pulse is proposed and experimentally evaluated.

II. PHASE-CHANGE STORAGE ELEMENT AND CHIP ARCHITECTURE

In PCMs, also referred to as Ovonic Unified Memories (OUMs), the storage device is made of a thin film of chalcogenide alloy (in our case, $Ge_2Sb_2Te_5$, GST). This material can reversibly change between an amorphous (high impedance, RESET state) and a polycrystalline (low impedance, SET state) phase when thermally stimulated, thus allowing information storage. The phase conversion of a storage element is obtained by appropriately heating (by means of electrical pulses applied to a suitable heater element) and then cooling a small, thermally isolated portion of the chalcogenide material. Once the chalcogenide material melts, it completely loses its crystalline structure. When rapidly cooled, the chalcogenide material is locked into its amorphous state (to this end, the cooling operation rate has to be faster than the crystal growth rate). To switch the memory element back to its crystalline state, the chalcogenide material is heated to a temperature between its glass transition temperature and its melting point temperature. In this way, nucleation and micro-crystal growth occur in tens of ns, thus leading to a (poly)crystalline state.

From above, it is apparent that the storage element can be modelled as a programmable resistor (high resistance = logic 0; low resistance = logic 1). Reading a cell basically consists in measuring the resistance of the addressed storage device. To this end, a predetermined voltage is forced across the storage element of the selected cell, and the resulting current flow is sensed.

Fig. 1 depicts a detail of the memory array integrated in our test-chip. A *pnp* Bipolar Junction Transistor (BJT) is employed as the cell selector in order to minimize silicon area occupation, and, hence, improve data storage density.

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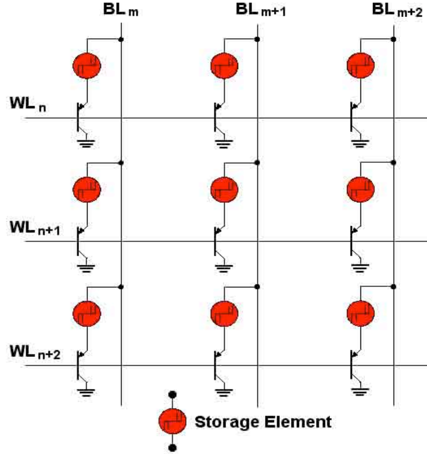

Figure 1 – Detail of the memory array.

A schematic diagram of the test chip array organisation is depicted in Fig. 2. The array is organized in two 4-Mb tiles (2048 word-lines by 2048 local bit-lines). A two-level hierarchical approach is adopted for bit-line driving: any main bit-line (implemented in metal2) feeds two local bit-lines (one per each tile) through respective local selectors Y_O, implemented by natural *n*-channel devices. The DC voltages required for the different operations of the array are provided through separate pins for better flexibility and observability. Program voltages VSET and VRESET, together with read voltage VREAD, are fed to the Operating Control (OC) block which, in turn, routes the required (pulsed by WE) voltage to the gates of the local selectors Y_O. VPCX and VA are the word-line and the column decoder supply, respectively. The power for the write operations is supplied by VA.

It is worth to underline that the bit-line resistance degrades program pulse efficiency since the current injected in cells far from the column selector is lower with respect to the current injected in cells near the selector [6]. The chosen hierarchical array configuration allows main bit-line resistance effects to be eliminated. This results in a similar behaviour of cells placed in the corresponding locations of the two tiles.

It is worth to point out that transistors Y_O (which operate in the saturation region) regulate the bit-line voltage to the required value during both reading and programming. In particular, the bit-line voltage turns out to be equal to $V_{G,YO} - (V_{th} + V_{ov})$, where $V_{G,YO}$, V_{th}, and V_{ov} are the gate biasing voltage, the threshold voltage including the body effect contribution, and the overdrive voltage, respectively, of transistors Y_O. In read mode, the chosen cascode bit-line biasing approach [7] allows fast bit-line precharge and sensing. It should also be pointed out that, during read operations, the bit-line voltage has to be adequately low, accurate, and stable in order not to disturb the state of the cell. In this respect, the adopted bit-line biasing technique prevents the risk of spurious SET pulses since the cascode structure rejects noise injection from the column decoder supply line VA.

It is apparent that, when SET and RESET operations are performed without resorting to program/verify and erase/verify techniques, very accurate electrical pulses have to be applied to the addressed bit-lines and, hence, to the selected cells. In write mode, a pulsed, regulated bit-line voltage is obtained by simply controlling the gates of selectors Y_O (no DC current drawing from the corresponding regulator is required).

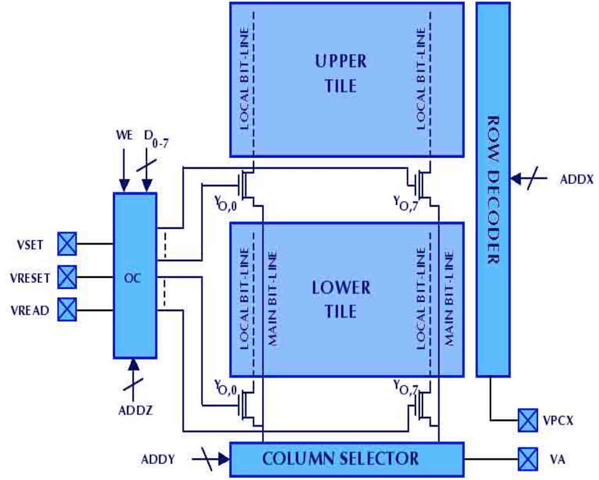

Figure 2 – Conceptual diagram of the test chip array: write path.

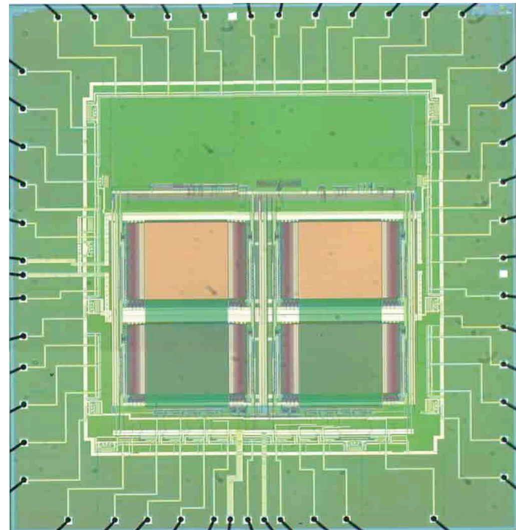

Figure 3 – Chip microphotograph.

III. Experimental Results and Discussion

The test chip was integrated by using a single-poly, single-well, 0.18-µm CMOS technology. Fig. 3 shows a chip microphotograph. Each tile is divided in two half tiles. The word-line decoder is placed vertically between the two left-side and the two right-side 2-Mb half tiles. In order to fit in a standard PAD frame configuration, large unused

areas are present in the chip periphery. The nominal supply voltage V_{CC} for logic is 1.8 V. VA was set to 4 V so as to correctly bias the column decoder during both read and program operations.

To characterize the impact of the bit-line resistance over programming pulse efficiency, the upper tile was considered. In this way, the effects of the resistance of a whole local bit-line resistance could be evaluated.

To assess the local bit-line resistance effect in the case of RESET pulses, the characterization has been focused on three different portions of the upper tile, one located at the top (word-lines 0 to 10, farthest cells, higher bit-line resistance), another in the middle (word-lines 1000 to 1010), and the last at the bottom (word-lines 2030 to 2040, nearest cells, lower bit-line resistance) of the array for a total cell count of 22528 in each portion (Fig. 4). To determine the optimum RESET voltages, 40-ns single-box pulses with different amplitude were applied to all cells in each of the considered array portions. After each RESET pulse (applied to cells previously programmed to the SET state), a readout operation has been performed until the required read criteria is obtained. The RESET voltage distributions have Gaussian shape whose peak values correspond to bit-line voltages shown in Fig. 5. It can be noted that, considering the current required for a RESET operation (600 µA [5]), the impact of the local bit-line resistance over the peak value of the distributions turns out to be about 300 mV.

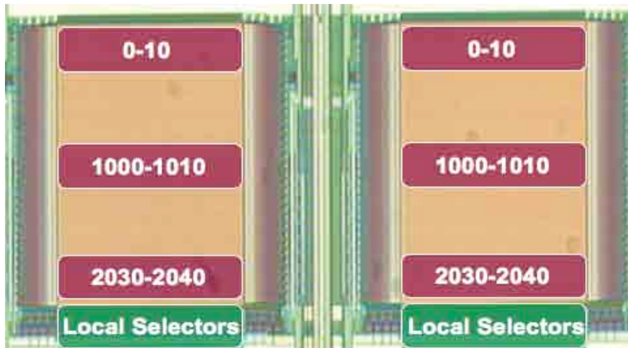

Figure 4 – Detail of the upper tile in which the array portions used for characterization and the local selectors are highlighted.

The above local bit-line resistance effect can hence be compensated by applying RESET pulses with a different amplitude properly assigned to different portions of the array (for example four portions with $\Delta V = 75$ mV). This approach allows obtaining substantially the same distributions for cells belonging to different array portions.

The same characterisation performed on the upper tile has been also carried out on lower tile. Fig. 6 depicts the peak values of RESET voltages Gaussian distributions associated to word-lines 2050 to 2060, 3000 to 3010, and 4080 to 4090. As expected, the observed local bit-line effect is substantially the same as seen on the upper tile.

The local bit-line resistance effect over SET operations has then been characterized. The spacing between the peak values of the distributions corresponding to word-lines 0 to 10 and 2030 to 2040 was now about 150 mV. This is in agreement with the expected value, since the cell current required for SET operation is 300 µA [5].

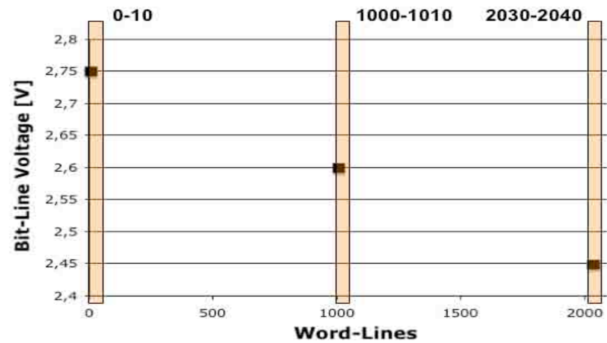

Figure 5 – Average RESET voltage as a function of word-line (upper tile).

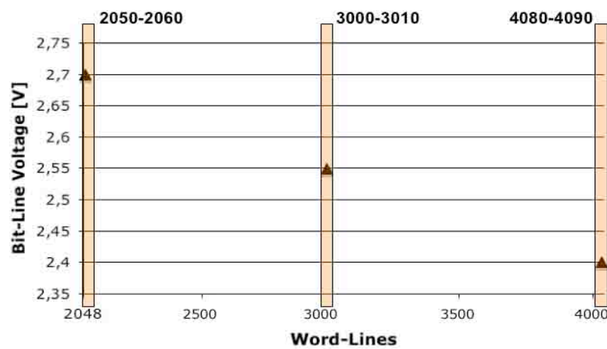

Figure 6 – Average RESET voltage as a function of word-line (lower tile).

A further characterisation on different SET pulse lengths has been then carried out, by using the array portion corresponding to word-lines 0 to 10. Fig. 7 depicts the number of SET cells obtained with 50-ns, 150-ns, 250-ns, and 500-ns single-box SET pulses having different amplitudes together with the number of RESET cells achieved by applying 40-ns RESET single-box pulses with different amplitudes. An overlap of about 400 mV is visible between the two set of curves. This is due to the spread in cell physical parameters in the considered array portion. Indeed, on the one hand, for each SET box pulse length, cells belonging to the same array portion require different optimum voltage to switch from the RESET to the SET state. On the other hand, for each SET voltage, cells belonging to the same array portion require different minimum SET box pulse length to switch from the RESET to the SET state. From Fig. 7, an adequate SET window is obtained only for 250-ns and 500-ns single-box pulses. By using a 50-ns pulse, the SET voltage that would be required to SET the whole distribution would unfortunately be enough to cause RESET in some of them. The 150-ns pulse results in a marginal situation, at least with the criteria of a robust 10 µA read window. It is apparent that this adversely affects programming speed, and, hence, write throughput.

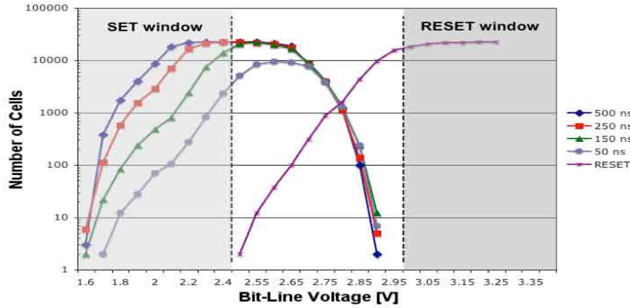

Figure 7 –Number of SET and RESET cells.

This drawback can be overcome by applying a staircase-down SET pulse [8], which consists in the sequence of two or more box pulses having the same length T_S and a decreasing amplitude, S_1, S_2, and S_3, respectively (Fig. 8).

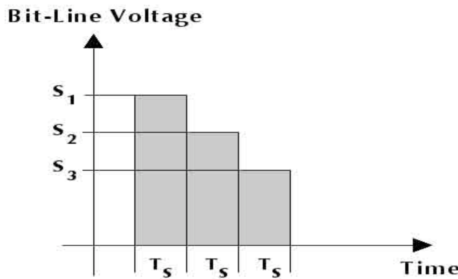

Figure 8 – Staircase-down SET pulse.

Staircase-down SET pulses allow different SET voltages to be applied to cells belonging to the same array portion. This means that some cells will switch to the SET state for voltage S_1, some other cells for voltage S_2 and, finally, some other cells for S_3. For better understanding this programming approach, it has to be considered that each cell has specific optimum SET and RESET voltages, which are adequately spaced from each other. By applying decreasing subsequent program pulses there is no risk to RESET a cell that has been set by a previous pulse. It has also to be pointed out that SET process is cumulative. This means that, even though optimum SET voltage is not applied to some cells, these exploit the cumulative SET effect of the previous and the subsequent program pulse to switch from the RESET to the SET state. In order to apply the optimum SET voltages for different cells in the considered array portion, the adequate pulse length T_S, together with the best voltage difference $S_1 - S_3$, and the best voltage step $S_1 - S_2$ have to be determined. This programming approach allows enlarging the SET window by using also SET voltages (first step), which are in the SET/RESET overlap voltage region, as shown conceptually by the arrow in Fig. 9.

This programming approach has been experimentally characterized, by using an external waveform generator to provide the staircase-down pulse to VSET pin. The staircase-down program pulse can be easily generated on-chip by means of an adequate programmable voltage regulator. The optimum staircase-down SET pulse was obtained by setting T_S equal to 50 ns, and S_1, S_2, and S_3 equal to 2.7 V, 2.55 V, and 2.4 V, respectively. The overall SET pulse length was, therefore, 150 ns. Under such program conditions, all cells of the considered array portion switched from the RESET to the SET state with the required read margin.

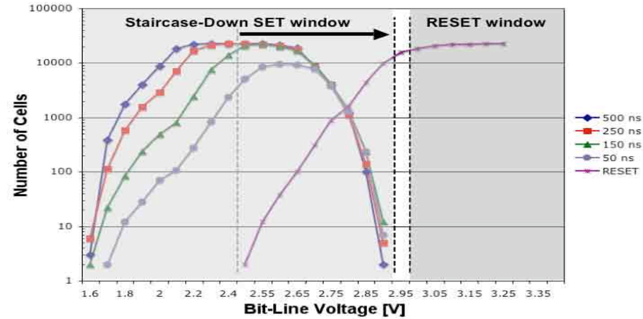

Figure 9 – Effect of staircase-down SET pulse.

IV. Conclusions

In this paper, program pulse characterization in an 8-Mb BJT-selected Phase-Change Memory test chip has been presented. Experimental results of the impact of the bit-line resistance over programming pulses have been provided. To compensate for spreads in cell physical parameters, a non-conventional staircase-down program pulse has been proposed and experimentally evaluated.

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