SEU-Hardened Energy Recovery Pipelined Interconnects for On-Chip Networks

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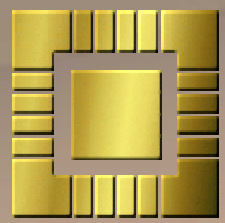
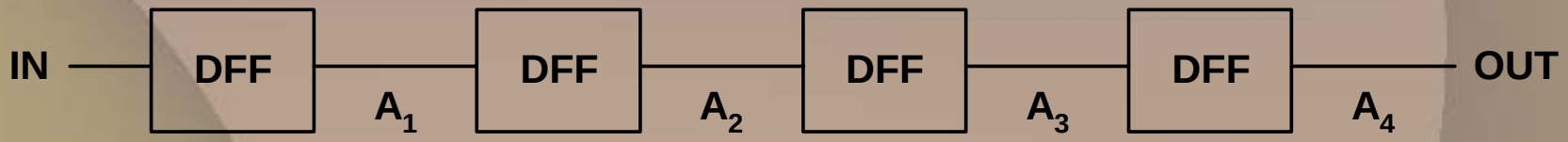


Overview

- Introduction
  - Pipelined On-Chip Interconnects
  - Addressed Problem
- Energy Recovery Circuits
- Energy Recovery Pipelined Interconnects
  - Proposed Designs
- Experiments

Pipelined On-Chip Interconnects



- Increased throughput
- Freedom in choosing arbitrary topologies
  - Pipelining decouples the throughput from the interconnect length.

Addressed Problem

- Reliability of on-chip interconnects
  - In DSM technologies, flip-flops are susceptible to SEUs.
- Energy consumption of on-chip interconnects
  - Up to 50% of the total on-chip energy
  - SEU tolerance and low energy are at odds.
- **In this work:** Specialized *energy recovery* designs to achieve both the above objectives at the same time

Previous Works

1) Energy recovery techniques for long wires

- Voss et al., 2000.
- Lyuboslavsky et al., 2000.

These works have not considered:

- reliability issues
- pipelined interconnects

2) Traditional Energy Recovery Logic Styles

- Eight-phase dual-rail logic
- 2LAL

They are not suitable for pipelined on-chip interconnects.

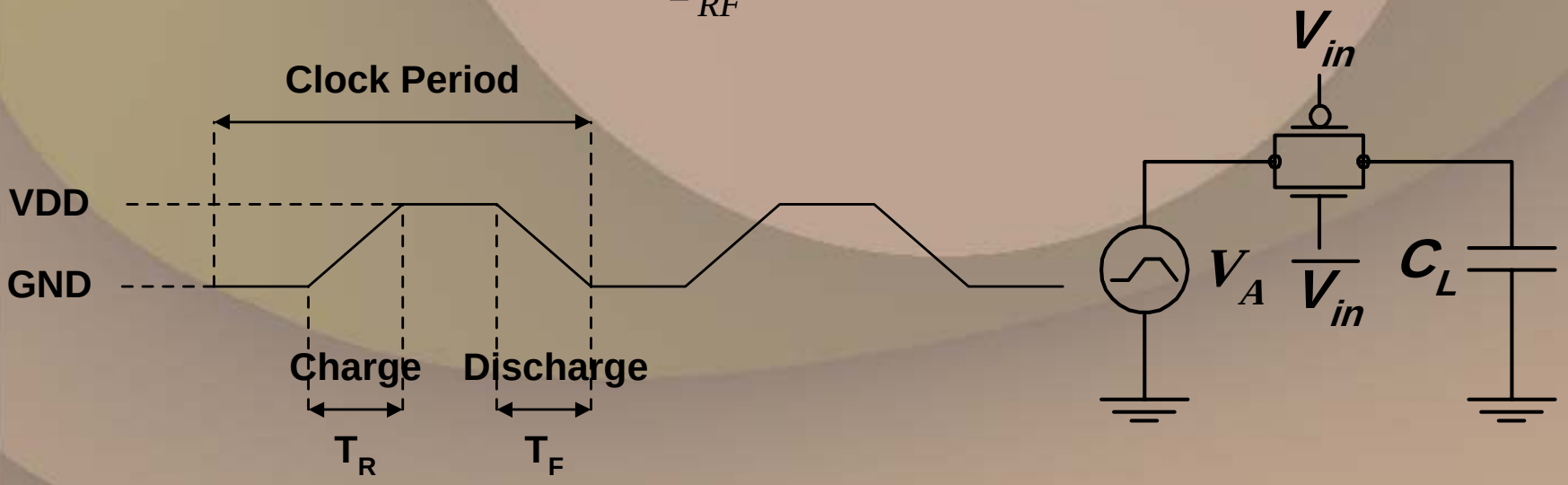
The Principle of Energy Recovery

- Conventional CMOS gates (Constant voltage charging)

$$E_{Conv} = \frac{1}{2} C_L V_{DD}^2$$

- Energy recovery CMOS gates (Constant current charging)

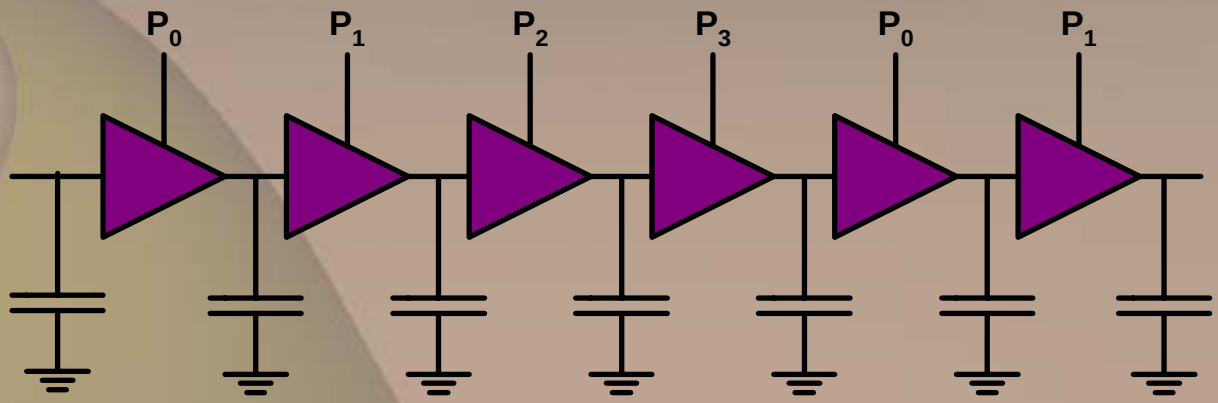
$$E_{Cons-Cur} = \left(\frac{RC_L}{T_{RF}}\right) C_L V_{DD}^2$$



Characteristics of Energy Recovery Circuits

- The trapezoidal signals provide
  - Operating power
  - Timing information (power-clocks)
- Essentially pipelined sequential circuits
- Multiphase trapezoidal power-clock signals
- Reversible logic functions

Energy Recovery Pipelined Interconnects



$$C_{Stage} = \frac{1}{n+1} \cdot C_L$$

- Constant current charging of the non-pipelined interconnect

$$E_{non-pipelined} = \frac{RC_L}{T_{RF}} C_L V_{DD}^2$$

- Constant current charging of the pipelined interconnect

$$E_{Stage} = \frac{RC_{Stage}}{T_{RF}} C_{Stage} V_{DD}^2 \Rightarrow E_{pipeline}(n) = (n+1) E_{Stage} = \frac{1}{n+1} \cdot \left[\frac{RC_L}{T_{RF}} C_L V_{DD}^2 \right]$$

Energy Saving via Pipelining

- Conventional pipelined interconnects:
  - Depth of pipelining$\Uparrow \Rightarrow$ Throughput$\Uparrow$
- Energy recovery pipelined interconnects:
  - Depth of pipelining$\Uparrow \Rightarrow$ Throughput$\Uparrow$
    - T_{RF} decreases
  - Depth of pipelining$\Uparrow \Rightarrow$ Energy consumption$\Downarrow$
    - T_{RF} remains unchanged

Proposed Designs

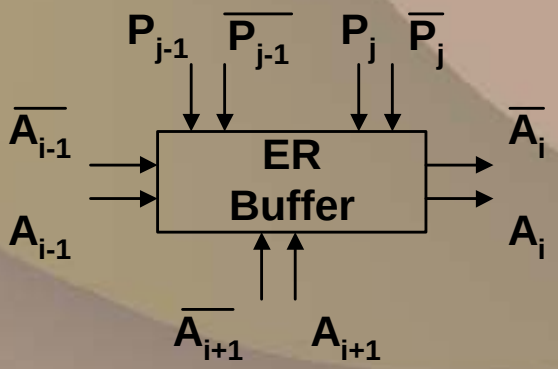
- ER
  - Energy Recovery Pipelined Interconnects
    - Energy Saving: 50%
    - Reliability: Slightly less reliable than conventional pipelines
- SHER
  - SEU-Hardened and Energy Recovery Pipelined Interconnects
    - Energy Saving: 30%
    - Reliability: Considerably hardened against SEUs

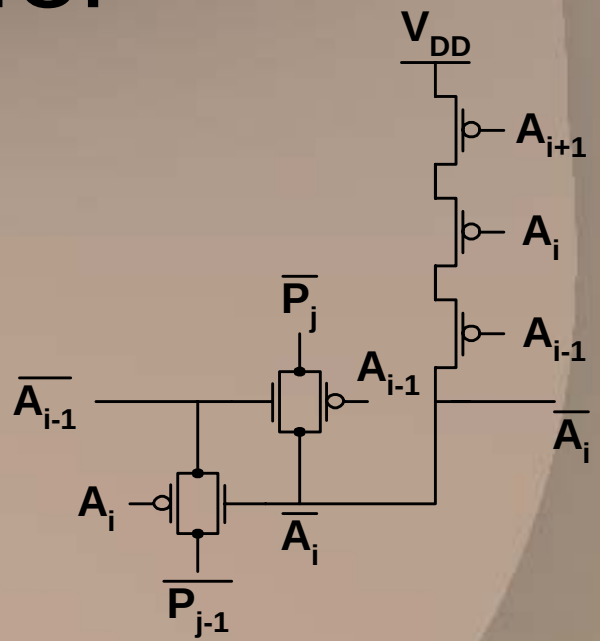
Disadvantages of Traditional Energy Recovery Logic Styles

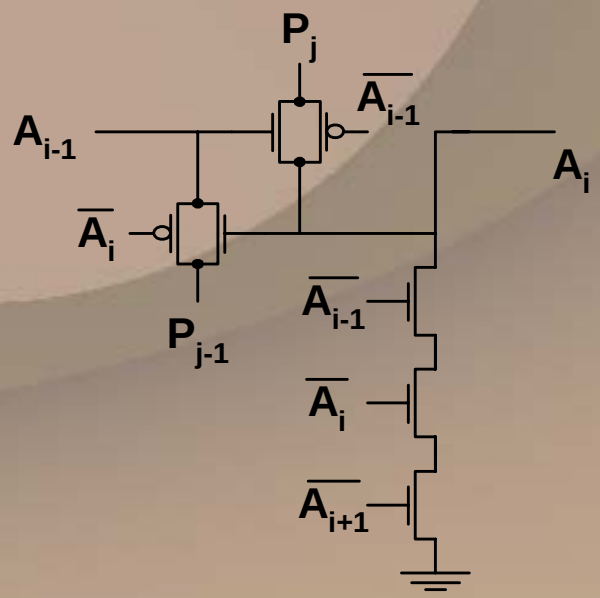
- Eight-phase dual-rail logic
  - 8 power-clock signals
- 2LAL
  - Floating nodes
  - Problems in DSM technologies
- SEU-Hardness has not been considered

ER Buffer

- Dual-rail logic
- 4 power-clocks
- Circuit parts:
  - Transmission gates
  - Transistor stack

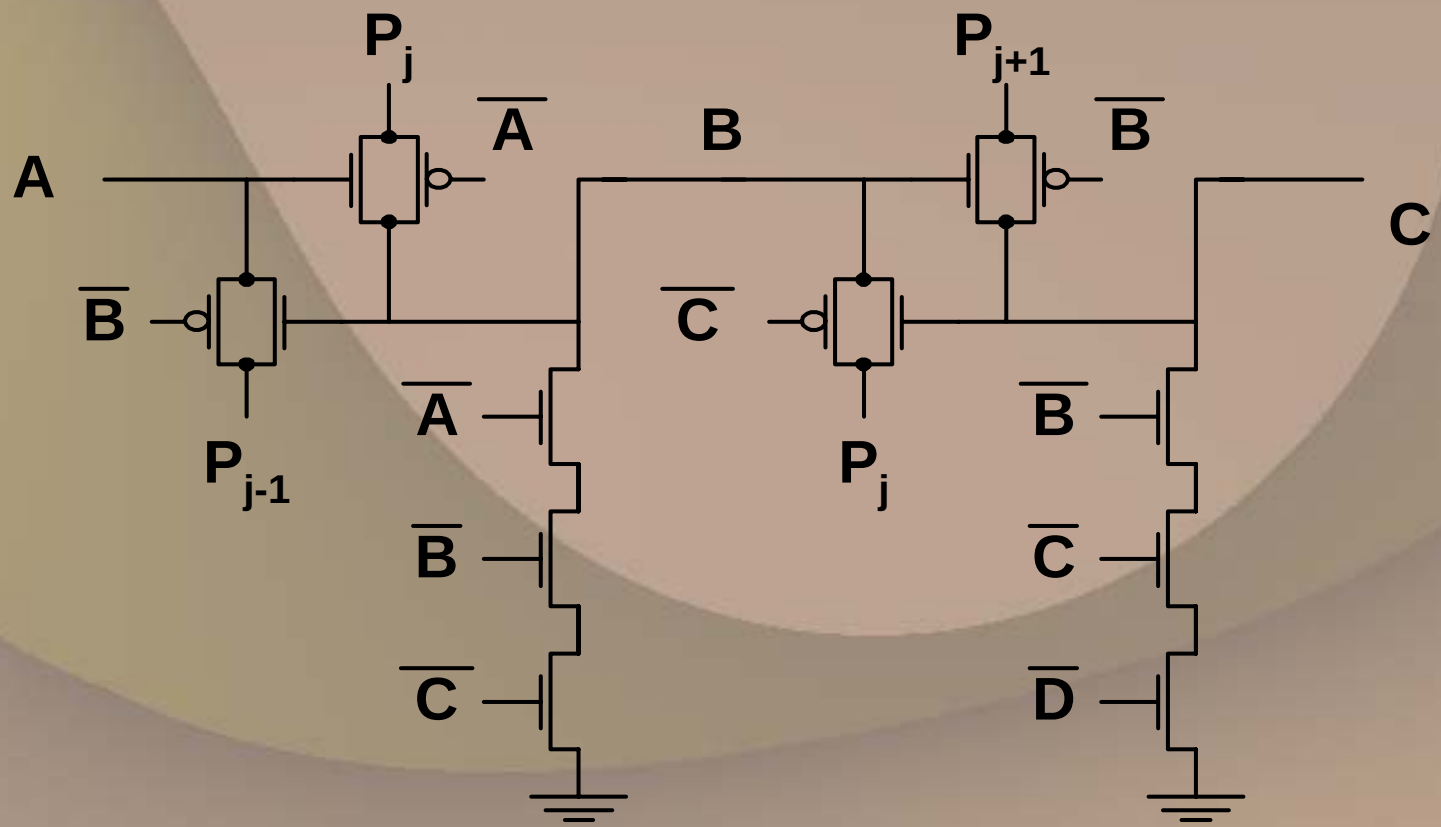




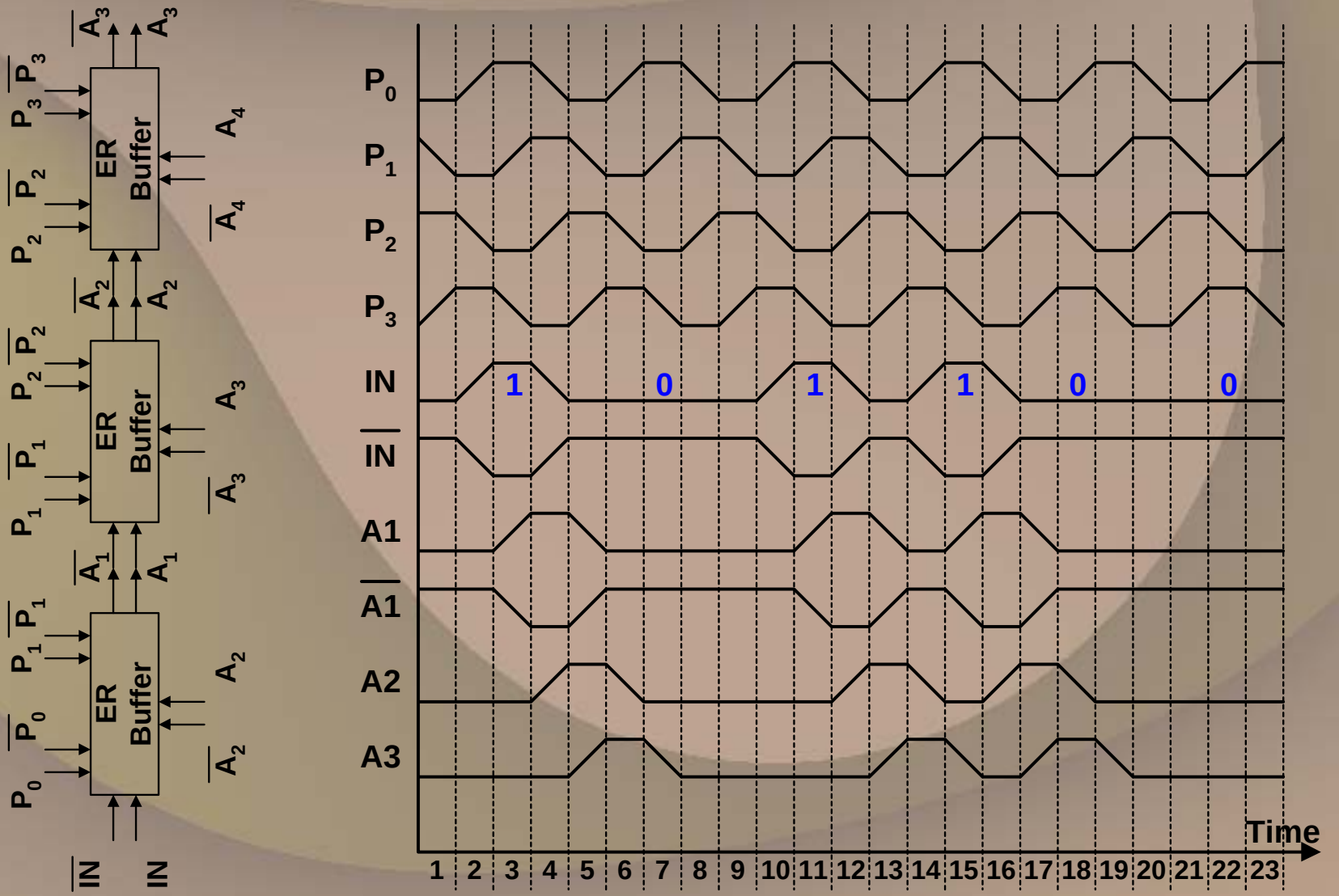


Clamp Transistor Stack

- Two consecutive buffers

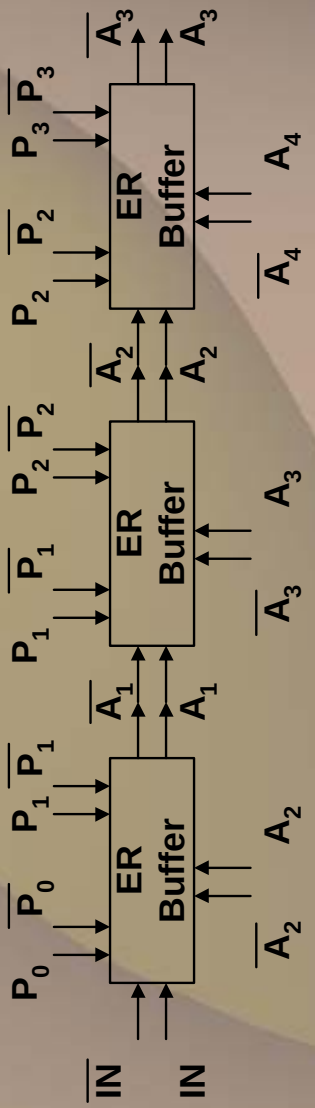


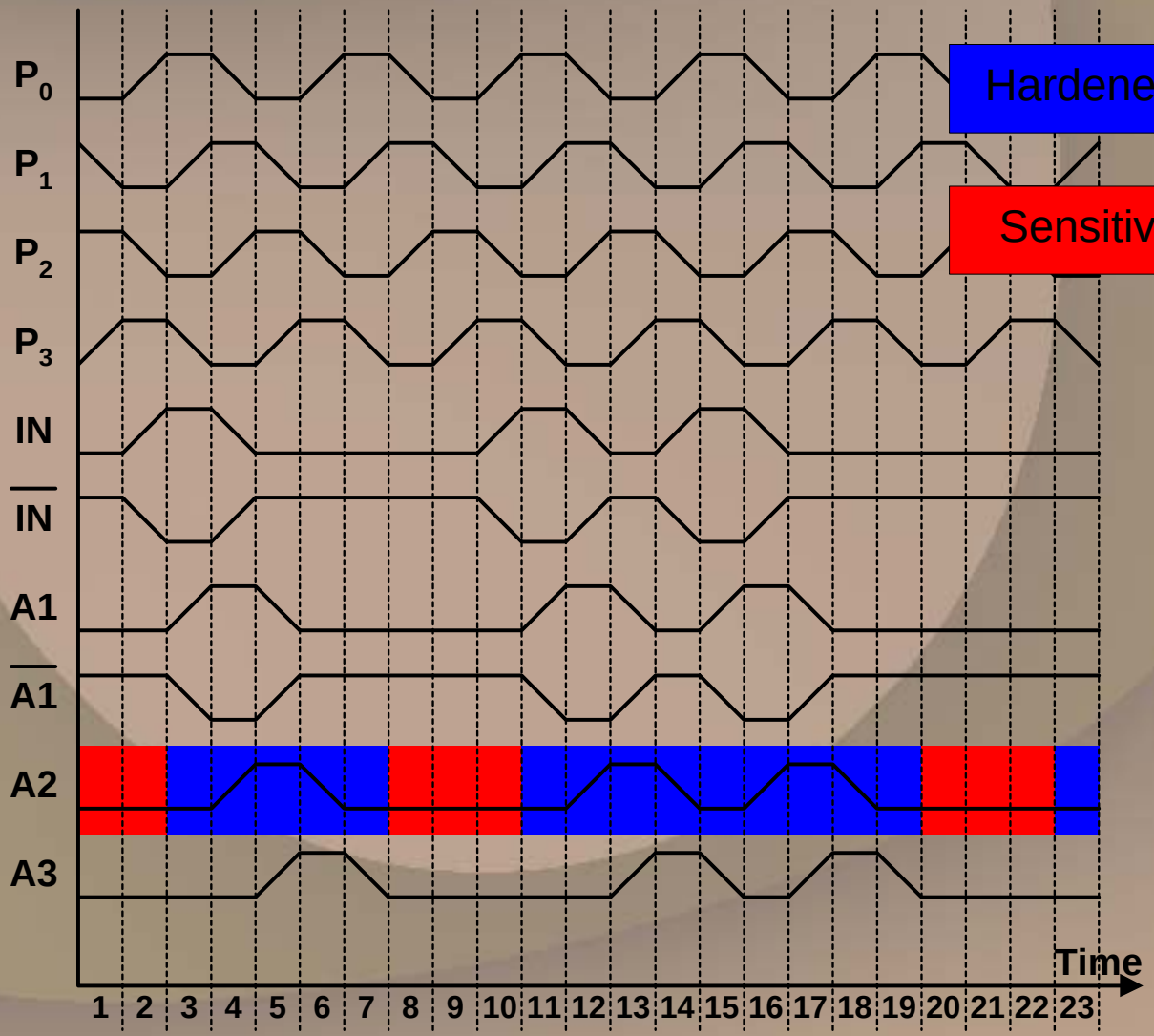
ER Pipelined Interconnects



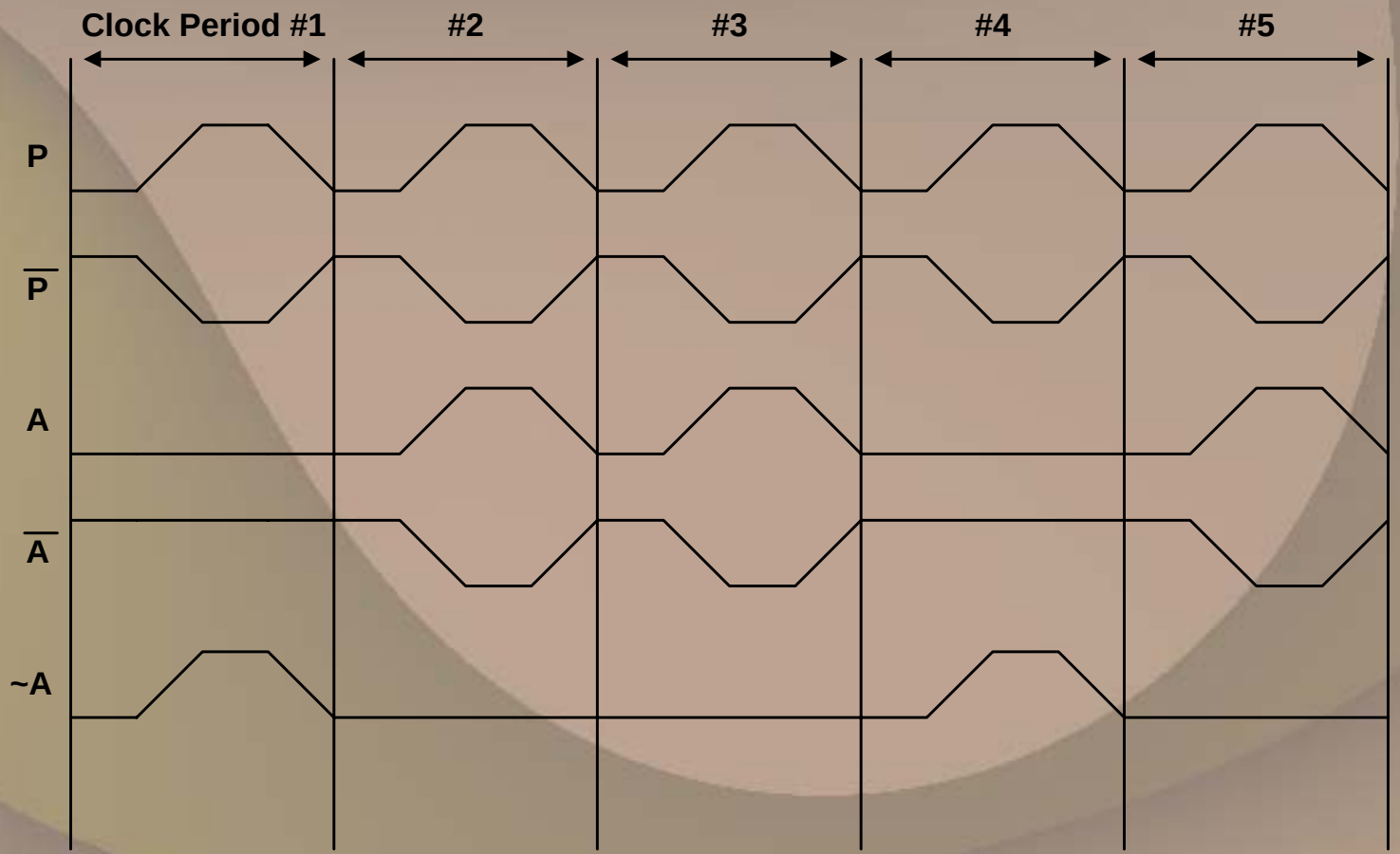
A detailed example in Pages 4 and 5 of the paper

SEU-Hardness





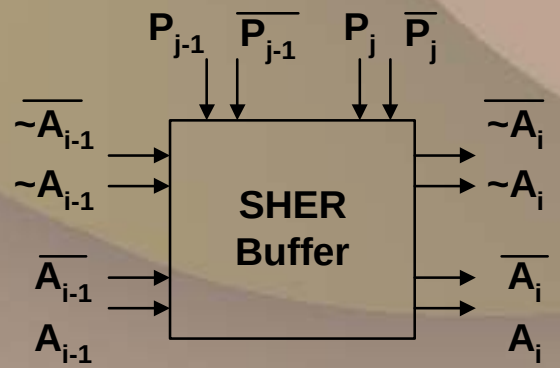
Voltage Inverse *vs.* Logical Inverse

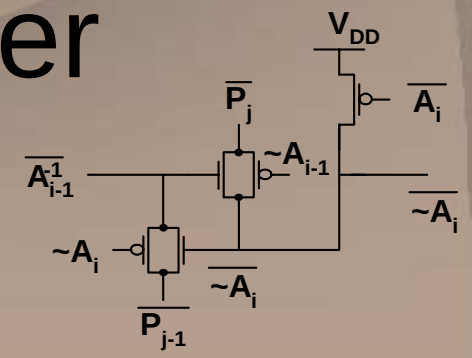


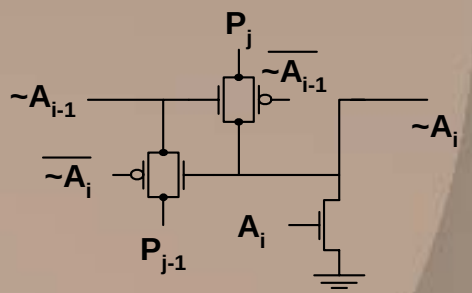
$\overline{A}$ = voltage inverse of A, ~A=logical inverse of A

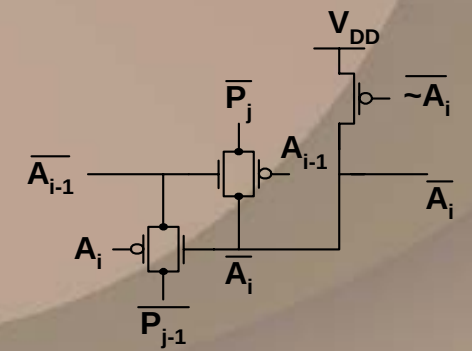
SHER Buffer

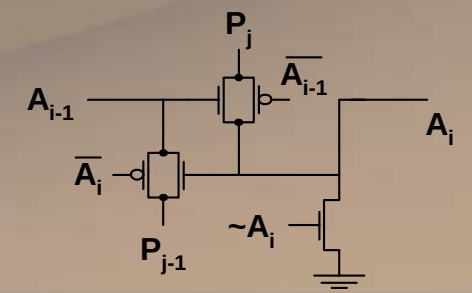
- 4-rail logic
- 4 power-clocks
- Circuit parts:
  - Transmission gates
  - Clamp transistor



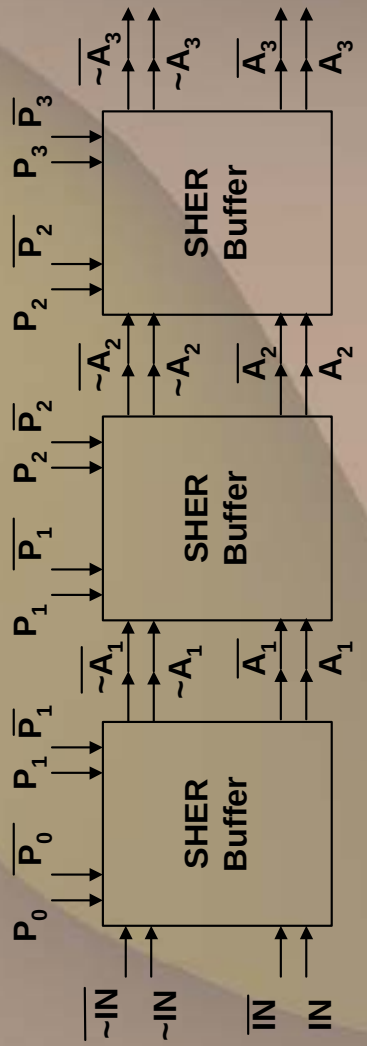


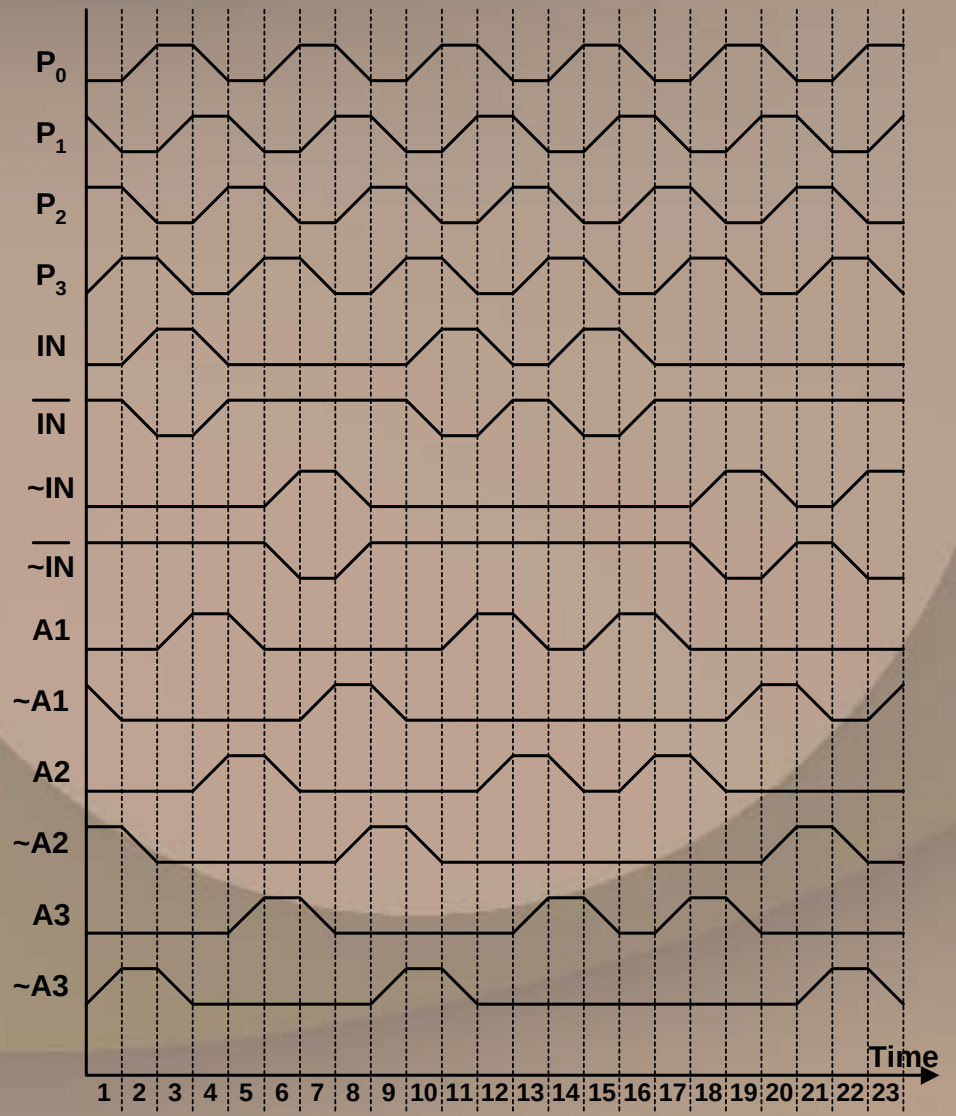






SHER Pipelined Interconnects

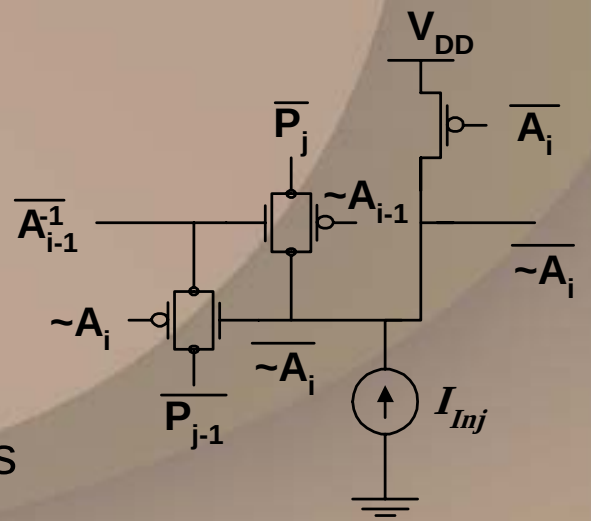




A detailed example in Pages 6, 7 and 8 of the paper

Experimental Evaluation

- SPICE simulations
  - 45nm PTM technology
- Interconnect
  - C_L=1pF
    - About 5 millimeters long wire in 45nm technology
  - Throughput = 0.1 Gbps
- Estimating energy consumption
  - A random bit string consisting of 120 bits
- Estimating reliability against SEUs
  - Faults were injected using current sources



$$I_{Inj}(t) = \frac{2}{\sqrt{\pi}} \cdot \frac{Q}{T} \cdot \sqrt{\frac{t}{T}} \cdot e^{-\frac{t}{T}}$$

Energy Consumption of Pipelined On-Chip Interconnects

Pipelining Scheme	# of FFs or # of Buffers	Average Power (uW)	Energy consumption*(pJ)
Conventional	3 FFs	11.90	14.28
	4 FFs	12.14	14.57
	5 FFs	12.42	14.91
ER	12 BUFs	7.42	8.90
	16 BUFs	6.36	7.63
	20 BUFs	5.56	6.67
SHER	12 BUFs	11.22	13.47
	16 BUFs	9.62	11.54
	20 BUFs	8.41	10.09

* The energy consumption when a bit string with 120 random bits is transmitted

Results Obtained From the Fault Injection Experiments

Pipelining Scheme	# of FFs or # of Buffers	# of SEUs	% of SEUs*
Conventional	3 FFs	377	9.2
	4 FFs	618	15.08
	5 FFs	792	19.33
ER	12 BUFs	502	12.26
	16 BUFs	816	19.92
	20 BUFs	844	20.61
SHER	12 BUFs	0	0
	16 BUFs	0	0
	20 BUFs	2	0.05
* 4096 faults (simulated particle strikes) were totally injected			

Summary

- We have proposed the use of energy recovery techniques to construct low energy and reliable pipelined on-chip interconnects.

- We have presented two energy recovery designs:
  - ER
    - Energy Saving: 50%
    - Reliability: Slightly less reliable than conventional pipelines
  - SHER
    - Energy Saving: 30%
    - Reliability: Considerably hardened against SEUs

Future Works

- Analyzing the use of frequency scaling:

$$E_{Cons-Cur} = (\frac{RC_L}{T_{RF}})C_L V_{DD}^2$$

- Analyzing the throughput/energy trade-off
  - Depth of pipelining$\Uparrow \Rightarrow$ Throughput$\Uparrow$
    - T_{RF} decreases
  - Depth of pipelining$\Uparrow \Rightarrow$ Energy consumption$\Downarrow$
    - T_{RF} remains unchanged

Thank You