

SEU-Sensitive Volumes in Bulk and SOI SRAMs From First-Principles Calculations and Experiments

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Abstract—Large-scale three-dimensional (3-D) device simulations, focused ion microscopy, and broadbeam heavy-ion experiments are used to determine and compare the SEU-sensitive volumes of bulk-Si and SOI CMOS SRAMs. Single-event upset maps and cross-section curves calculated directly from 3-D simulations show excellent agreement with broadbeam cross section curves and microbeam charge collection and upset images for 16 K bulk-Si SRAMs. Charge-collection and single-event upset (SEU) experiments on 64 K and 1 M SOI SRAMs indicate that drain strikes can cause single-event upsets in SOI ICs. 3-D simulations do not predict this result, which appears to be due to anomalous charge collection from the substrate through the buried oxide. This substrate charge-collection mechanism can considerably increase the SEU-sensitive volume of SOI SRAMs, and must be included in single-event models if they are to provide accurate predictions of SOI device response in radiation environments.

I. INTRODUCTION

SOFT errors (also known as single-event upsets) due to α -particles and cosmic ray neutrons are a growing problem for terrestrial memory and digital logic integrated circuits (ICs) as technology scaling leads to decreased cell capacitance and operating voltage [1]–[3]. Increased usage of flip-chip packaging, growing numbers of metallization levels, and the presence of boron-rich compounds exacerbate the problem [2], [4]. Meanwhile, soft errors have been a concern for many years for ICs operating in space environments. To improve soft error immunity, manufacturers of radiation-hardened ICs may use feedback elements (e.g., resistors, capacitors) to slow the propagation of voltage transients, at the expense of performance [5]. Other techniques to decrease soft error sensitivity include circuit design techniques that lead to increased transistor counts and layout area [6], [7]. While these techniques are quite effective, manufacturers of commercial ICs have been willing to implement them only on a very limited basis due to area and speed penalties [8], [9]. A more fundamental method for hardening against single-event upsets (SEUs) is to reduce the SEU-sensitive volume. This can be accomplished through the use of silicon-on-insulator (SOI) substrates, for example [10]. It is therefore important to understand the differences between SEU-sensitive regions in bulk and SOI technologies.

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In this paper we use large-scale 3-D device simulations, focused ion microscopy, and broadbeam heavy-ion experiments to determine and compare the SEU-sensitive volumes of bulk-Si and SOI CMOS SRAMs. The simulations include upset maps and upset cross section curves calculated directly from first principles with no prior assumptions of the sensitive area. Calculated heavy ion upset cross sections are compared to broadbeam heavy ion measurements on 16 K and 256 K bulk CMOS SRAMs fabricated at Sandia. Simulated charge-collection and upset maps for the 16 K bulk SRAM memory array are directly compared to equivalent maps obtained using a focused ion microprobe. Charge-collection and SEU experiments are performed on 64 K and 1 M SOI CMOS SRAMs fabricated at Sandia. Surprisingly large SEU-sensitive volumes in SOI SRAMs are discovered and possible mechanisms responsible for anomalous charge collection are explored. Implications for the use of SOI technologies in radiation environments and prospects for single-event modeling of SOI devices and ICs are considered.

II. EXPERIMENTAL AND SIMULATION DETAILS

A. Bulk and SOI CMOS Technologies

Two Sandia CMOS technologies were studied in this work, a 5-V bulk silicon technology, and a 3.3-V SOI technology. The 5-V bulk silicon technology, known as CMOS6r, has been described in detail elsewhere [11]. This technology has a drawn gate length of 0.6 μm , a gate-oxide thickness of 12.5 nm, and uses hardened shallow trench isolation (STI). This single-polysilicon process uses twin doping wells on 2.5- μm thick p-type epitaxial substrates, and is fully planarized using chemical-mechanical polishing. The gate width to length (W/L) ratio for minimum-sized transistors in CMOS6r is 2.3 $\mu\text{m}/0.6 \mu\text{m}$ for both n- and p-channel transistors. Two CMOS6r SRAM ICs were studied in this work, a 16 K SRAM test chip known as the TA788, and a 256 K SRAM standard evaluation circuit (SEC) known as the SA3953. Both ICs use feedback resistors to provide SEU protection, but the 16 K SRAM memory field is separated into two 8K partitions, one of which has feedback resistors and one of which does not. The 256 K SRAM has feedback resistors throughout the entire memory array. Both SRAMs use a symmetric 6-transistor cell design with active p-channel pull-up transistors. The 256 K and the 16 K SRAMs are fabricated simultaneously using a single reticle set, but the 16 K SRAM is fully functional after processing through a single metal level, while the 256 K SRAM requires processing through all three levels of AlCu

metallization available in the CMOS6r process. For ICs that have been processed through all 3 metal levels, the inter-level dielectric (ILD) and passivation overlayer thickness is about $5.6 \mu\text{m}$, and for 16 K ICs processed only through 1 metal level the overlayer thickness is $2.25 \mu\text{m}$. TA788 16 K SRAMs were packaged in 40-pin dual-inline packages (DIPs) that allow full external control of chip timing signals, while SA3953 256 K SRAMs were packaged in 24-pin DIPs and timing signals were internally generated.

A preliminary description of Sandia's 3.3-V partially depleted SOI technology, known as CMOS7, has been given previously [12]. For the ICs studied here, SOITEC bonded SOI wafers with a buried oxide thickness of 200 nm and a post-processing top silicon thickness of about 250 nm were used. This thicker-than-standard top silicon thickness is used to accommodate the Body-Under-Source FET (BUSFET), which is used to provide an efficient body tie and to prevent back-channel inversion in total-dose environments [13]. The 250-nm top silicon ensures an adequate thickness of the body region exists under the shallow source after processing is completed. The CMOS7 technology has a drawn n-channel gate length of $0.35 \mu\text{m}$, a gate-oxide thickness of 8 nm, and uses a hardened STI process similar to CMOS6r. Four levels of AlCu metallization and a single n-type polysilicon layer are used, and the gate width to length (W/L) ratio for minimum-sized transistors is $0.8 \mu\text{m}/0.35 \mu\text{m}$ for n-channel transistors and $0.8 \mu\text{m}/0.45 \mu\text{m}$ for p-channel transistors. Two CMOS7 SRAM ICs were studied in this work, a 64 K SRAM test chip, and a 1 M SRAM standard evaluation circuit. Both ICs use the BUSFET for n-channel transistors and more conventional body ties at the ends of the channel for the p-channel transistors. Similar to the 16 K bulk SRAM, both the 64 K and 1 M SRAM use feedback resistors to provide SEU protection, with the memory array separated into two halves, one of which has feedback resistors and one of which does not. Both SOI SRAMs use a symmetric 6-transistor cell design. The 64 K SRAM is fully functional after processing through a single metal level, while the 1 M SRAM requires processing through all 4 levels of metallization. ICs that have been processed through all 4 metal levels have a total overlayer thickness of about $7 \mu\text{m}$, and for 64 K SRAMs processed only through the first metal level the overlayer thickness is $2.55 \mu\text{m}$. The 64 K and the 1 M SOI SRAMs were packaged in 40-pin and 64-pin DIPs, respectively, and both ICs allow externally generated control signals.

B. Experimental Technique

Heavy ion experiments were performed using both broad-beam and focused ion sources. Broadbeam testing was performed at the Brookhaven National Laboratory tandem Van de Graaff accelerator using a Hewlett-Packard 82000 digital IC tester. All testing was performed in a static mode, i.e., the SRAMs were written with a specific pattern, irradiated to a given fluence, and after the beam was turned off the parts were read and errors were counted. The number of errors for each exposure was limited to no more than 10% of the total number of bits to minimize bit "reflips." All parts were irradiated with a checkerboard pattern at worst-case bias (4.5 V for the 5-V bulk

parts and 3.0 V for the 3.3-V SOI parts). All measurements were performed at room temperature.

Focused ion experiments were performed at the heavy ion microbeam facility on the EN tandem Van de Graaff at Sandia [14]. Ions accelerated by the Van de Graaff were magnetically focused to a submicron spot size, and electrostatically scanned across the SRAM being tested. The size of the scan was calibrated by imaging TEM (transmission electron microscope) grids of known dimensions and pitch. Two types of experiments were performed. The first, calibrated IBICC (ion beam-induced charge collection) imaging, uses a charge sensitive pre-amplifier connected to the V_{DD} pin of the SRAMs to produce 2-D images of charge collection across the scanned region [15]. Measurements of charge collection in a fully-depleted p-i-n diode were used to calibrate the signal electronics (charge sensitive pre-amp, amplifier and digitizer). We also performed SEU imaging experiments, which provide 2-D maps of the SEU-sensitive regions of the SRAMs [14]. For these experiments, an HP82000 digital IC tester was used to monitor the logic state of the SRAMs while the beam was scanned across a region of the memory array. When an upset was noted, the bit error was corrected and a signal was sent to the computer controlling the microbeam to record the scan location of the upset. For the IBICC experiments, the SRAMs were allowed to power up into their preferred logic state, but for the SEU-imaging experiments the SRAMs were tested with a pattern of all "ones" stored in the array.

C. Simulation Methodology

Simulations were performed using the 3-D device/circuit simulator Davinci [16]. Details of the cross section calculations are provided in Section III. SEU threshold calculations were performed using Davinci's mixed-level device/circuit capabilities [17]. Physical models used in the simulations included carrier concentration-dependent minority carrier lifetimes, Auger recombination, and mobility models which included doping, electric field, and carrier-carrier scattering dependence. Because of its importance for SOI devices, all CMOS7 simulations were performed using Davinci's impact ionization model. The impact ionization model parameters were calibrated to snapback experiments in previous work [12].

III. FIRST-PRINCIPLES CALCULATIONS OF SEU CROSS SECTIONS

Standard single-point 3-D mixed-level simulations are known to predict upset thresholds in very good agreement with measured thresholds [18]. In these simulations, the most sensitive strike location must be assumed based on past experience. However, error rates in ICs are dependent not only on the threshold LET, but also on the sensitive area, which cannot be obtained from a single-point simulation. Previous authors have generated simplified step-function cross section curves from theoretical and simulation results by making assumptions about the sensitive area [19], [20]. More recently, charge-collection contours in an SOI transistor were calculated using 2-D simulations, but these simulations could not directly compute upset thresholds

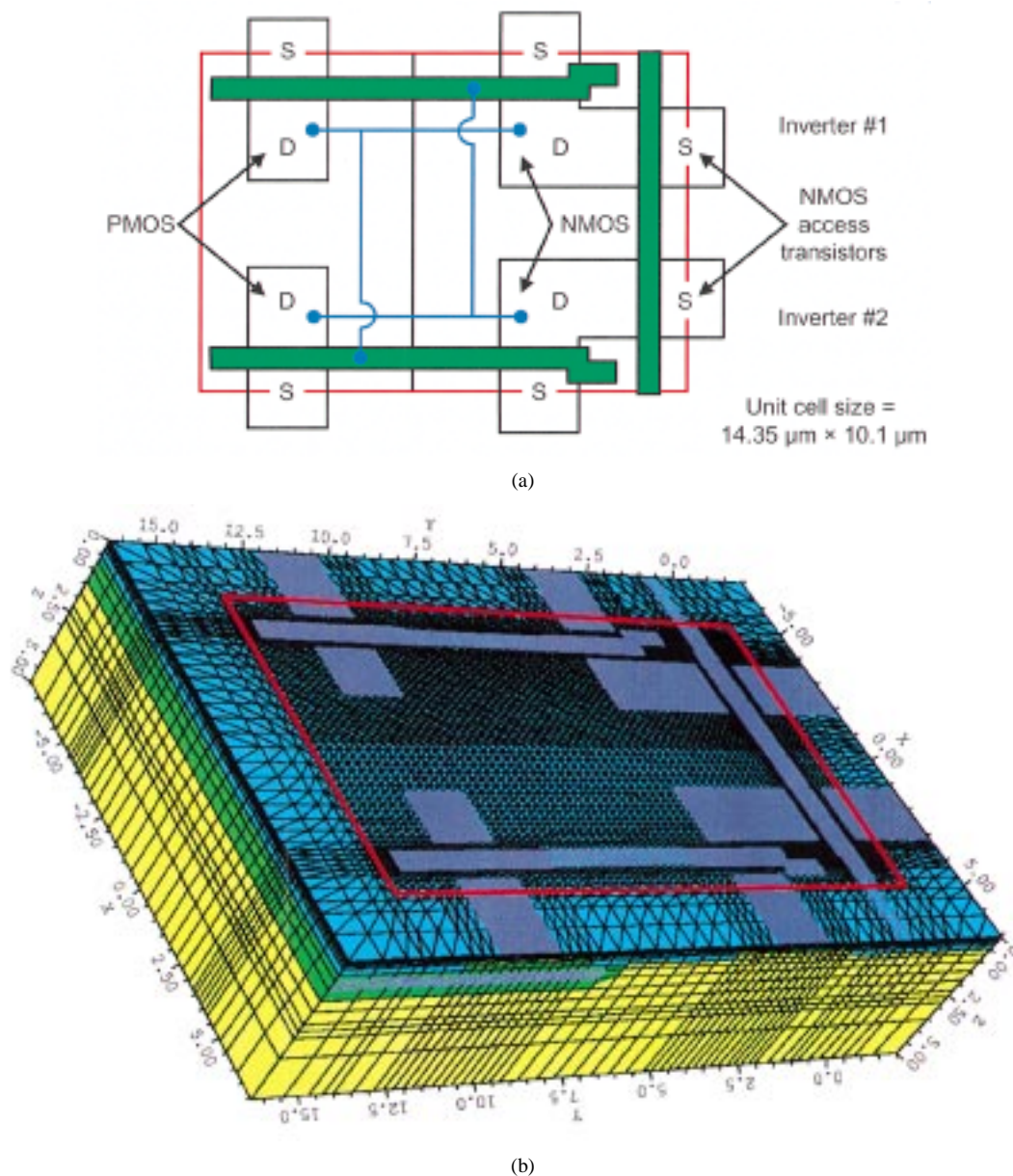


Fig. 1. (a) Layout of 256 K 6-transistor SRAM unit cell (D = drain and S = source). The red box indicates the boundaries of the unit cell, the green regions are the gate polysilicon lines, and the blue lines show the interconnections within the unit cell. (b) View of 3-D unit cell as laid out in Davinci. The mesh size is approximately 100 000 points.

[21]. Using a customized version of Davinci (SNL-Davinci) running on a 592-processor parallel computer we have simulated ion strikes at 630 locations throughout a unit cell of a CMOS6r SA3953 256 K SRAM without feedback resistors. Fig. 1(a) shows a top view of the layout of the 256 K SRAM unit cell without feedback resistors. The red box indicates the boundaries of the unit cell, the green regions are the gate polysilicon lines, and the blue lines show the interconnections within the unit cell. The full SRAM is generated by flipping this unit cell at each of the boundaries. In this figure, “D” indicates a drain region and “S” indicates a source region. Note that for this SRAM design, the NMOS pull-down transistors and the NMOS access transistors share common drains, and all source regions (PMOS and NMOS) are shared with the nearest neighboring cells. The unit cell area is $14.35 \mu\text{m} \times 10.1 \mu\text{m}$, and 3-D simulations were performed for ion strikes incident every $0.5 \mu\text{m}$ throughout the

SRAM unit cell. An additional $2 \mu\text{m}$ of silicon was simulated around the unit cell to minimize nonphysical reflection of carriers at the boundaries. Fig. 1(b) shows the 3-D grid used for the simulations, which contained about 100 000 grid points with a maximum grid spacing of $0.2 \mu\text{m}$.

The simulations give a map of the SEU-sensitive area of the SRAM unit cell for a given ion and energy. By repeating these simulations for several ion/energy combinations, we can generate the evolution of the sensitive area as a function of ion LET, as shown in Fig. 2. For ions with an LET of $11.5 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ (just above the upset threshold), the SEU-sensitive area is the center portion of the reverse-biased NMOS drain. This is the expected most-sensitive strike location [18]. Note that the sensitive area of the reverse-biased NMOS drain increases gradually with LET. For the highest LET values, the sensitive area around the NMOS drain is larger than the drain itself, because diffusion

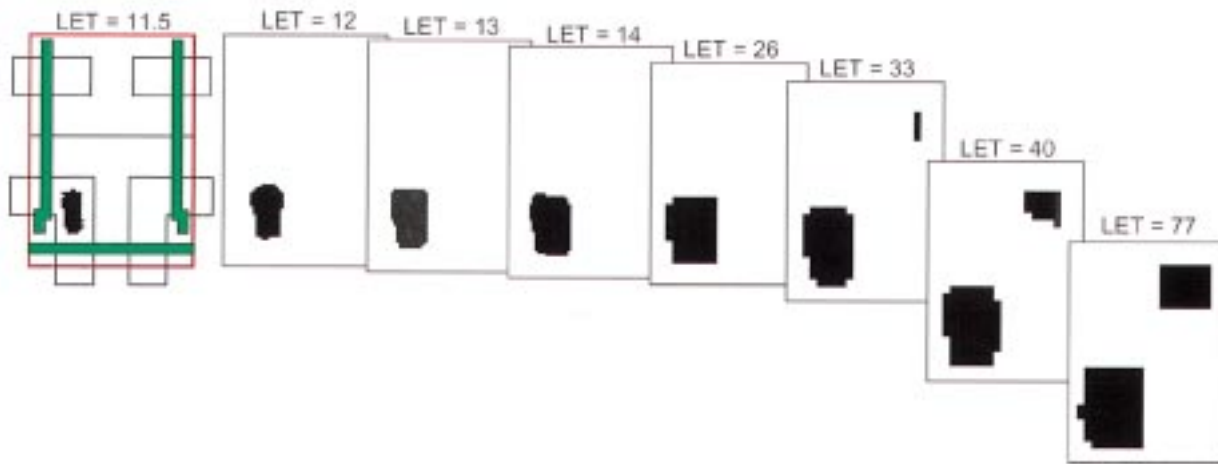


Fig. 2. Evolution of the soft-error sensitive area (black regions) of a 256 K SRAM unit cell without feedback resistors as a function of increasing ion LET. Note increasing sensitive area of reverse-biased NMOS drain. At an LET of 33 MeV-cm²/mg, the reverse-biased PMOS drain also becomes SEU-susceptible.

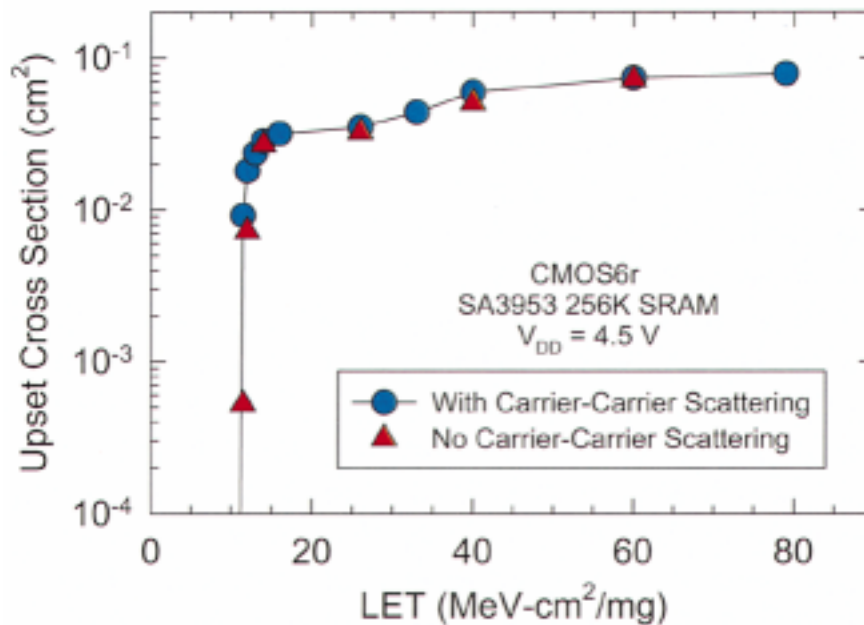


Fig. 3. Simulated upset cross section in a CMOS6r bulk 256 K SRAM without feedback resistors. Each data point is calculated based on the sensitive area of a unit cell multiplied by 256 K.

of charge from near misses is sufficient to cause upsets [22]. At an LET of 33 MeV-cm²/mg, we see that the reverse-biased PMOS drain also becomes susceptible to soft errors. Combining the information in the individual upset maps, we can create a full upset cross section curve for the 256 K SRAM, as shown by the blue circles in Fig. 3. In this figure, the SEU-sensitive area per unit cell has been multiplied by 256 K bits to arrive at the total IC cross section. Note that the cross section curve shows a double-hump structure as first the n-channel, then the p-channel drains become SEU sensitive. We sometimes see evidence of such a hump in experimental data, but it is rarely as pronounced as shown in the simulations, perhaps because it is “washed out” by cell-to-cell variations in the experimental SEU response.

Also shown in Fig. 3 (red triangles), are the results of cross section simulations using a mobility model in Davinci that does

not include carrier-carrier scattering effects. Uncertainty in carrier mobility models due to carrier-carrier scattering at the high carrier concentrations found in an ion track has been postulated to be one of the largest sources of error in single-event simulations [17]. This previous work showed that current transients in unloaded n+/p diodes can have more than a factor of two variation in peak current depending on whether or not carrier-carrier scattering is included in the mobility model used in the simulation. The simulations shown in Fig. 4 indicate that once the device is embedded in an SRAM, there is little difference in either the predicted upset threshold LET or the SEU cross section. These results suggest that at least for the modeled IC, the circuit response to the ion strike dominates the response of an individual junction. It is likely that the presence of carrier-carrier scattering plays a more important role in faster circuits, and in determining the magnitude of single-event transients.

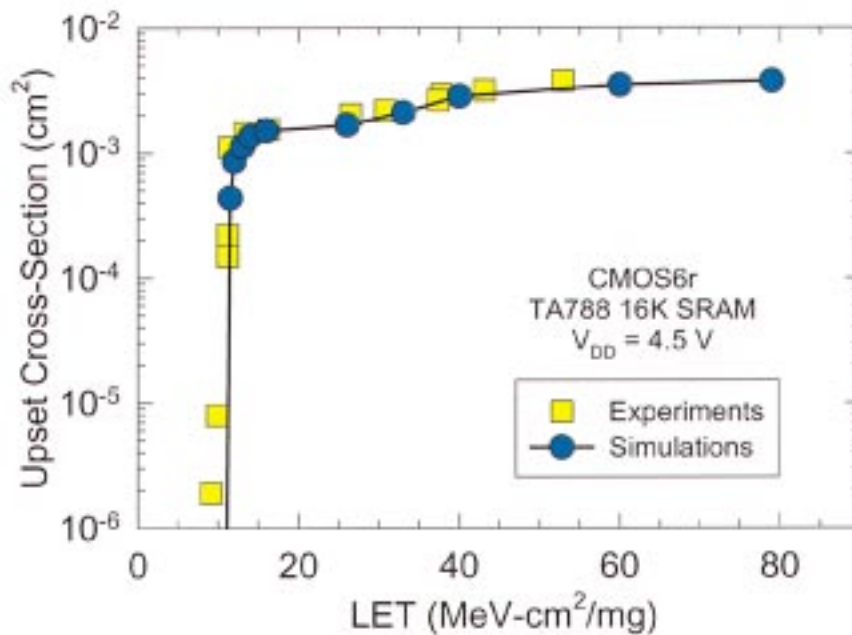


Fig. 4. Measured and simulated upset cross sections in a CMOS6r bulk 16 K SRAM biased at 4.5 V. The cross section curve is shown for the 8K bits of this SRAM that do not contain feedback resistors.

The cross section curve shown in Fig. 3 is based on nearly 7000 individual soft error simulations, and took about three months to perform on 30 nodes of the parallel computer (compared to 7.5 years required for a single-node workstation of equivalent speed). The computational speedup is due to simply running many simultaneous individual jobs. These jobs are managed by Perl scripts that automatically generate the input files, monitor free nodes, submit the jobs as soon as nodes are available, and assemble the results. Unfortunately, because SNL-Davinci is not truly a parallel application, each individual job must fit in the memory space of a single processor; currently, this limits us to running on the relatively small number of processor nodes that have sufficient memory (1 GB) to run a complete unit-cell simulation. An additional feature of SNL-Davinci is that all memory is dynamically allocated, so the number of grid points in a simulation is limited only by available memory. The commercial version of Davinci is limited to 60 000 grid points, but we have demonstrated 333 000 grid point solutions using SNL-Davinci.

IV. SINGLE-EVENT UPSET CROSS SECTIONS: BULK SRAMs

A. Broadbeam Heavy Ion Experiments and Simulations

To validate the simulations of single-event upset cross sections in bulk SRAMs we have performed broadbeam experiments on CMOS6r SRAMs. Because no 256 K SRAMs without feedback resistors were available, we performed experiments and simulations of the TA788 16 K SRAM. Recall that one half of this SRAM does not contain feedback resistors. The measured SEU cross section curve of the 8K of the TA788 without feedback resistors is shown in Fig. 4, along with the simulated cross section curve. The agreement between the data and simulations is within about 20%, which we estimate to be close to the measurement accuracy of the broadbeam experiments. This agreement was obtained without adjusting any parame-

ters for the calculations. Note that a slight hump in the experimental cross section curve at an LET of 35 MeV-cm²/mg due to the p-channel drains becoming sensitive can possibly just be discerned. This good agreement validates that mixed-level simulators like Davinci can accurately predict the SEU-sensitive volumes of bulk-Si ICs. From the mask layout for the TA788 SRAM we find that the combined area of the sensitive n- and p-channel drains (one each per cell) is 26 μm²/bit. For 8K bits, this would result in an expected saturation cross section of about 2 × 10⁻³ cm². However, as previously noted the simulations indicate that the sensitive area around the NMOS drains grows larger than the drain itself due to diffusion from near-miss strikes at high LETs. This leads to cross sections that are larger than the total drain area, and that continue to increase with LET. The failure of upset cross sections to saturate at an asymptotic value has been previously noted in the literature and studied by diffusive transport models [22]. Our results clearly demonstrate that there is not a single well-defined sensitive volume, and that the sensitive volume varies as a function of LET.

B. Focused Ion Microprobe Experiments and Simulations

Focused ion microprobe experiments were performed to provide additional validation of the Davinci simulations at the level of individual memory cells. Fig. 5 shows experimental and simulated SEU images for 35-MeV chlorine ion strikes to a TA788 16 K bulk SRAM (in the region without resistors). Because only a single unit cell was simulated with Davinci, the simulated SEU image was replicated in all directions to produce an equivalent image for several unit cells. A portion of the layout mask is shown overlaid on the simulated upset image to help identify the SEU sensitive regions. The SEU-sensitive regions are shown in black in these images. Both images clearly show that at this LET (~16 MeV-cm²/mg), only the reverse-biased NMOS drains cause upsets.

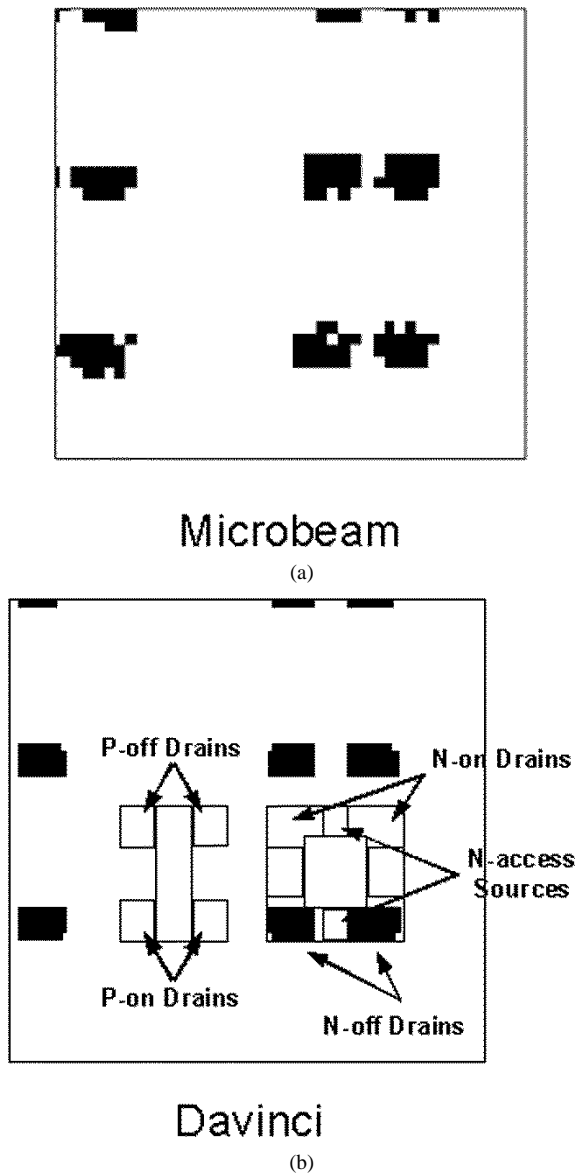


Fig. 5. (a) Single-event upset image of several unit cells in a TA788 16 K bulk SRAM (without resistors) obtained with 35-MeV chlorine ions using a focused ion microbeam. (b) Equivalent simulated SEU map for 35-MeV chlorine ions. The upsetting regions correspond to the reverse-biased n+ drains.

In addition to the soft-error sensitive region for a given ion/energy combination, the simulations give the transient currents in the SRAM cell as a function of ion strike location. By integrating the current over time we can compute the total charge collection as a function of ion strike location in an externally accessible contact (in the present work, the power supply pin, V_{DD}). By comparing the simulated charge-collection images to experimentally measured calibrated IBICC images obtained from the heavy ion microprobe, we are able to further validate the accuracy of the simulations. Fig. 6 shows a 20-MeV carbon-ion calibrated IBICC image of several unit cells of the TA788 16 K SRAM in the memory region without feedback resistors, along with the simulated charge collection. 20-MeV carbon ions have an LET of ~ 6 MeV-cm²/mg, below the upset threshold. Because of background electrical noise in the microbeam target chamber, the minimum charge collection signal that could be measured in this experiment was about 30 fC. Con-

sequently, although the simulations indicate that some regions exhibit even lower charge collection, a minimum collection of 30 fC has been used in rendering the simulated IBICC image in Fig. 6 in order to facilitate direct comparisons. The simulated and measured IBICC images generally agree to within about 20–30%. The regions showing highest charge collection include the reverse-biased n-channel drain that is sensitive to upsets, and the n-well/p-epi junction in which the p-channel transistors are located. Although the entire n-well/p-epi junction area shows high charge collection, it is important to remember that strikes here cannot cause upset because the charge is collected directly into the V_{DD} and V_{SS} lines and does not affect the memory cell. The microbeam IBICC image clearly shows that the off-biased p-channel transistors exhibit locally higher charge collection within the n-well, but this is more difficult to see in the simulated charge-collection image. The n+ sources of the access transistors also show considerable charge collection because they are pre-charged to V_{DD} , but strikes to these regions do not cause upsets.

The validation experiments shown here indicate that mixed-level device/circuit simulation tools such as Davinci are well-suited to single-event upset modeling of bulk CMOS SRAMs. Previous validation studies showed good agreement with experiments for single-point SEU threshold calculations [18], but the results presented in this section represent a much more rigorous validation of Davinci. It is important to note that all of the simulations performed here were for SRAMs without feedback resistors. For resistively-hardened SRAMs it is common to measure decreasing saturation cross sections with increasing resistor size, but the reasons for this are not currently well-understood. In the future we hope to study this phenomenon using similar first-principles cross section calculations.

V. SEU CROSS SECTIONS: SOI SRAMs

A. Broadbeam Heavy Ion Experiments and Simulations

64 K and 1 M CMOS7 SOI SRAMs fabricated at Sandia were tested at Brookhaven to study the upset cross section curve in SOI ICs. The measured upset cross section curve for both devices is shown in Fig. 7. Data are shown for the halves of the SRAMs without feedback resistors and the halves with 100 k Ω feedback resistors. The halves of the SRAMs without resistors showed an upset threshold LET of about 7–10 MeV-cm²/mg, and 100 k Ω feedback resistors increased the threshold LET to 35–40 MeV-cm²/mg. These values of threshold LET are consistent with single-point Davinci simulations of the upset threshold due to gate region ion strikes. Davinci predicts gate-strike upset thresholds of 7 MeV-cm²/mg for SRAMs without resistors, and 40 MeV-cm²/mg for SRAMs with 100 k Ω feedback resistors. However, careful analysis of the curves in Fig. 7 for the SRAMs without resistors shows that the saturation cross section is about 7 $\mu\text{m}^2/\text{bit}$ for the 1 M SRAM, and almost 8 $\mu\text{m}^2/\text{bit}$ for the 64 K SRAM. The total sensitive gate area (assuming one sensitive n-channel gate and one sensitive p-channel gate per bit) in both SRAMs is the same: 0.64 $\mu\text{m}^2/\text{bit}$. On the other hand, the gate plus drain area per bit (assuming one sensitive n-channel drain and one sensitive p-channel drain per bit) matches much more closely the measured saturation cross section: 6.1 $\mu\text{m}^2/\text{bit}$ for

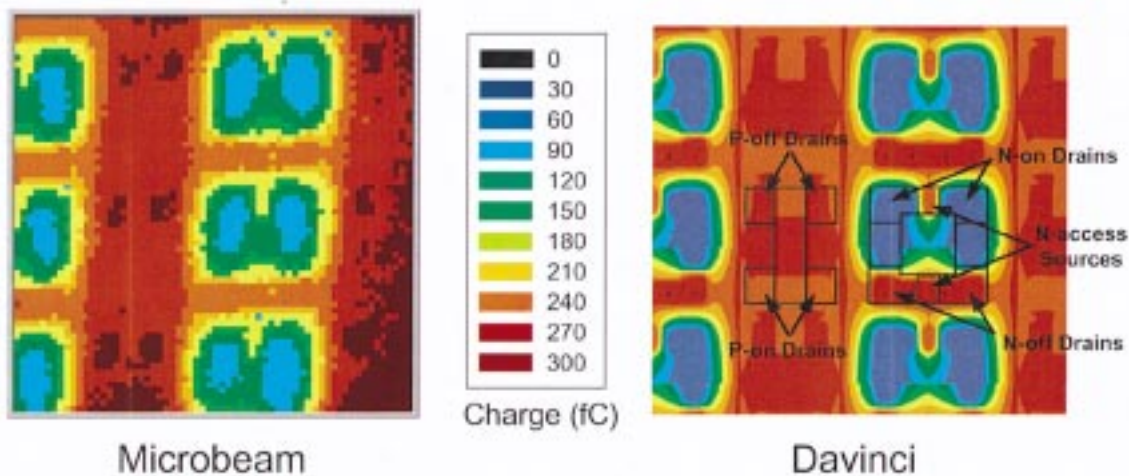


Fig. 6. Left: Calibrated IBICC image of several unit cells in a TA788 16 K bulk SRAM obtained with 20-MeV carbon ions using a focused ion microbeam. Right: Equivalent simulated charge-collection map for 20-MeV carbon ions. The color scales for both maps are the same and indicate total charge collection measured at the power supply.

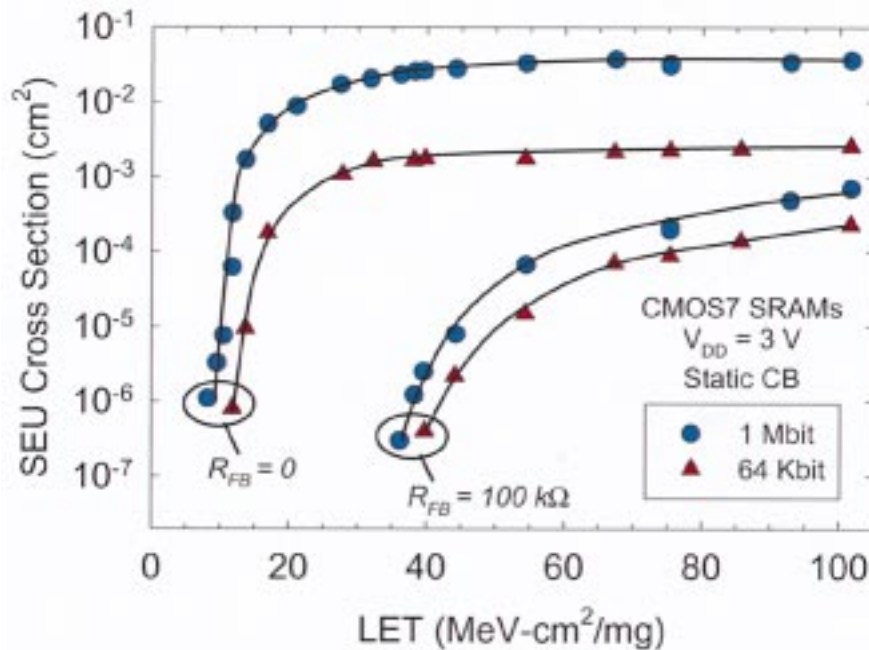


Fig. 7. SEU cross section in 1 M and 64 K CMOS7 SOI SRAMs with and without feedback resistors at $V_{DD} = 3$ V.

the 1 M SRAM, and $6.3 \mu\text{m}^2/\text{bit}$ for the 64 K SRAM. The data of Fig. 7 therefore suggest that *not only the gate regions of these SRAMs are sensitive, but also the reverse-biased drain regions*. This is in contrast with conventional wisdom that only gate-region strikes cause upsets in SOI and SOS ICs [10], [19], [23], [24].

We have not performed full cross section simulations for the SOI SRAMs, but single-point Davinci simulations of n-channel gate and drain strikes are shown in Fig. 8. Simulated gate and drain voltage transients are plotted following ion strikes with an LET of $30 \text{ MeV-cm}^2/\text{mg}$ (well above the SEU threshold) to the centers of the gate and reverse-biased drain regions. For the gate strike (red curve in Fig. 8), Davinci correctly predicts that the memory cell will upset. For a strike to the center of the reverse-biased drain, however, Davinci predicts no significant

transient response will occur. In fact, Davinci predicts a total drain charge collection of *less than 0.25 fC*. Although this is in agreement with the traditional idea that only gate strikes cause upsets, it is clearly inconsistent with the broadbeam heavy ion data.

B. Focused Ion Microprobe Experiments

To further study the possibility of drain strikes causing upsets in SOI ICs, we performed focused ion microbeam experiments on the 64 K CMOS7 SRAMs. IBICC imaging was carried out using 20-MeV carbon ions ($\text{LET} = 6 \text{ MeV-cm}^2/\text{mg}$) to determine if significant charge collection occurred in the reverse-biased drain regions. Previous experiments at the Sandia microbeam by researchers at the Air Force Research Laboratory (AFRL) had indicated the possibility for drain charge collection

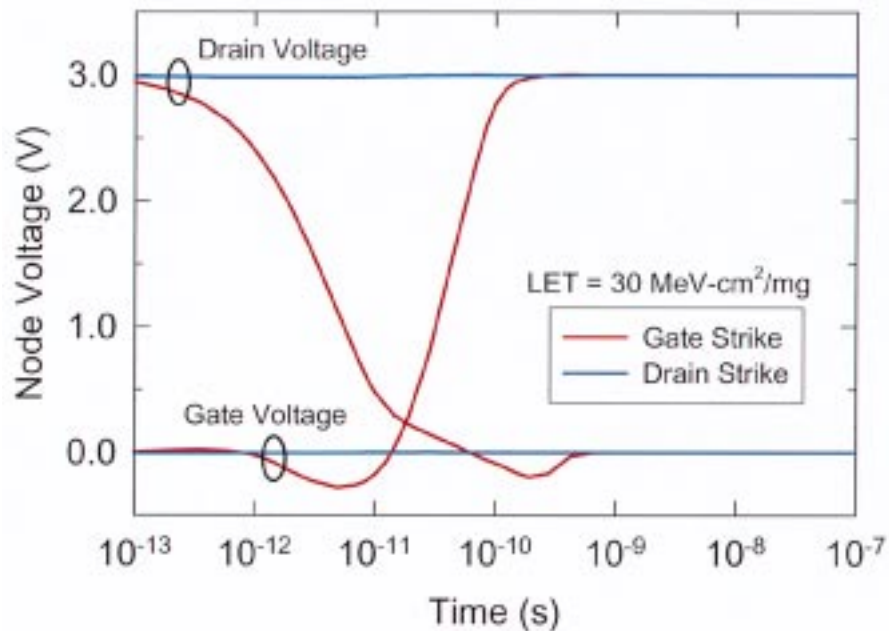


Fig. 8. Simulated single-event voltage transients following ion strikes to the center of the gate and drain regions of an n-channel SOI transistor in an SRAM cell. Davinci predicts no significant transient response to drain region strikes.

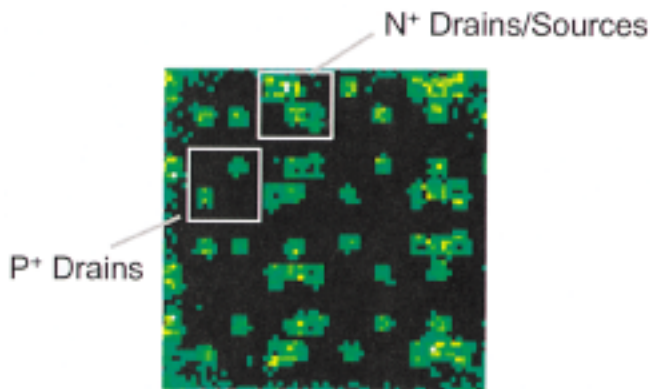


Fig. 9. Uncalibrated IBICC image for 20-MeV carbon ions showing regions of highest charge collection in a 64 K SOI SRAM at $V_{DD} = 3$ V.

in isolated fully-depleted SOI transistors fabricated by MIT Lincoln Labs [25], while our own measurements had also revealed surprisingly large charge collection signals from heavily-doped silicon regions of SOI test structures. For the IBICC experiments reported here, the charge-collection signal was measured at the V_{DD} pin, and the substrate bias was 0 V.

Fig. 9 shows an uncalibrated IBICC image from the 20-MeV carbon ion experiments. The green regions in this image are the regions with the highest charge collection in the scan area. Unlike IBICC spectra measured from previous non-SOI devices, such as in Fig. 6, the IBICC spectra measured from some charge collection regions of this SOI SRAM (e.g., the reverse-biased p-channel drains) do not exhibit clear, well-defined peaks. At this point it would be misleading to identify a characteristic charge collection value from these spectra without further understanding of the underlying charge collection mechanism. This issue is currently under further investigation. Nonetheless, the IBICC image of Fig. 9 clearly

indicates that the reverse-biased drains (both n- and p-channel) and the n-channel access transistor sources are regions of high charge collection. These results strongly suggest that charge collection from either within the buried oxide or the substrate (or a combination of both) is occurring.

SEU imaging experiments were performed on the 64 K CMOS7 SRAMs to unambiguously determine whether the unexpectedly high charge collection measured from the drains in the IBICC experiments could indeed cause upsets, as indirectly inferred from the broadbeam data. 35-MeV chlorine ions ($LET = 16$ MeV-cm²/mg) and 50-MeV copper ions ($LET = 29$ MeV-cm²/mg) were used for these experiments. Both ions are above the SEU threshold LET, but the 35-MeV Cl ions are only slightly above the threshold (still in the region of rapidly increasing cross section), while the 50-MeV Cu ions are in the region where the cross section is near its saturation value (see Fig. 7). The upset images for both ions are displayed in Fig. 10, overlaid on top of the 64 K SRAM mask layout to allow identification of the regions causing upsets. In these images, only the polysilicon lines (pink regions in Fig. 10) and the silicon active region islands (blue regions) are shown. Regions that cause upsets when hit by the ion beam are shown in black on top of the layout mask. For the 35-MeV chlorine experiment (left side of Fig. 10), we see that only ion strikes to the gate regions are causing upsets, but both the n-channel and p-channel gates are upsetting. These results are consistent with the broadbeam-measured upset cross section (1.8×10^{-4} cm², or 0.55 $\mu\text{m}^2/\text{bit}$) at an LET of 16 MeV-cm²/mg, which closely corresponds to the total expected sensitive gate area of 0.62 $\mu\text{m}^2/\text{bit}$. These data support the usual supposition that the gate regions are the most SEU-sensitive area in SOI SRAMs.

In the 50-MeV copper image (right side of Fig. 10), the regions causing upsets have grown to include not only the gate regions, but also the n- and p-channel reverse-biased

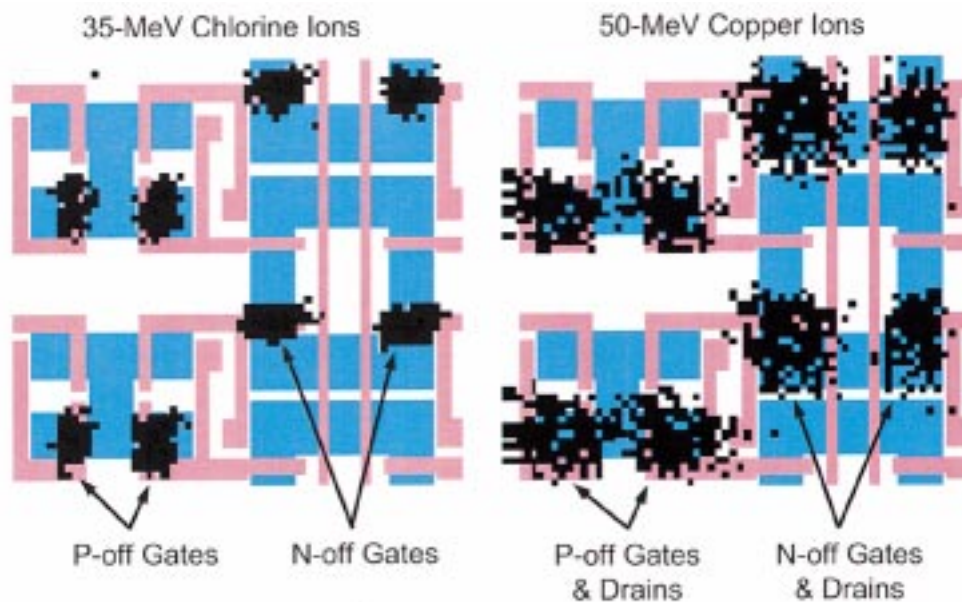


Fig. 10. Focused ion microbeam single-event upset images of several unit cells in a 64 K SOI SRAM without feedback resistors. Left: Image obtained using 35-MeV chlorine ions (LET= 16 MeV-cm²/mg). Right: Image obtained using 50-MeV copper ions (LET= 29 MeV-cm²/mg). In these images the pink regions are the polysilicon lines, the blue regions are the active silicon islands, and the black regions are locations that cause upsets when hit by the ion beam.

drain areas. While a portion of the increase in the measured SEU-sensitive area shown in this figure could be attributed to the typically poorer beam focus that can be achieved with heavier ions, differences in beam focus cannot explain all of the increase in sensitive area, nor can they account for the shift in offset between the n- and p-channel sensitive regions. By this we mean the fact that as the p-channel sensitive regions grow to include the p-drains they become bigger primarily in the horizontal direction of Fig. 10, while the n-channel sensitive regions grow bigger in the downward vertical direction of Fig. 10 as the n-drains become sensitive. This fact gives the n-channel sensitive regions the appearance of having moved downward in the copper image of Fig. 10. This behavior is contrary to what could be explained by use of a larger beam diameter alone, since in that case these upset regions would simply expand symmetrically about their center. Taken in tandem with the broadbeam data of Fig. 7, the data of Fig. 10 show conclusively that for these SOI SRAMs drain strikes can indeed cause single-event upsets.

VI. DISCUSSION

A. Charge Collection Mechanisms in SOI

From the results in Section IV, it appears that charge-collection mechanisms and SEU-sensitive volumes in bulk-Si technologies are fairly well understood and can be accurately modeled using current simulation tools. For SOI technologies, however, we find an unexpectedly large amount of charge collection from both the n- and p-channel reverse-biased drains. This was an unexpected result, but is well-supported by both broadbeam and microbeam experiments.

Early work published on CMOS/SOS and CMOS/SOI SRAMs discussed the possibility of charge collection from the buried oxide or substrate. The first paper on the transient

response of SOI CMOS SRAMs found larger than expected photocurrents, and briefly conjectured on the possibility of conduction through the buried oxide before determining that the cause of the excess current was the now well-known parasitic bipolar effect [26]. CMOS/SOS heavy ion experiments showed that charge deposited in the sapphire substrate was not collected in the silicon layer, and that the SEU-sensitive area in CMOS/SOS SRAMs could be attributed entirely to gate strikes [24], [27]. More recently, Musseau *et al.* performed charge collection experiments on source/buried oxide (BOX)/substrate capacitors as a function of substrate bias [28]. The measured charge collection was ascribed to “substrate funneling,” in which the ion track perturbs the electric field under the capacitor when biased in inversion and causes a capacitive discharge [10], [29]. It was predicted that substrate funneling would probably not degrade the sensitivity of SOI technologies. Some recent data on deep submicron ($\leq 0.35 \mu\text{m}$) SOI ICs have shown considerably larger than expected upset cross sections, but the discrepancies were explained by the size of the high-energy ion track used in the experiments, which was larger than the transistor body dimensions [30]. Under these conditions, the cross section is no longer a valid concept, and becomes a measure of the size of the ion track radius rather than a true sensitive volume.

SEU cross section data have been reported for 0.25- μm commercial SOI and bulk SRAMs fabricated at IBM [31]. The measured saturation cross section in the SOI ICs was about 1/10 that of the equivalent bulk ICs, a reasonable ratio of gate to drain area. On the other hand, the sensitive area in the SOI SRAMs was 1.5 $\mu\text{m}^2/\text{bit}$, which seems very large for this 0.25- μm technology. Unfortunately, no transistor-level design information was given, but an area of 1.5 $\mu\text{m}^2/\text{bit}$ implies a transistor gate width of 6 μm if only the channel region were SEU-sensitive. Very recently, SEU cross section data have been

reported for 0.2- μm commercial SRAMs manufactured by Mitsubishi [32]. The saturation cross section of these ICs was about 2 $\mu\text{m}^2/\text{bit}$, but the total sensitive gate area (assuming one sensitive n-channel gate and one sensitive p-channel gate per bit) in the SRAM was less than 0.2 $\mu\text{m}^2/\text{bit}$, while the gate plus drain area was estimated to be about 1.2 $\mu\text{m}^2/\text{bit}$ [33]. These results suggest that in these commercial SOI SRAMs drain upsets are likely occurring.

Our results indicate that revisiting the possibility of substrate and/or buried oxide charge collection in SOI devices is merited. Figs. 7, 9, and 10 indicate that n- and p-drain charge collection can occur, and that it can cause upsets in our SRAMs without feedback resistors. For the reverse-biased n-channel drains of Fig. 9, the IBICC spectra do show a well-resolved peak at a charge collection of 39 fC. Secondary ion mass spectroscopy (SIMS) measurements of the dopant profiles in our n-channel transistors confirm that the heavily-doped n-drains extend all the way to the BOX. It is highly unlikely that any significant amount of charge liberated in the very heavily-doped drain regions could be collected before it recombines, but even if this did occur, the total charge generated in the 250-nm top silicon layer by a 20-MeV carbon ion is only about 10 fC. Even less charge (<2 fC) is liberated in the 200-nm BOX; this leaves a significant amount of charge that could only come from the substrate. We believe the most likely scenario is that a temporary conductive pipe between the substrate and the top silicon is induced by the ion strike, similar to that presumed to account for single-event gate ruptures [34]. The low fields present in the buried oxide do not lead to ruptures, and if permanent damage is caused by the ion strike it was not detectable in our experiments. While the conductive pipe exists, charge can be transferred between the substrate and the drain. For high enough LETs this charge transfer becomes more efficient (the pipe becomes more conductive [34]), and upsets may result. Electrons liberated within the buried oxide may also participate in this process, but are probably insufficient by themselves to account for the observed charge collection. The exact details of what drives charge transfer between the drain and substrate are not known.

At this point it is reasonable to ask why this mechanism was not observed previously, especially given that researchers were actively looking for it 10–15 years ago. We can only conjecture that significant improvements in buried oxide quality and the thinner buried oxides of today have materially changed the charge transport properties of the BOX. It is also possible that as devices have scaled, what was previously a negligible amount of additional charge collection has become a significant contributor to single-event upset.

B. Prospects for Single-Event Modeling in SOI

As shown in Fig. 8, standard device models such as Davinci do not predict any significant impact of ion strikes to the drain of SOI transistors. In fact, for the drain strike simulated in Fig. 8, Davinci predicts a drain charge collection of less than 0.25 fC. This is because in its standard configuration, Davinci completely ignores charge transport in the oxide (it assumes oxides are perfect insulators), and the charge liberated in the heavily-doped drain immediately recombines before it can

be collected. Total-dose models that treat charge transport in oxides have been developed and could perhaps be applied to the study of ion-induced transport in the BOX of SOI devices [35], [36]. Such models might also prove useful for studying single-event gate rupture. Whether these models can be adapted to accurately predict the formation and charge transport properties of conductive pipes in the oxide (if this is the pertinent transport mechanism) is not clear. What is clear is that without such improvements the usefulness of device simulations to study single-event mechanisms in SOI devices and ICs may be limited.

Given the failure of Davinci to correctly predict the SEU response of SOI due to drain strikes, one might wonder how it so closely predicted the threshold LETs observed in Fig. 7 for SOI SRAMs with and without feedback resistors. This may be an indication that for gate strikes (which are in fact the most sensitive strike locations), either substrate charge collection does not occur, or it is insignificant compared to bipolar-enhanced collection from the body region. For either case, the SEU response may be controlled by charge collection in the silicon layer, which Davinci accurately models.

VII. CONCLUSION

In this summary, we have used large-scale 3-D simulations, broadbeam experiments, and focused ion microscopy to study several aspects of SEU-sensitive volumes in bulk-Si and SOI CMOS SRAMs.

Using a customized version of the Davinci mixed-level device simulator we have performed first-principles 3-D simulations of the SEU cross section curve for a bulk CMOS SRAM. The simulations predict a double-hump structure in the curve as distinct regions (first the n-drains, then the p-drains) become sensitive to SEU. This characteristic is difficult to observe in experimental curves, probably because of cell-to-cell variations in the SEU response. The simulations also predict nonsaturating upset cross sections that are frequently observed experimentally. This nonsaturation is due to diffusion of charge from strikes near sensitive reverse-biased junctions. At high LET values this diffusive charge collection results in a gradual growth in upset cross section, demonstrating that there is no single well-defined sensitive volume.

Direct comparisons of simulated and experimentally-measured cross section curves show agreement to within 20%. Simulated charge-collection maps in a 16 K SRAM show similar agreement with images obtained using a focused ion microbeam. These techniques allow much more rigorous validation of the Davinci code by enabling large-area multipoint comparisons rather than the simple single-point comparisons that have been possible previously.

Studies of SEU in SOI SRAMs fabricated at Sandia have shown an unexpectedly large amount of charge collection following drain region strikes. Simulations do not predict this sensitivity, but seem to accurately predict gate-strike induced upset thresholds, at least for the ICs simulated here. We find that drain charge collection can lead to an SEU-sensitive volume in SRAMs without resistors that includes the reverse-biased n- and p-channel drains. This may increase the SEU-sensitive area (and

hence the error rate) in commercial SOI ICs by about a factor of ten compared to gate strikes alone, depending on the relative areas of the gate and drain regions.

We postulate that the anomalous drain charge collection is due to the formation of a conductive pipe in the SOI buried oxide immediately following an ion strike. This conductive pipe allows the transfer of charge between the substrate and the active silicon region. While no permanent damage to the BOX results, for high enough LETs this charge transfer may cause single-event upsets in some SOI ICs. Current device simulation tools may have to be modified to accurately predict the SEU response of SOI integrated circuits.

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