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Shallow states at SiO_2/4H-SiC interface on $(11\bar{2}0)$ and (0001) faces

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Shallow interface states at SiO_2/4H-SiC were examined on $(11\bar{2}0)$ and (0001) faces using metal–oxide–semiconductor (MOS) capacitors. The MOS capacitors were fabricated by wet oxidation on both faces to investigate the difference in the energy distribution of interface state density. The parallel conductance as a function of frequency was measured at room temperature, and high-frequency capacitance (C)–voltage (V) curves were measured both at room temperature and 100 K. By the conductance method, the interface state density on $(11\bar{2}0)$ was revealed smaller than on (0001) at shallow energies, while at deeper energies the relation changes to opposite situation. High-frequency $C-V$ curves at 100 K show a large positive flatband voltage shift and a large injection-type hysteresis on (0001) samples, while those were small on $(11\bar{2}0)$, indicating another evidence of smaller interface state density near the conduction band edge on $(11\bar{2}0)$. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1492313]

Silicon carbide (SiC) has received much attention due to its superior physical properties for high-power and high-temperature devices. In addition, insulating oxide SiO_2 can be grown by thermal oxidation like for Si. Therefore, many researchers have been trying to realize SiC metal–oxide–semiconductor field-effect transistors (MOSFETs) with high performance, especially in 4H-SiC due to higher electron mobility in the bulk. However, the SiO_2/4H-SiC interface processed by standard thermal oxidation has a high density of interface states,[1–3] resulting in poor MOSFET performance[4,5] due to a low channel mobility (typically $<10\ cm^2/V\,s$).[6–10] Almost all MOS-related researches have been done using (0001) face materials. We have reported that a higher channel mobility ($\sim 100\ cm^2/V\,s$) can be obtained for 4H-SiC MOSFETs by using the $(11\bar{2}0)$ face[11–13] instead of the conventional (0001) face. Recently another group has improved the channel mobility further ($>110\ cm^2/V\,s$) by applying post-oxidation annealing in hydrogen or pyrogenic steam on the $(11\bar{2}0)$ face.[14,15] We also found that the interface state density was very different for the $(11\bar{2}0)$ and (0001) faces, from the temperature dependence of threshold voltage of the MOSFETs.[16] In this letter, we evaluate the interface state density based on the conductance and capacitance measurements of MOS capacitors at room temperature and a low temperature for the $(11\bar{2}0)$ and (0001) faces, focusing on shallow interface states.

MOS capacitors were fabricated on nitrogen-doped n-type epilayers grown by chemical vapor deposition (CVD) on 4H-SiC substrates with the surface orientations of $(11\bar{2}0)$ and (0001). The $(11\bar{2}0)$ substrates were prepared by cutting modified-Lely-grown bulk crystals parallel to the $(11\bar{2}0)$ face without an intentional off-angle. The (0001) substrates have an off-angle of 8°. The net donor concentrations of epilayers were 2×10^{16}–$2\times10^{17}\ cm^{-3}$ achieved by changing growth conditions during CVD. Prior to thermal oxidation, the samples were cleaned by a standard RCA method with a HF dip at the final step. Then, wet oxidation was performed at 1100 °C for 50 min, resulting in oxide thicknesses of approximately 40–50 nm and 14 nm for $(11\bar{2}0)$ and (0001) samples, respectively. For (0001) samples, 40-nm-thick oxides were also grown by wet oxidation at 1150 °C for 120 min. After the thermal oxidation, all samples were subjected to post-oxidation annealing at the oxidation temperatures for 30 min in Ar. Al was used for the gate electrode with a diameter of 300 μm. For the backside contact, blanket deposition of Al was done.

To obtain the interface state density (D_{it}), the parallel conductance (G_p) as a function of frequency was measured at room temperature. High-frequency (1 kHz, 1 MHz) capacitance (C)–voltage (V) characteristics were also measured at both room temperature and a low temperature (100 K) with a bias sweep rate of 0.1 V/s. Both the conductance and capacitance measurements were done by using a computer-controlled HP4284A precision LCR meter in an electrically shielded dark box.

The interface state density was extracted from a conductance method, which is considered to be the most sensitive way to determine the interface state density. The equivalent parallel conductance was measured at a given gate bias voltage, which caused a certain band bending, over a wide frequency range from 1 kHz to 1 MHz. The conductance represents the loss due to capture and emission of carriers by interface states, and the peak value of equivalent parallel conductance divided by angular frequency (ω) is directly connected to the interface state density as follows:[17]

$$D_{it}=\frac{1}{qAf_D}\left[\frac{G_p}{\omega}\right]_{peak}. \tag{1}$$

Here, A is the area of gate electrode and f_D is a parameter depending on the standard deviation of the surface potential fluctuations (σ_s). Not only the interface state density but also the capture cross section for majority carriers and infor-

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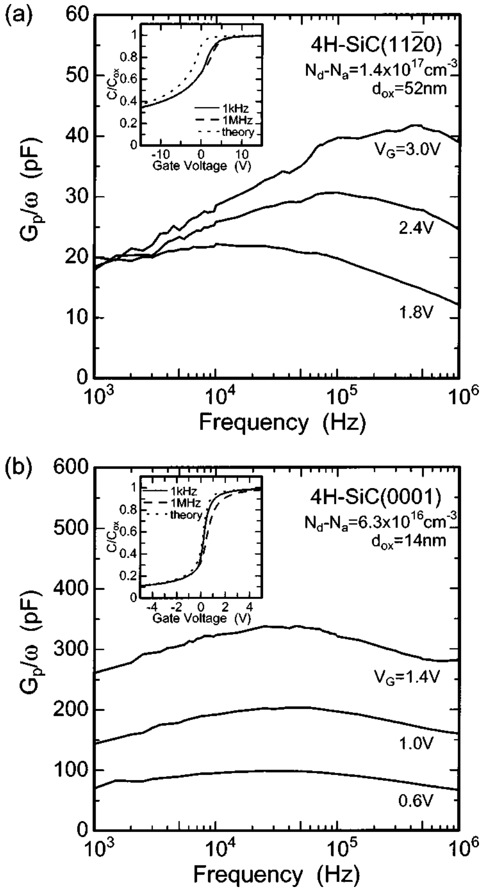

FIG. 1. G_p/ω as a function of frequency for n-type 4H-SiC MOS capacitors with wet oxides on (a) (11$\bar{2}$0) and (b) (0001) faces. Insets show high-frequency $C-V$ curves for the corresponding MOS capacitors.

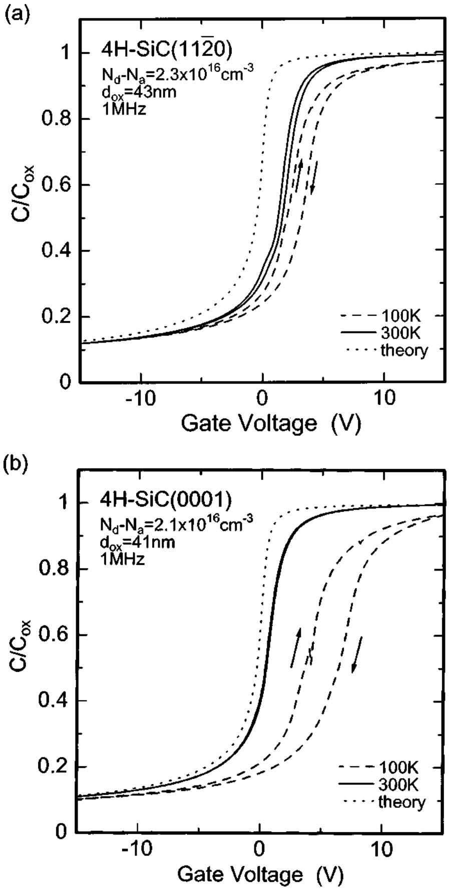

FIG. 3. High-frequency (1 MHz) $C-V$ characteristics of n-type 4H-SiC MOS capacitors on (a) (11$\bar{2}$0) and (b) (0001) faces measured at 300 K and 100 K. Injection-type hysteresis is observed.

mation about surface potential fluctuations can be evaluated by the conductance method. However, this paper focused on the interface state density.

The measured G_p/ω as a function of frequency for different gate biases is shown in Figs. 1(a) and 1(b) for the (11$\bar{2}$0) and (0001) faces of 4H-SiC MOS capacitors, respectively. The inset figures show high-frequency $C-V$ curves of the corresponding MOS capacitors. Though the $C-V$ curve measured at 1 kHz of 4H-SiC(0001) looks close to the theoretical curve compared to that of 4H-SiC(11$\bar{2}$0), the frequency dispersion between 1 kHz and 1 MHz for the (0001) sample is larger than that for the (11$\bar{2}$0) sample. This indicates that the (0001) sample has a higher density of interface states than (11$\bar{2}$0). This fact is observed directly from the peak height of G_p/ω for these two samples. The peak heights of G_p/ω for the sample on the (11$\bar{2}$0) face are one order of magnitude lower than that for the sample on the (0001) face, indicating that the interface state density on 4H-SiC(11$\bar{2}$0) is lower than that on 4H-SiC(0001) by one order of magnitude. Using the manner given as a simple calculation method,[18] values of σ_s (in thermal units of kT/q) and $1/f_D$ were extracted to be 3.5 and 6.3 for (11$\bar{2}$0), and 3.7 and 6.8 for (0001), respectively.

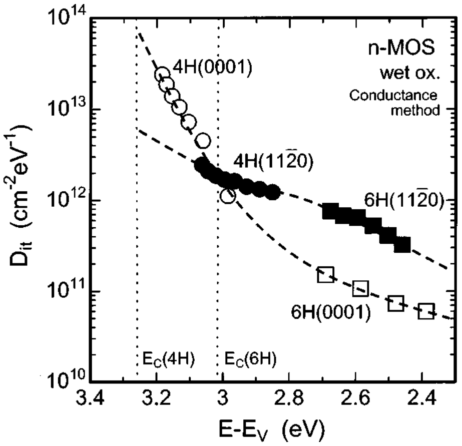

FIG. 2. Interface state density (D_{it}) of 4H-SiC MOS capacitors processed by wet oxidation calculated by conductance method. Energy position of D_{it} is plotted from the valence band edge. The data of 6H-SiC on (11$\bar{2}$0) and (0001) are also plotted.

The interface state density for these samples are shown in Fig. 2, in which the energy position is plotted from the valence band edge. In Fig. 2, the results obtained from 6H-SiC MOS capacitors fabricated in the same manner as 4H-SiC are also shown. The properties of 6H-SiC MOS capacitors on (11$\bar{2}$0) and (0001) indicate the similar tendency to a previous report,[19] in which the samples were oxidized in wet O_2 and their interface state densities were measured by the conductance method at 310 °C. 4H- and 6H-SiC have the same energy for the valence band edge, which is 6.0 eV below the conduction band edge of SiO_2.[20,21] The distribution of interface state density for 4H- and 6H-SiC can be plotted on the same curve, and this can be applied even in the different surface orientations. Therefore, the larger band gap

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polytype of 4H-SiC has a higher interface state density near the conduction band edge. The increase of the interface state density is emphasized on the (0001) face, resulting in a quite high density of states at the SiO_2/4H-SiC(0001) interface near the conduction band edge, even if a low interface state density is obtained at deeper energies. On the $(11\bar{2}0)$ face, however, the increase of interface state density is slow, which leads a lower density of states at the SiO_2/4H-SiC$(11\bar{2}0)$ interface near the conduction band edge. For this reason, less electron trapping at the interface occurs in the inversion condition of MOSFETs, and a higher channel mobility can be obtained on the $(11\bar{2}0)$ face.

Another way to characterize the shallow interface states is to measure high-frequency $C-V$ curves at low temperatures.[22,23] At low temperatures, the emission time of electrons trapped at interface states becomes long, and then the interface states at shallow energy affect $C-V$ curves. Because of this, relatively shallow interface states bring a large positive shift in $C-V$ curves due to the existence of negative charges caused by electrons trapped at the interface. In addition, electrons trapped at quite shallow interface states are emitted gradually during the voltage sweep of $C-V$ curves, leading a large injection-type hysteresis. At room temperature, such shallow states do not contribute to both the flatband voltage shift and hysteresis, because the emission time of electrons becomes short.

Figures 3(a) and 3(b) show $C-V$ curves at 1 MHz for 4H-SiC MOS capacitors on $(11\bar{2}0)$ and (0001), respectively, measured at 300 K and 100 K. Both samples have a similar oxide thickness of 40 nm grown in wet O_2 at different oxidation temperatures and different oxidation times. At 300 K, the flatband voltage shift on $(11\bar{2}0)$ is 2.6 V, which is the difference between the theoretical curve and the measured curve from accumulation to depletion direction. The value is larger than on (0001) (1.2 V) due to a higher interface state density at deeper energies for $(11\bar{2}0)$ as shown in Fig. 2. Electrons trapped at the deeper energies work as negative charges, which brings the large positive flatband shift. The effective negative oxide charge densities extracted from the flatband voltage shift are 1.3×10^{12} cm^{-2} for $(11\bar{2}0)$ and 6.5×10^{11} cm^{-2} for (0001). At a low temperature of 100 K, however, a larger flatband voltage shift is observed on (0001) than on $(11\bar{2}0)$. The flatband voltage shifts and the effective oxide charge densities measured at 100 K are 4.9 V and 2.4×10^{12} cm^{-2} for $(11\bar{2}0)$ and 8.0 V and 4.3×10^{12} cm^{-2} for (0001), respectively. As for a hysteresis, the different aspect between $(11\bar{2}0)$ and (0001) clearly appeared as in Fig. 3. On $(11\bar{2}0)$, a hysteresis of 0.4 V is observed at 300 K, and it increases to 0.9 V at 100 K. The increase of hysteresis from 300 K to 100 K corresponds to an emitted electron density of 2.6×10^{11} cm^{-2}. On the other hand, while the hysteresis on (0001) is small (0.1 V) at 300 K, it drastically increases to 2.4 V. The increase of hysteresis on (0001) is the result from the electron emission of 1.2×10^{12} cm^{-2} in density. These results indicate another evidence that the interface state density on 4H-SiC(0001) increases significantly toward the conduction band edge[22,23] and that on 4H-SiC$(11\bar{2}0)$ gradually increases as shown in Fig. 2.

In summary, the interface states near the conduction band edge at SiO_2/4H-SiC on the $(11\bar{2}0)$ and (0001) faces oxidized in wet O_2 ambient were characterized by a conductance method at 300 K and high-frequency $C-V$ measurements at 300 and 100 K. The $(11\bar{2}0)$ MOS capacitors showed a smaller interface state density near the conduction band edge than the (0001) MOS capacitors determined by the conductance method. The $C-V$ measurements at 100 K revealed a small increase in the flatband voltage shift and hysteresis on $(11\bar{2}0)$ and a large increase on (0001), by which the analysis using the conductance method was confirmed separately. The smaller interface state density at shallow energies on $(11\bar{2}0)$ should give favorable influence to 4H-SiC MOSFETs for obtaining a higher channel mobility.

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