Research Article

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Shock and impact reliability of electronic assemblies with perimeter *vs* full array layouts: A numerical comparative study

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Abstract: This study aims to assess the effect of the solder joint array layouts, including full and peripheral designs, on the mechanical response and reliability of electronic packages subjected to shock and impact loadings. Linear and nonlinear finite element simulations using the global-local modeling technique are employed to perform the analysis. Several peripheral array configurations are considered and compared to the full array systems. The results showed that, for optimum electronic package designs in terms of reliability and cost, it is highly recommended to use peripheral packages having three or four rows of solder interconnects in electronic systems under shock and impact loadings.

Keywords: electronic packaging, reliability, peripheral and full arrays, shock and impact

1 Introduction

Ball grid array (BGA) solder technologies are rapidly becoming of popular interest in designing electronic devices due to its cost-efficient properties [1,2], smaller size [3] and high input/output (I/O) electrical characteristics [4,5]. In fact, BGAs are commonly categorized based on the solder shape, *i.e.*, geometry, and array layout [6]. Actually, BGA reliability is highly dependent on the geometric factors of the joint, *i.e.*, diameter and standoff height [7–9]. For the layout configurations, peripheral (or perimeter) and full arrays are the most popular solder array or matrix layouts [10]. Generally, full arrays are available in most BGA component types while the perimeter configuration is widely used in wafer-level packages (WLP) and plastic ball grid array (PBGA) components [11]. Only a few published works are available for the reliability assessment of full *vs* peripheral array layouts. Using the finite element (FE) simulations, Chandran *et al.* [12] identified the location of solders with maximum damage to be at the package corner in both peripheral and full arrays in accelerated thermal cycling testing. In addition, their results showed that the risk of solder thermal fatigue is much possible in peripheral arrays than full array configurations. Such findings were recently confirmed with Gharaibeh's simulation-based work [13]. Liu *et al.* [14] used FE models to enhance the thermal reliability of peripheral WLP systems by installing dummy solder interconnects of larger sizes (height and diameter) at the array corner and around the corner. Titus and Jaiswal [15] discussed the reliability of solder balls of several arrangements of array designs considering different I/O counts. They found that the package with larger I/O count number could generally improve the solder interconnect thermal cycling reliability. However, BGA packages with high I/O counts and small pitch distance (distance between two adjacent joints) might lead to routing defects between the solders. Jung *et al.* [16] used two-dimensional (2-D) FE models to investigate the thermal fatigue characteristics of lead-based solders in both perimeter and full PBGA components. Their results showed that the full array layout systems could last longer than peripheral arrays. However, their results were based on FE numerical models with coarse mesh characteristics and the important and crucial in-plane deformations of the test package were not considered due to the use of 2-D models. Recently, Gharaibeh [17] discussed the random vibration reliability of perimeter and full BGA layouts using comprehensive nonlinear FE analysis. Gharaibeh's findings stated that in both array arrangements, the location of the critical solder joint is at the corner of the solder matrix. In addition, the value and the distributions of the critical solder stresses are not

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affected by the array type. Thus, the random vibration reliability is not influenced by the array layout. This was explained based on the fact that the outer solder rows/columns of the solder matrix carry most of the bending induced mechanical stresses and loadings while the inner interconnects do not meaningfully contribute to that. However, the use of peripheral arrangements could lead to electrical conductivity problems.

Based on the previous literature discussions, it is proved that most of the work done on the effect of the solder array configuration on electronic package reliability was limited to the thermal cycling and vibration loading conditions. Evidently, there is a lack of research studies investigating the behavior of full and peripheral solder layouts in drop, shock and impact loadings. Therefore, this article aims to bridge this research gap and discuss the mechanical behavior and reliability of electronic packages with both peripheral and full array configurations due to shock and impact loadings using computationally effective nonlinear finite element analysis (FEA) models with high-quality mesh properties.

This article begins with a detailed description of the package array layouts studied as well as the test assembly considered. Consequently, the FE modeling approach and global-local analysis techniques are fully presented. The correlations of the present FE models with modal analysis with hammer testing experiments are discussed, accordingly. Subsequently, a comprehensive presentation of the effect of solder matrix layout on the impact-induced mechanical behavior is explored. Finally, the present work provides useful design recommendations of BGA electronic packages exposed to shock and impact loadings.

2 Methodology

2.1 Area array layouts

In the present work, an integrated circuit (IC) package with body size of $17\,\text{mm}^2 \times 17\,\text{mm}^2$ and 1 mm thickness is centrally mounted on a squared printed circuit board (PCB) is considered. For the package layouts, a 16×16 SAC305 interconnect array with full (256 solder count) and 4-row peripheral (192 solder count) array systems are considered. The full and peripheral array layouts are designated in Figure 1 and the details of the tested configurations are summarized in Table 1.

2.2 FE modeling

ANSYS R17.1 is considered to build the FE model and to analyze the problem. For the FE mesh process in this model, only 3-dimensional hexahedron SOLID185 elements are generated to produce high-quality mapped mesh properties. During the modeling, only linear elastic mechanical properties are employed for the PCB, IC component and copper pads. However, for the SAC305 metallic alloy, both linear and nonlinear mechanical properties are considered. For the nonlinear material modeling, Anand visco-plastic constitutive material model [18,19] is implemented. All material properties are listed in listed in Tables 2 and 3. For the boundary conditions and to properly restrain the FE model, zero translational and rotational motions are imposed on the four corners of the PCB. This FE model is presented in Figure 2.

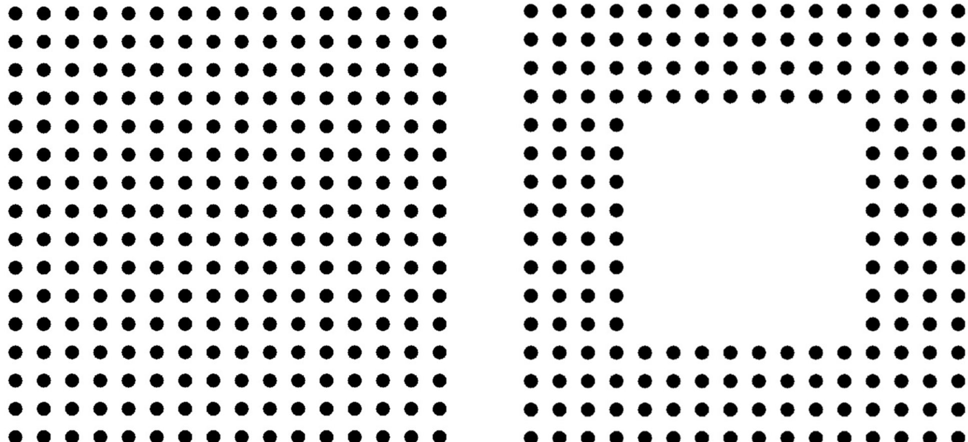


Figure 1: Solder array layouts: 16×16 full (left) and peripheral (right) arrays.

Table 1: Test configurations details

Part	Configuration
PCB size (mm × mm)	76 × 76
PCB thickness (mm)	1
Component size (mm × mm)	17 × 17
Component thickness (mm)	1
IC Package	16 × 16 full and perimeter area arrays
I/O count	Full: 256, peripheral: 192
Solder joint type	BGA
Solder joint alloy	*SAC*305
Solder joint height and diameter (μm)	300 and 280
Pitch distance (mm)	1

Table 2: Linear elastic material properties used in the FE model [20–22]

Material Parameter	PCB	Component	SAC305	Copper pads
Young's modulus (GPa)	32.0	27.0	43.0	120.0
Poisson's ratio	0.24	0.25	0.36	0.30
Density (kg/m^3)	3,000	1,100	7,400	8,800

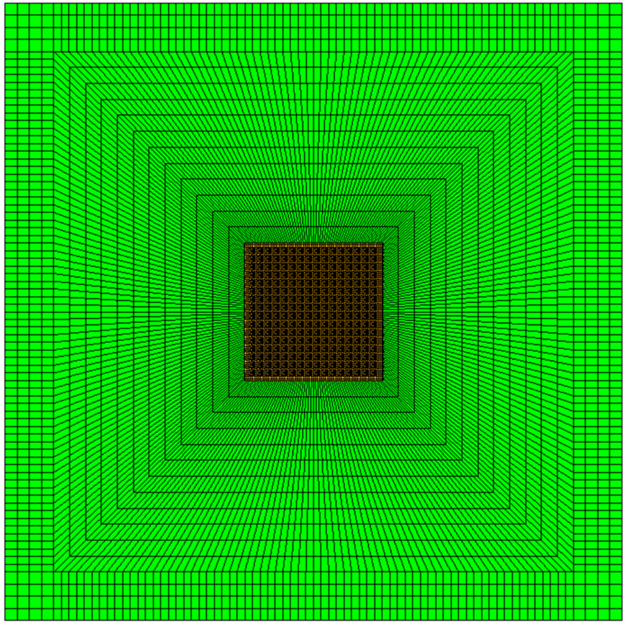
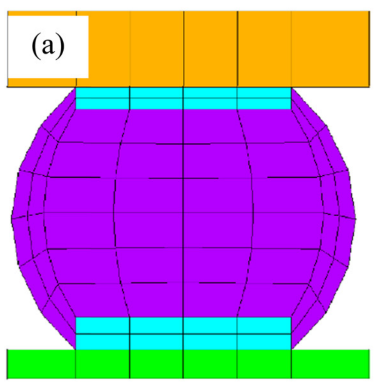


Figure 2: Finite element model.

In impact loadings, the electronic structure undergoes very large deformation and high strains during a very short period of time. In fact, performing nonlinear simulations in impact loading conditions is computationally very expensive in terms of computer run durations and memory as well as hardware resources usage. Nonetheless, it is very important to simulate the large deformations and the nonlinear behavior of the solder interconnect to reasonably estimate stresses and strains of the critical regions of the electronic structure, of course with computationally effective approaches. For this reason, the current study adopts the global-local modeling technique for executing the analysis for best results and for optimum simulation characteristics. This technique generally consists of two steps. In the first step, the global (full) model is executed using the mode superposition transient ANSYS analysis considering only linear mechanical properties for all parts of the electronic assembly. This step aims to simulate the overall deformations of the assembly with shortest simulation times. This is followed by the second and final analysis step in which a local model (submodel) of the most-critical solder interconnect, with improved mesh properties, is analyzed using nonlinear static analysis. The main goal of implementing the submodeling approach here is to generate and simulate an engineered and finely tweaked FE model of the most important solder joint.

Table 3: Anand model parameters used in the FE model for the SAC305 solder alloy [23]

Anand's parameter	Description	Units	SAC305
s_o	Initial value of deformation resistance	MPa	32.2
Q/R	Activation energy/Boltzmann's constant	1/K	9,320
A	Pre-exponential factor	s^{-1}	2,800
ξ	Stress multiplier	Dimensionless	4
m	Strain rate sensitivity of stress	Dimensionless	0.29
h_o	Hardening-softening constant	MPa	186,000
$\hat{s}$	Coefficient for saturation value of deformation resistance	MPa	44.67
n	Strain rate sensitivity of the saturation value	Dimensionless	0.0120
a	Strain rate sensitivity of the Hardening-softening	Dimensionless	1.72



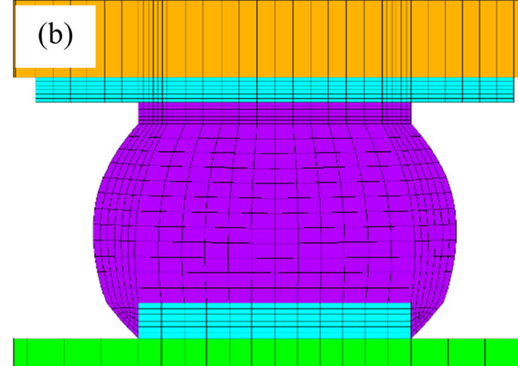


Figure 3: Solder joint used in (a) global model and (b) local model.

Figure 3 shows the corner solder joint mesh used in the full (global) model and in the submodel (local) configuration. In this submodel, the mechanical properties of the PCB, IC package and copper pads are remained linear elastic and are the same for the global model. However, the SAC305 solder mechanical properties in the local modeling are nonlinear for best solder stress computations. This is a common practice as it is very well known that the solder properties do not significantly influence the overall stiffness of the test assembly; however, solder stresses are highly dependent on the mechanical properties. If the nonlinear mechanical properties are plugged into the full model, the FEA simulation time will be very long and computationally intensive. Thus, the nonlinearities are only included in the local modeling. As a result, in this global-local modeling process, both accuracy and simulation efficiency are optimized.

Internationally, Joint Electron Device Engineering Council (JEDEC) recommends general rules and standards for conducting and simulating the reliability performance of electronic assemblies under shock impact loadings [23–25]. One specific JEDEC condition, namely JEDEC B-Condition, is widely used for the evaluation of SAC305 shock reliability performance. Therefore, JEDEC B-condition, which is characterized by a half-sine wave profile of 1,500 g's shock level with 0.5 ms pulse duration [24], is applied in the global model. In addition, a constant damping ratio of 55%, as extracted from [26], is used in the analysis. As mentioned previously, only static analysis is employed in the local to investigate solder stresses, which are induced by the transient analysis of the global model, of all tested array layouts. The application of degrees of freedom interpolations on the cut boundaries process is performed at the time instance with maximum PCB out-of-plane deflections as shown in the subsequent sections.

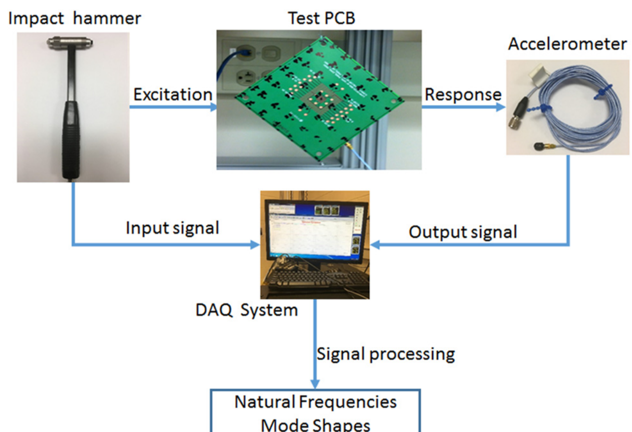


Figure 4: Modal analysis experiment.

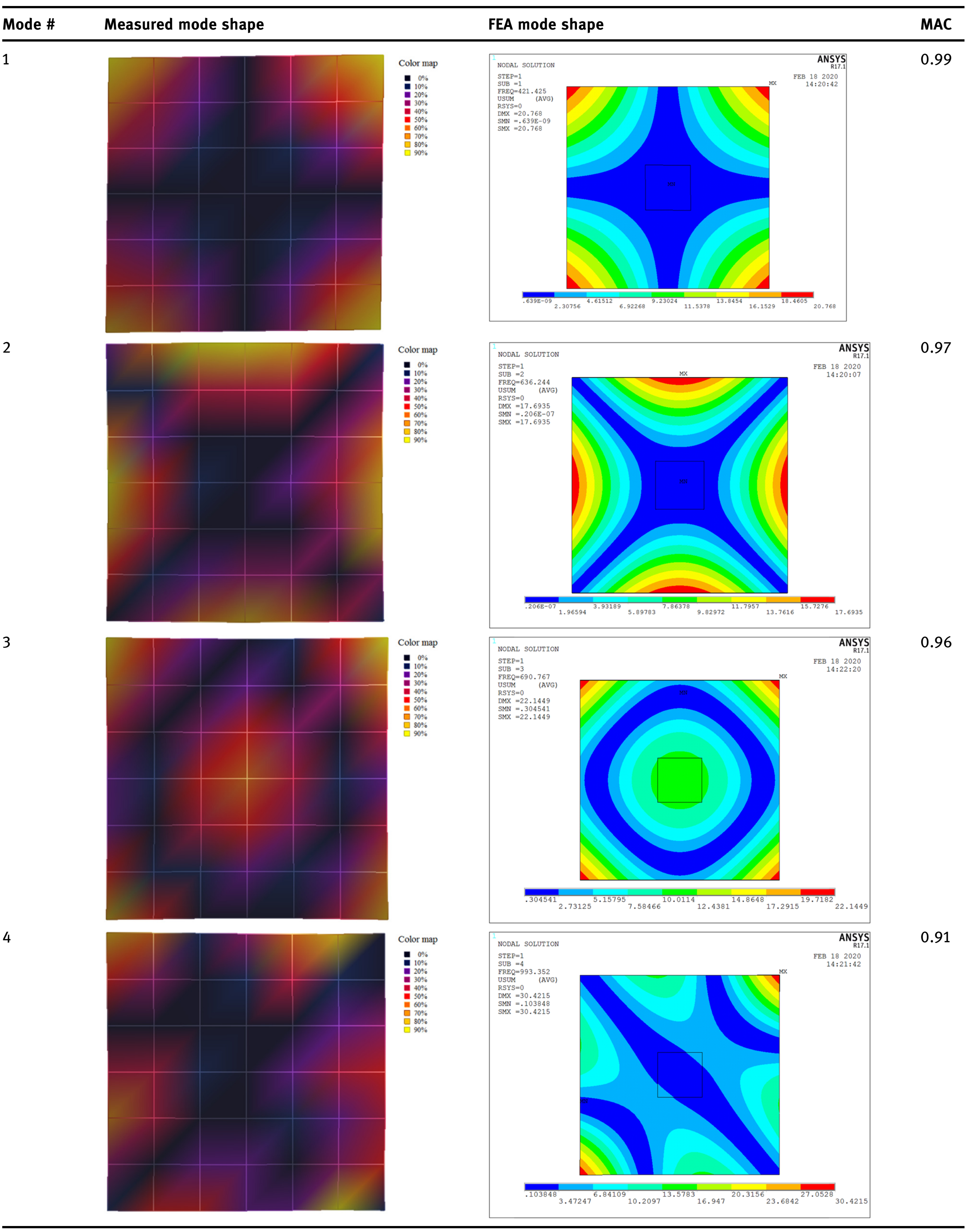
Table 4: Modal analysis experimental setup details

Equipment	Make and model number
Impulse hammer	PCB Piezoeletronics 086C01
Accelerometer	PCB Piezoeletronics 352C23
DAQ system	National Instruments NI-DAQ 4431
Software	Spectral Dynamics STAR Version 7.2

Table 5: Natural frequencies correlation results

Mode number	Experiment natural frequency (Hz)	FEA natural frequency (Hz)	% Error
1	422	421	−0.24
2	626	636	1.60
3	770	691	−10.34
4	1,036	993	−4.25

Table 6: Vibratory mode shapes correlation results



Mode #	Measured mode shape	FEA mode shape	MAC
1			0.99
2			0.97
3			0.96
4			0.91

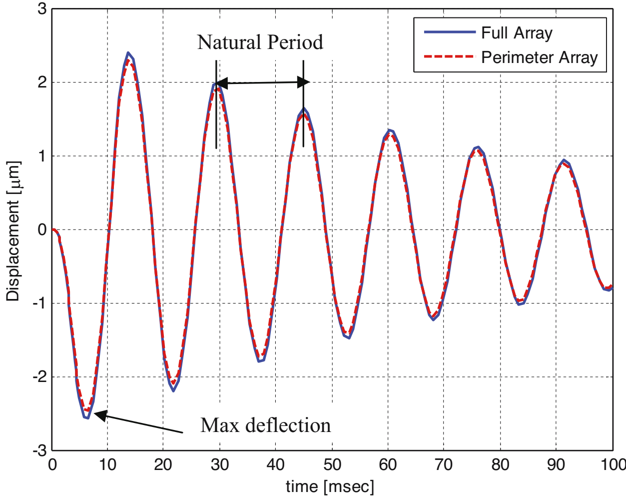
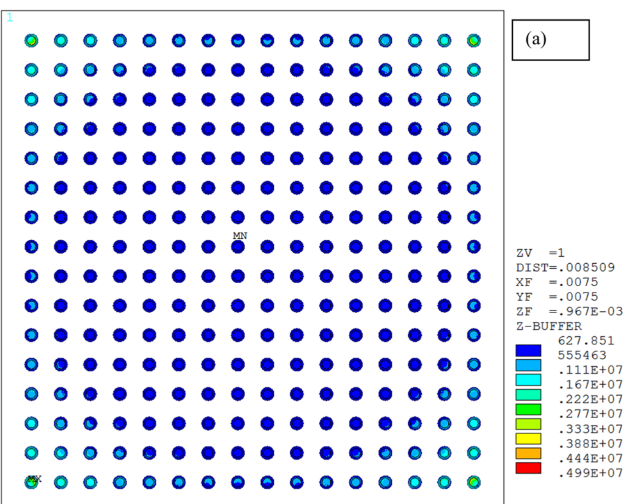


Figure 5: Time response of the out-of-plane deflections of the PCB in full and perimeter rray.

2.3 Modal analysis experiment

Like any other numerical approach, the results of this FE model are required to be validated and correlated. Thus, the current FEA model is correlated with modal analysis with hammer testing experimental findings in terms of the basic dynamic characteristics, *i.e.*, natural frequencies and mode shapes. In other words, the free vibration data (natural frequencies and mode shapes) of the FEA model are systemically compared to their corresponding experimental results and hence discrepancies are quantified by the relative error in the resonant frequencies and modal assurance criterion (MAC) number for the mode shapes. Throughout this correlation process, free boundary



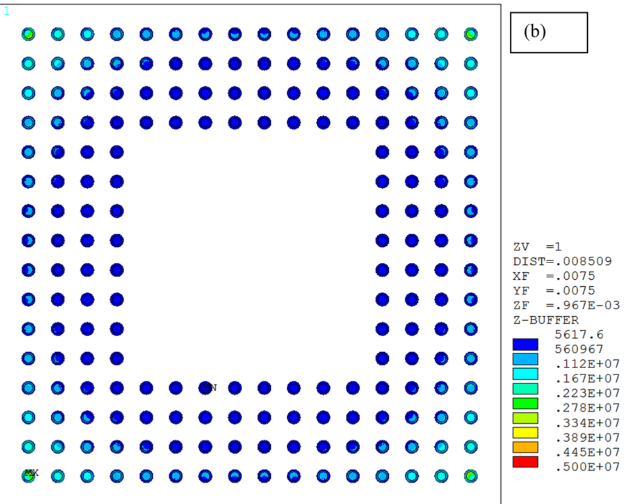


Figure 6: Von Mises stresses of the solder matrix in (a) full and (b) peripheral layouts.

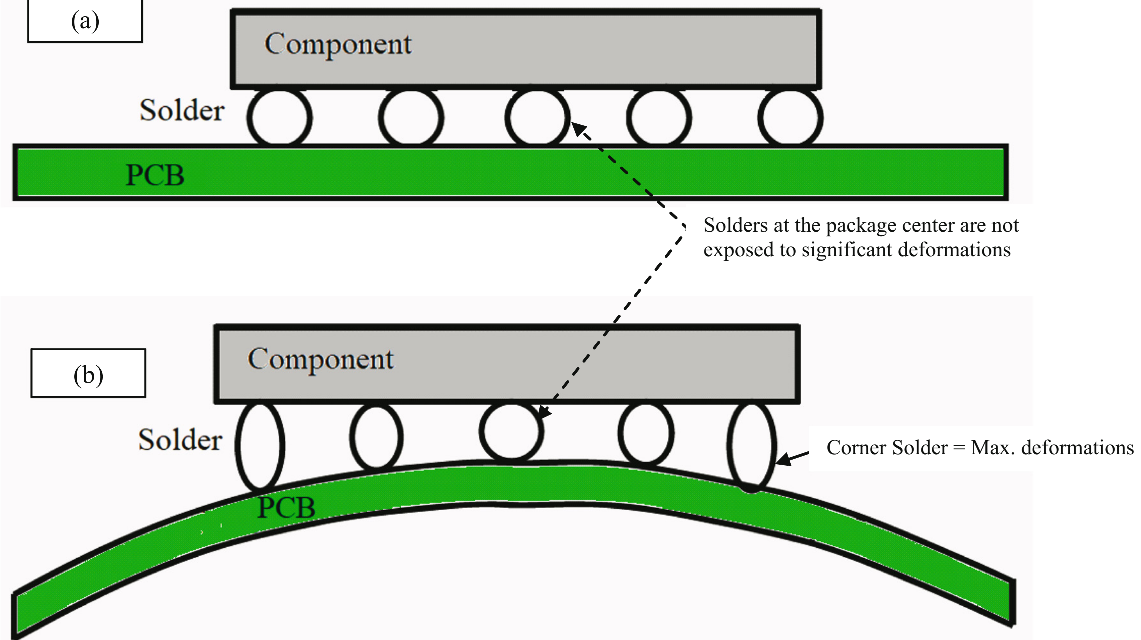
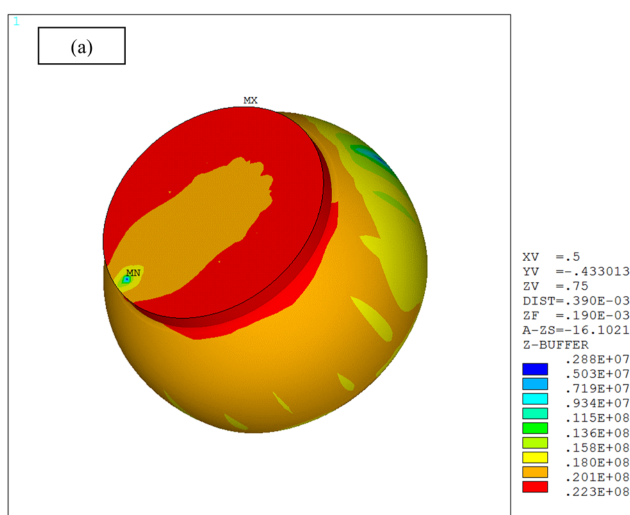


Figure 7: Schematics for (a) nondeformed and (b) deformed electronic package after bending due to vibration.

conditions are considered, and the first five vibratory modes are tested.

For the details of the modal analysis experiment, the setup is composed of an impact hammer (exciter), a data acquisition system (DAQ), a light-weight accelerometer, a computer and the test vehicle. Table 4 lists all the specifications of this setup. For the measurement procedure, a 7-by-7 equally spread-out grid is marked on the test sample. The hammer is accordingly used to softly tap the assembly at each measurement point (total of 49), while the board accelerations are continuously measured using the accelerometer. For more accurate measurement, the average of three consecutive taps is computed and hence considered. Consequently, the transfer function between the output acceleration and the input hammer force is acquired using the DAQ device. Finally, the PUMA V7.2 software from Spectral Dynamics is used for the modal data generation. Figure 4 shows the schematics of the test and a photograph for the actual test piece.

The results of this validation analysis, detailed in Tables 5 and 6, show that the FEA natural frequency and mode shapes are in a very good agreement with the corresponding measured data. As a result, the present FE model can be further employed with confident to perform the rest of the analysis in this work.



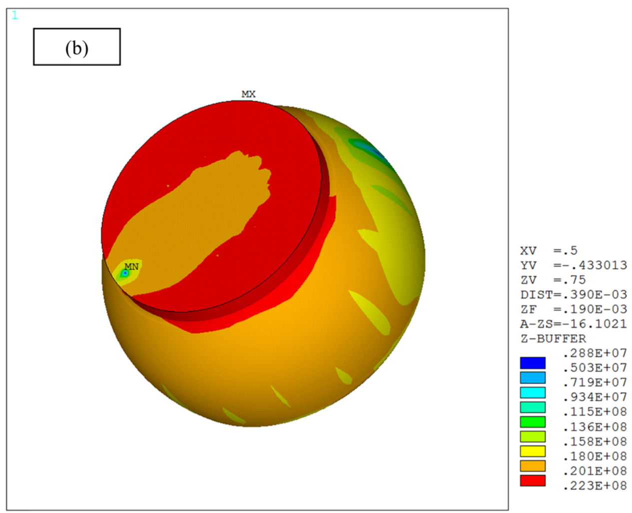


Figure 8: Critical solder joints von Mises stress distributions in (a) full and (b) peripheral arrays.

3 Results and discussions

3.1 Board deflections

Figure 5 shows the time response of the transverse deformations (U_Z), in both full and perimeter array layouts, at the PCB center due to the applied shock profile. The first conclusion that can be drawn here is that the boards with any array configuration have the same natural frequency as the natural period time is the same for both systems. Another important observation is that the maximum lateral deflection of the PCB is almost the same for both array configurations. Specifically, in full array U_z = 2.57 µm and in the perimeter array U_z = 2.46 µm with the relative difference percentage of 4% approximately. As it is already known, solder stresses are highly dependent on the PCB deformations. Full discussion on solder stress analysis will be shown in the following subsection.

3.2 Solder interconnects stress analysis

Figure 6 presents the von Mises stress contour plots of the studied configurations. The figure shows that, in both array styles, the corner joint is the joint with highest stress value, *i.e.*, the most critical solder interconnect. This is due to the bending difference between the PCB and the IC package is often maximum at the package corners. In addition, the stress contour plots show that the solder stresses of the peripheral array are very similar to the stresses of the corresponding interconnects of the full array system. This is true for both solder stress values and distributions. Such findings suggest that for a 4-row/column perimeter array and the full array layouts, the interconnect matrix type does not affect solder stresses. Therefore, the solder located at the outer rows/ columns of the matrix undergoes most of the mechanical loading induced by the drop impact and the solder of the

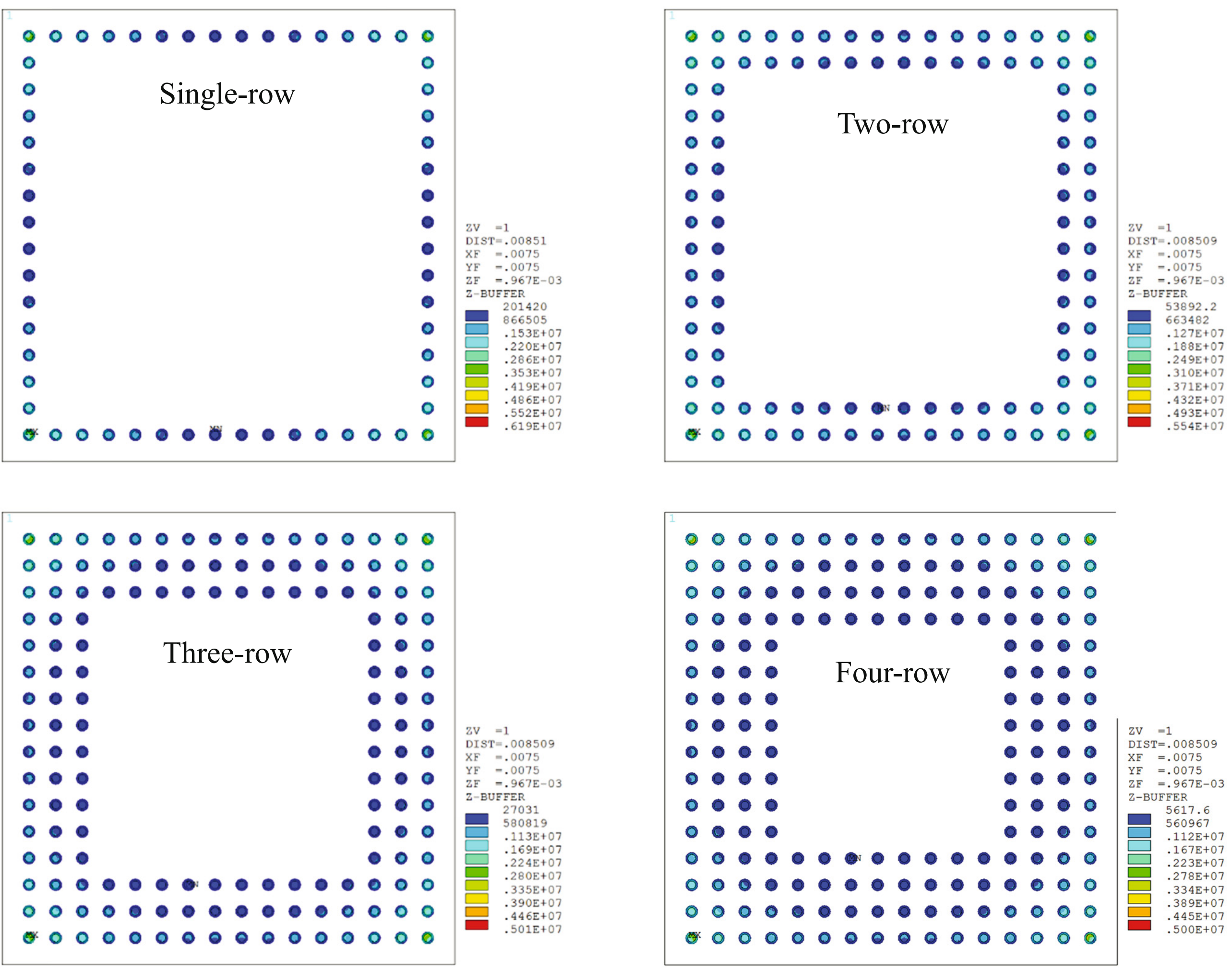


Figure 9: Von Mises stress distributions of the interconnect array in one-, two-, three- and four-row partial array configurations.

inner columns and rows does not exhibit much of the deformations, as explained in Figure 7. From a financial point of view, the use of peripheral arrays is highly preferable, and it could lead to cheaper electronic assemblies' designs, as less number of solder interconnects are required. However, the use of partial array systems must not interfere with the electrical properties, *i.e.*, conductivity properties, of the electronic system.

For a closer look on the critical interconnect, *i.e.*, corner joint, the submodel is considered, for both array schemes. Figure 8 presents the von Mises stresses in the critical joints. The plots show that solder stress distributions and values are the same in both peripheral and full array layouts. In addition, the maximum stress in the solder is located at the top (component side). Therefore, the solder mechanical failure due to impact loadings is expected to be the same in both array systems and this failure is more likely to occur at the component side of the outer most interconnect.

For deeper analysis and understanding of the difference between solder failure in full and perimeter array configurations, an additional FEA investigations are performed. In these investigations, a peripheral array component with four, three, double and single rows (or columns) of the 16 × 16 solders are modeled and hence analyzed. The loading and boundary conditions used in this analysis are the same of the previously described conditions. Figures 9 and 10 illustrate the von Mises stress results of this investigation for the arrays considered and the corner interconnects of each system. The stress findings demonstrate that the location of the solder with maximum stress is not affected by the number of the rows available in the partial array and this location is at the corner of the interconnect matrix. In addition, the critical solder (corner solder) stress distributions of the single row configuration are slightly different than those of the configurations with two-, three- and four-row/column arrays, especially around the solder upper neck. In the one-row system, higher stresses are surrounding

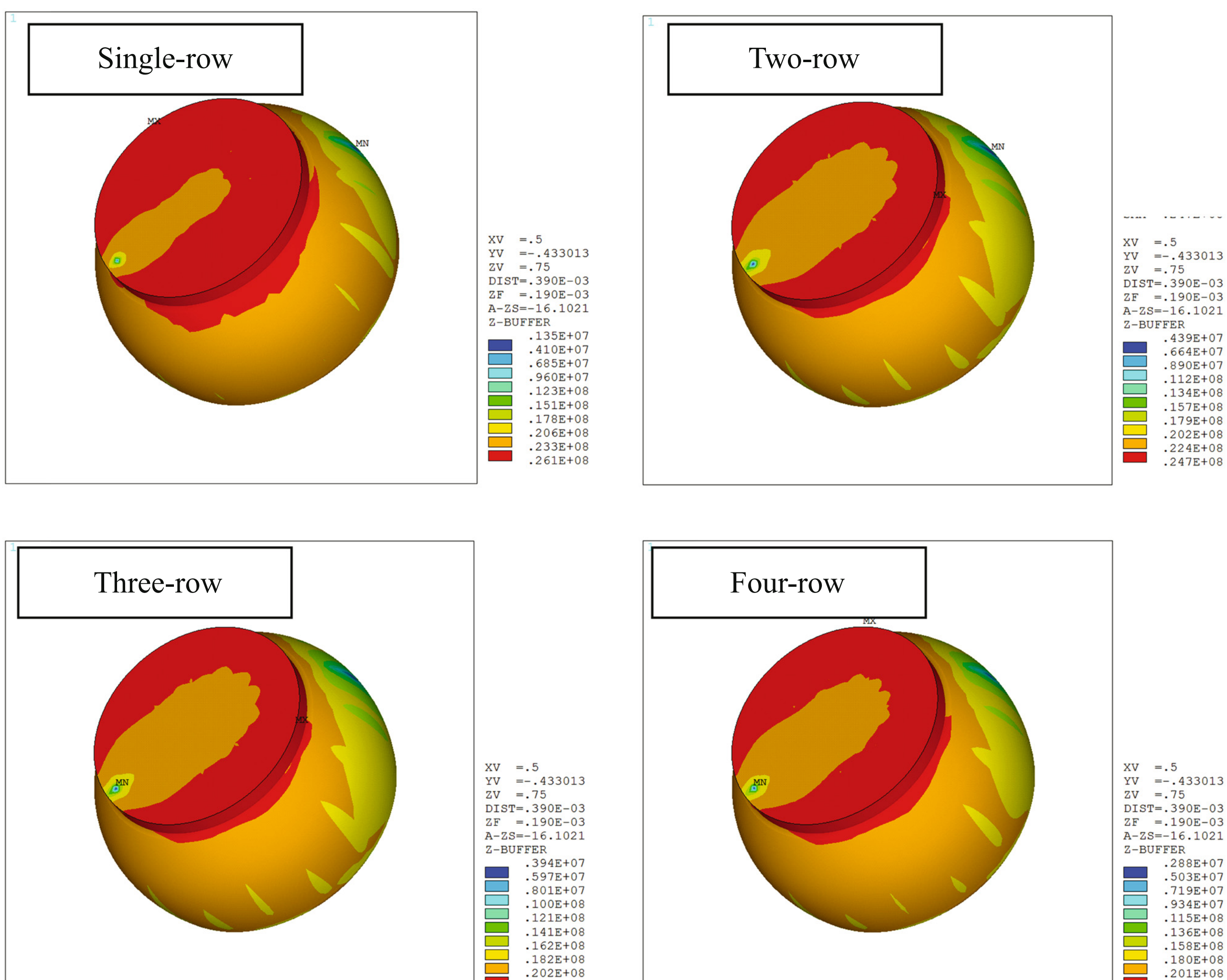


Figure 10: Von Mises stress distributions of the critical solder interconnect in one-, two-, three- and four-row partial array configurations.

Table 7: Solder maximum von Mises stress results in several row configurations

Number of rows in the partial array	von Mises stress (MPa)
1	26.1
2	24.7
3	22.3
4	22.3

the solder upper neck which further facilitates the solder failure, *i.e.*, crack.

Table 7 lists the maximum von Mises stress values of all tested partial array configurations. The results here show that solder stresses are higher for the single row system (26.1 MPa) and it is reduced as more rows and/or columns available in the package array till the stress value reaches a constant value (22.3 MPa) in the configurations of 3 and 4 columns. In other words, the maximum stress in the single row configuration is 17% higher than that of in the 3- or 4-row systems.

This phenomenon can be justified again using Figure 7. Considering the deformed shape of this figure, the explanation is that the outer rows/columns of the solder ball array do the heavy lifting of the bending-induced mechanical loading while the inner most interconnects do not effectively participate in the loading carrying process. Thus, if the inner joints are not included in (or removed from) the array that would not appreciably affect the outer solders deformations and stresses.

As a result of this discussion, the present work recommends integrated packages with 3- or 4-row/column peripheral arrays designs for cheaper and more dependable electronic structures exposed to shock and impact loadings.

4 Conclusions

Extensive linear and non-linear FE analysis simulations were conducted in the present work to investigate the effect of the solder array layouts, peripheral *vs* full, on the mechanical behavior and reliability performance of electronic assemblies due to impact and shock loadings. In this investigation, a 16×16 integrated package with full and 4-row/column perimeter arrays was thoroughly examined. Using the global-local advanced modeling technique, it was shown that there is no significant difference between the solder behavior and stresses in the full and the 4-row/column peripheral array layouts. Nonetheless, the work was extended to examine the influence of the difference perimeter array configurations including single, double and triple rows, in addition to the 4-row, partial array systems on solder stresses and hence reliability performance. The findings showed that peripheral arrays with fewer rows/column (single and double) will end up with higher solder stresses and less reliable electronic packages. Also, the solder maximum stress reaches a stable minimum value in solder array layouts with triple and quadrable rows/columns. Thus, the present work recommends the use of packages with peripheral arrays of three or four solder rows for financially competitive and reliable electronic assemblies undergoing shock and impact loadings.

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