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ORIGINAL RESEARCH

Short Communication: An Updated Design to Implement Artificial Neuron Synaptic Behaviors in One Device with a Control Gate

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Background: As a key component in artificial intelligence computing, a transistor design is updated here as a potential alternative candidate for artificial synaptic behavior implementation. However, further updates are needed to better control artificial synaptic behavior. Here, an updated channel-electrode transistor design is proposed as an artificial synapse device; this structure is different from previously published designs by other groups.

Methods: A semiconductor characterization system was used in order to simulate the artificial synaptic behavior and a scanning electron microscope was used to characterize the device structure.

Results: It was found that the electrode added to the transistor channel had a strong impact on the representative transmission behavior of such artificial synaptic devices, such as excitatory postsynaptic current (EPSC) and the paired-pulse facilitation (PPF) index.

Conclusion: These behaviors were tuned effectively and the impact of the channel electrode is explained by the combined effects of the joint channel electrode and conventional gate. The voltage dependence of such oxide devices suggests more capability to emulate various synaptic behaviors for numerous medical and non-medical applications. This is extremely helpful for future neuromorphic computational system implementation.

Keywords: artificial synapse, thin-film transistor, channel-electrode transistor, neuron behavior control

Introduction

In view of common electronic devices, numerous materials, such as silicon-on-insulator (SOI) and nanotubes, can be used.[1–4] In addition, numerous papers focused on artificial synapses have been reported, such as two-terminal memristors[5] and devices with three-terminals which have been proposed to mimic artificial synapse functions.[1,6-10] While memristors have reliability issues or are hard to fabricate,[24,25] three-terminal transistors have been developing for several decades and are appropriate for artificial synaptic realization.[16,26] Presynaptic spikes could be emulated by voltage pulses applied on the gate electrode, while the synaptic weight is represented by channel conductance. Typical synaptic behaviors, including excitatory postsynaptic current (EPSC) and paired-pulse facilitation (PPF), have been reported.

The traditional method uses CMOS-based transistors (Metal-Oxide-Semiconductor Field-Effect Transistor, MOSFET) to emulate an artificial synaptic signal; however, the MOSFET synapse needs several transistors to emulate one signal and the energy

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dissipation of a MOSFET synapse is much higher than natural neurons.[20,27] Other synaptic transistors include ferroelectric field-effect transistors[28,29] and electric double layer transistors.[20,26] Meanwhile, amorphous oxide semiconductor (AOS) materials have attracted much attention due to their optimal properties, including room temperature fabrication conditions, transparency, and electrical properties.[1,11] AOS materials such as IGZO (In-Ga-Zn-O) have been reported as resistive change materials in two-terminal resistive-switching memory for artificial synapse emulating.[5] The oxygen vacancies in the amorphous oxide semiconductor serve as mobile carriers, which could simulate the mobile ions in real neurons.[5,30] Synaptic behaviors from different dimensions have been investigated for the first time in our present design. Two-dimensional presynaptic spikes, which are similar to real life, are of importance and interest to build biological systems, such as neuron synapses.

In this paper, an updated channel-electrode transistor (CET) design is proposed to realize artificial synaptic devices (Figure 1E). The configuration has only one transistor together with an additional electrode jointed in the channel (ie, channel electrode, CE), and a side electrode as the side gate (SG). With a vertically coupled bottom electrode, a channel electrode and a lateral side electrode as the presynaptic terminal, this design could emulate synaptic behaviors in three different directions. It might be helpful to push the development of neuromorphic computation integrated circuits (IC) in the future.[31]

Figure 1A–E shows a 3-dimensional schematic comparison among the published designs and our new structure. Some have more layers and the others have more of a footprint than our design. The CET design with a conventional bottom gate and a vertically stacked channel electrode and a lateral side gate could better simulate the synaptic behaviors, which is different from previously published designs by other groups. The electrodes could use conductive materials such as metals and ITO. Here, the control gate uses Ni/Au, which was deposited together with the drain and source electrodes. The CET could be realized with a foundry process at present. Here, we use an amorphous oxide semiconductor (AOS) thin-film transistor (TFT) process[12] to realize our CET. The AOS TFTs have many good properties, such as a low-temperature process, high uniformity over large areas and high-stress stability, which suggests wide applications in portable electronics and displays.[11,13] IGZO TFTs were used in this study to realize our design.

Experimental Section

For the fabrication, initially, IGZO channels were grown by radio-frequency sputtering on a Si wafer and patterning by lithography, the Si wafer served as the bottom gate and gate dielectric layer. IGZO channels with a 3~36 nm thickness were selected for our investigation here. The channel width and length were about 100 μm and 90–120 μm, respectively, and the dimension of the channel could be decreased by lithography methods and could be as short as a nanometer.[14] The thickness of our IGZO semiconductor can be adjusted by tuning the deposition time from 3 nm to 36 nm. The devices with a channel thickness of 3 nm showed stable electrical properties in our experiments.

After the IGZO semiconductor channels were deposited and patterned, the mask patterns of the metal electrodes were transferred to the wafer. Ni/Au metal electrodes (ie, the source, drain, channel electrode, and side electrode) with about a 100 nm thickness were deposited by electron beam evaporation techniques and further developed. The electrode is metal but not limited to metal, and could also be ITO or

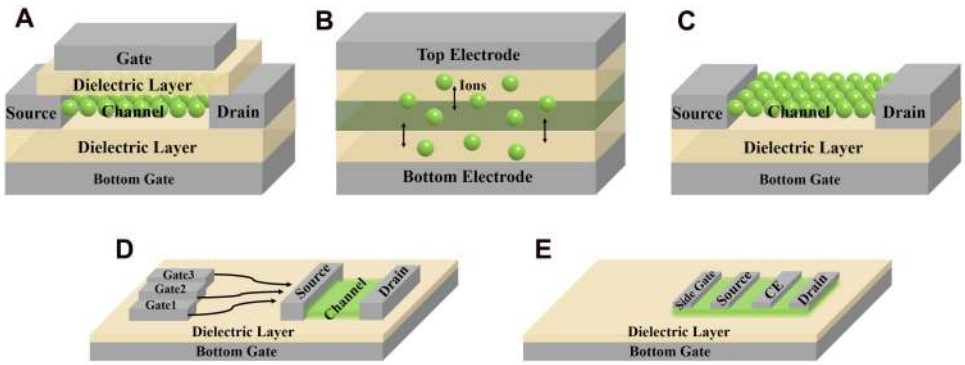

Figure 1 3D schematic comparison of the previous structures and our structure. (**A**) Hybrid heterojunction based synapse.[8] (**B**) Synaptic devices based on ion-exchange kinetics.[5,6,9] (**C**) Electric-double-layer transistor-based synapse.[7,10,19] (**D**) Side gate approach for synaptic behavior control.[20] (**E**) Our channel-electrode transistor (CET) design, with fewer fabrication processes and less area cost.

other conductive materials. Different electrode materials will lead to different experimental results due to their instinctive work function and a different band structure between the electrode and active material. This structure fabrication process, which is typical for a transistor, suggests a good assembly possibly more complex than integrated devices.

Electrical properties were measured by a semiconductor characterization system (Keithley 4200), where the source voltage was set to 0 V and the drain voltage was constant. The pre-synaptic spike was simulated by the voltage applied on the channel electrode (ie, control gate), side gate or the bottom gate. The excitatory postsynaptic current was simulated by the channel current (ie, the current between the drain and source electrode).

Results and Discussion

The synaptic behavior could be obtained by CET with a control gate (Figure 2). In order to obtain the EPSC, a −2 V presynaptic spike was applied to the control gate, which stimulated an EPSC amplitude of over 20 μA. The EPSC reached a peak value and decreased gradually, which is similar to the nonlinear transmission characteristic of a biological synapse.[15] It is worth noticing that the EPSC here was obtained on a device with an IGZO layer thickness of only 3 nm, which is shown in the insert in Figure 2A. As the fitting line shown in Figure 2A, the decay of EPSC can be described by a stretched exponential function:

$$I = (I_0 - I_\infty)\exp\left[-\left(\frac{t-t_0}{\tau}\right)^{\beta}\right] + I_\infty \quad (1)$$

where τ is the retention time, t_0 is the time when the presynaptic spike finishes, I_0 is the triggered EPSC, and I_∞ is the postsynaptic current at the end of the presynaptic spike. The τ is estimated to be ~2 μs, which means the feature time of the mobile carrier migration is about 2 μs. This representative artificial synaptic transmission behavior is due to the mobile carriers in the amorphous oxide, which depends on the oxide components,[1,22] which is similar to those in cation transport among neurons. The oxygen vacancies in the IGZO channel layer serve as the majority carriers, and the artificial synaptic transmission behavior is due to oxygen ion migration and diffusion.[5,30]

The synaptic behavior of CET could be obtained with a side electrode as the side gate (Figure 2B). When stimulated by a 6 V and 150 ms width spike, an EPSC amplitude of over 2.2 nA was obtained. As shown in Figure 2B, the energy dissipation was 5 pJ, which is on the same order of the aim of power dissipation for neuromorphic systems

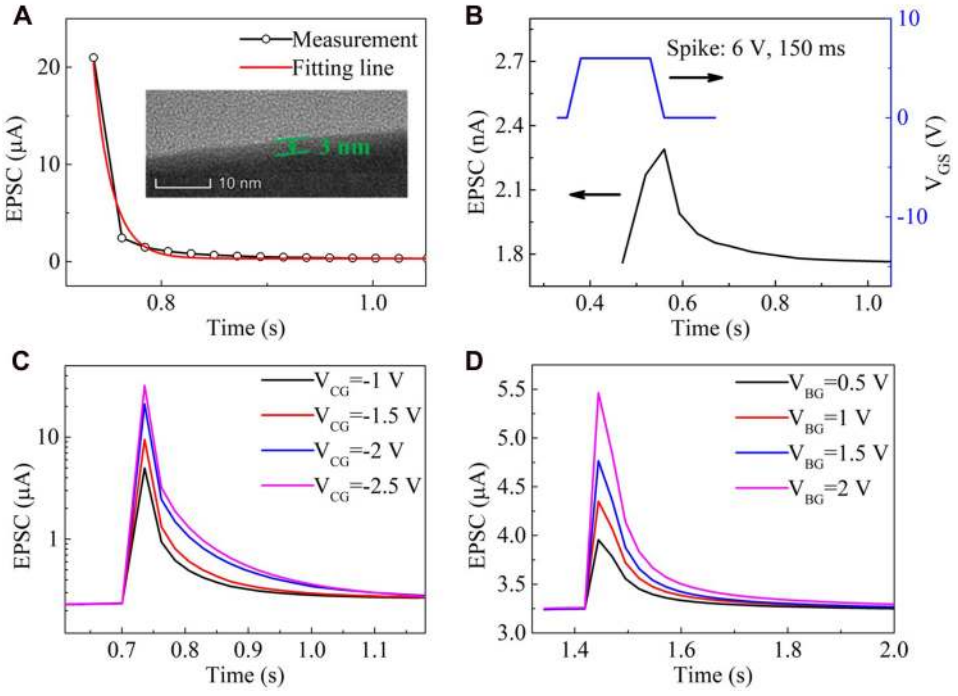

Figure 2 EPSC behavior of CET. (**A**) EPSC triggered by a presynaptic spike on the channel electrode as the control gate, with fitting by a stretched exponential function. Inset is the cross-section of the 3 nm thick IGZO channel layer between the ITO electrodes and the dielectrics layers. (**B**) EPSC decay experimental behavior triggered by a presynaptic spike on the side gate. (**C**) EPSC triggered by a presynaptic spike on the control gate with different amplitudes, with a 25 ms pulse width. This shows the control gate could show EPSC without a bottom gate. (**D**) EPSC triggered by a presynaptic spike on the bottom gate with different amplitudes, with a 25 ms pulse width.

and much lower than the reported CMOS-based artificial synapse.[16,21,32] Here, both the width and length of our sample were on the order of 100 μm. Given a smaller dimension, the current and thus the power dissipation could be reduced. A postsynaptic neuron could be triggered to establish a dynamic logic by the spatiotemporally correlated stimuli from various neurons.

As shown in Figure 2B, the EPSC was controlled under the same voltage by the side gate and was much lower than that by the control gate in Figure 2A. This is consistent with the mechanism for the different structures, with the side gate adjusting the channel in a far separated location and the control gates directly adding to the channel. As shown in Figure 2C and D, both the control gate and the bottom gate have a more direct impact on the channel than the side gate. The EPSC stimulated by the same voltage on the control gate and bottom gate could reach a peak value of μA level, which is far greater than on the side gate. This suggests that a similar synaptic effect is easier to achieve by applying spikes on both the bottom gate and control gate than on the side gate. A vertical coupled gate (bottom gate and control gate) has a stronger impact on device conductivity and thus on the synaptic behavior than that with a lateral side gate. In the real life, neurons have connections from junctions in various directions. We could also note that the impact of the connections from various directions could be emulated, by adjusting the voltages in both the vertical and lateral dimensions.

The transient current arises from states highly localized in energy and is assumed to follow the function *exp(-et)*,[2,3] where *e* in the function is the emission rate of the carriers and *t* is the transient time after the pulse. Therefore, *e* is related to the energy level where the carriers emit. If only one *e* is given, the curves show obvious deviation. If two *e*, which are correlated to different gates are given, ie, $1/e_1$ ~0.5 μs and $1/e_2$ ~0.2 μs, the calculated curve could be found to fit the transient measurement current well. Therefore, we propose a model for transient current for AOS as follows:

$$I(\mathrm{t}) = I_{01}\ \exp(-e_1 \cdot t) + I_{02}\ \exp(-e_2 \cdot t) + \ldots + I_{0n} \exp(-e_n \cdot t) \quad (2)$$

where e_n corresponds to the No. n gate if there are more than 2 gates and n is the number of the gates which could control the channel including the channel electrodes acting as control gates. This is reasonable for different *e* corresponding to different gate impacts because it was found that there was an element of localized trap in the deep states, which should have different emission time from the element of the shallow trap in the states near *Ec*.[17] As suggested in Figure 2C and D, both the control gates and the bottom gates could control the EPSC shape. Therefore, there should be at least one additional element to the transient current with another emission time, with a control gate pulse and another bottom/side gate pulse. Therefore, the channel after being turned on should have two emission times for the gate control from the bottom gate, control gate, and other gates. The model for AOS is different from the conventional model.[3] This shows that we could adjust the artificial synaptic behaviors on both the amplitude and different transition times.

The mobile carriers in the amorphous oxide depend on the oxide components.[1] As shown in Figure 3A, the EPSC was triggered by two successive presynaptic spikes on the control gate with a spike amplitude of 1 V and 1.5 V, the EPSC triggered by the second spike is larger than the first one. The phenomenon is called paired-pulse facilitation (PPF), in which EPSC evoked by the second spike increases when it follows a previous spike closely (25 ms interspike interval here). PPF is a form of short-term synaptic plasticity and is reported to be important for decoding temporal information in the biological system.[15] The PPF phenomenon in our CET is due to the oxygen vacancy migration in the IGZO channel layer, when applying a presynaptic spike on the control gate, the oxygen vacancies concentrated near the control gate and diffused slowly into the bulk; when applying the second presynaptic spike, the oxygen vacancies resided near the control gate augmented with the oxygen vacancies triggered by the second spike, thus results in a larger EPSC. The PPF index, ie, the ratio of max EPSC2/max EPSC1, as a function of the interspike interval is shown in Figure 3B. The interspike interval Δt_{pre} is between the two subsequently correlated spikes on the control gate. As seen in Figure 3B, the PPF index reaches a peak value and gradually decreases as the interspike interval increases, the PPF index reaches 1.4 with a Δt_{pre} of 25 ms and could maintain 1.03 after 300 ms. It was found that there is an elevation in responsiveness for the second spike when two spikes are less than 300 ms apart. Therefore, the shorter the Δt_{pre} is, the higher the PPF index would be for a pair of spikes on the control gate, which is consistent with the time-related oxygen vacancy migration. These behaviors were also found in the situation for the bottom gate.

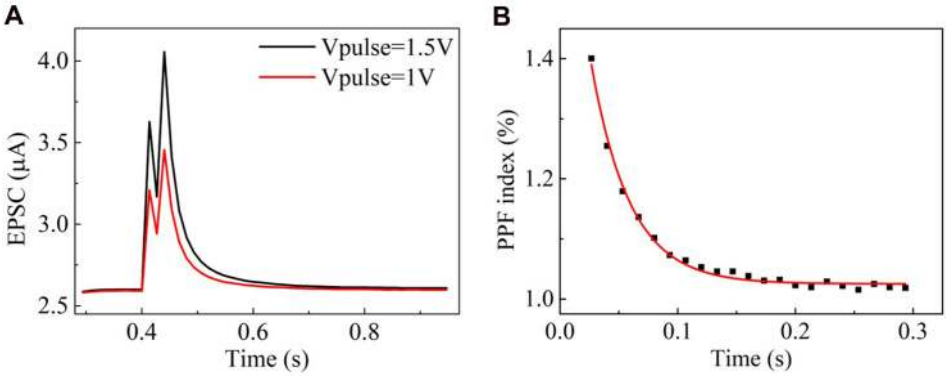

Figure 3 (**A**) Paired-pulse facilitation (PPF) behavior. EPSC triggered by a pair of consecutive spikes at 1 V and 1.5 V, the PPF behavior could be observed. (**B**) PPF index, ie, the ratio of A2/A1, as a function of interspike interval (presynaptic spike of 1 V, interspike interval from 25 ms to 300 ms).

Another short-term plasticity behavior is shown in Figure 4A, when stimulated by a series of spikes on the control gate, the channel conductance (ie, synaptic weight) gradually increased and can last for tens of seconds after the spike, which shows a post-tetanic potentiation (PTP) behavior.[7,23] The amplitude of the triggered spike is 1.5 V, with a 25 ms pulse width, and an interspike interval of around 50 ms. It is worth mentioning that with this CET structure, long-term potentiation (LTP) behavior could be obtained by changing the channel materials. The synaptic potentiation and depression behaviors are shown in Figure 4B, the EPSC amplitude (ie, synaptic weight) gradually increased when stimulated by sequential positive spikes (1 V, 25 ms), and decreased when following negative spikes (−0.5 V, 25 ms).

When two parallel-connected synapses were triggered by a presynaptic spike, the EPSC from different synapses would show a combination effect. The combination would be a dynamic analogue function of time. The EPSC as a function of Δt_{pre} (the interspike interval, Δt_{pre} is the time gap between the two presynaptic spikes when they finished) is shown in Figure 4C. The responses of the post-synapse

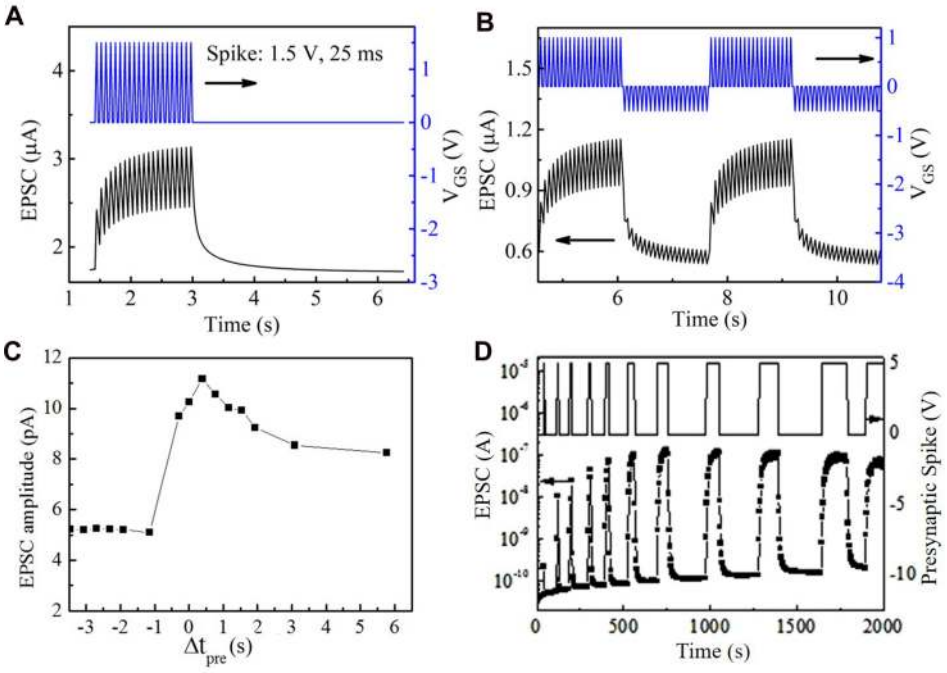

Figure 4 (**A**) CET stimulated by a series of 1.5 V, 25 ms presynaptic spike, the channel conductance increased temporarily, which shows a short-term plasticity behavior. (**B**) Synaptic potentiation and depression behavior mimicked by a sequential stimulus train. (**C**) Dynamic logic. EPSC triggered by presynaptic spike 1 and spike 2 on the control gate. (**D**) Drain current responses to different gate pulses with different amplitudes.

are measured with a presynaptic spike of 1.5 V and a constant drain voltage V_{DS} of 2 V. When Δt_{pre}=0, the presynaptic spikes applied simultaneously on the two parallel-connected synapses, the EPSCs from the postsynaptic terminal augmented and thus resulted in a combined EPSC, which is larger than the linear sum of EPSC 1 and EPSC 2. This super-linear amplification behavior is similar to what is observed in hippocampal CA1 pyramidal neurons.[18]

As shown in Figure 4D, the response to the gate pulse of the drain current is similar to the synapse behavior in the nervous system.[5] The channel conductance could be adjusted by the voltage pulse duration and amplitude. As shown in Figure 4D, the drain current increases with a presynaptic spike of longer pulse duration, and eventually rose to a maximum. These nonlinear transmission characteristics corresponding to different pulses are very similar to the behaviors of the synapse after the different stimulations in the central nervous system.[5] This suggests that the design has the potential ability to realize short-time memory and long-time memory.

Conclusion

In summary, a strategy with a channel electrode is proposed here for artificial synaptic electronics and AI computing. In this strategy, a simplified single-channel transistor, ie, CET, was shown to realize synaptic functions with both a conventional gate and control gates connected to the channel directly. This device, under a driving voltage of no more than 2 V, could be accomplished by standard processes. This study showed that the CET employing advanced semiconductor materials emulated and opened the door for improved neuron behavior control and understanding. This CET device could be appealing for neuromorphic computation circuits as well as other bioinspired applications.

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Disclosure

The authors report no conflicts of interest in this manuscript.

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