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Short-Time Fourier Transform Based Transient Analysis of VSC Interfaced Point-to-Point DC System

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***Abstract*—The transient response of the voltage source converter (VSC) interfaced DC system is significantly different from the AC counterpart. The rapid discharge current from the DC-link capacitors and the vulnerability of the free-wheeling diodes during short-circuit in DC grid demands the transient detection algorithm to execute within few milliseconds. The rapidly rising fault current in DC grid is expected to have high frequency components which might be an effective indicator of the transient condition. This paper presents quantitative investigation of the high frequency components utilizing Short-Time Fourier Transform (STFT) during transient conditions. Detailed operating principle with various factors affecting the STFT operation such as ripple content of the input DC signal and window type & length have been thoroughly investigated. STFT algorithm is able to detect low impedance faults within 1 ms and high impedance faults in 2 ms. Moreover, it is able to distinguish between short-circuit fault and less severe transient conditions such as sudden load change. The STFT algorithm is evaluated analytically and subsequently applied to MATLAB/Simulink based DC test system. It is further validated and substantiated with the real fault current data obtained from a scaled-down experimental testbed. Sensitivity analysis and comparison with the existing frequency domain based fault detection method are done to support the efficacy of the proposed method.**

***Index Terms*—DC grid, Fault Analysis, Short-Time Fourier Transform (STFT), Transient Analysis, VSC.**

I. Introduction

With the rapid development of the voltage source converter (VSC) interfaced generation and load systems, DC grid is becoming a popular choice over AC grid. Some of the signifi

cant advantages of dc power system are lower conduction losses, the absence of reactive power component, easier integration of renewable energy & asynchronous generation sources, and economic operation. [1]. The ease of development of the DC power systems have been furthered with the advent of efficient power electronic converters [2], [3]. This can be seen by the increased research attempts toward multi-terminal high-voltage DC (HVDC) power transmission systems [4], DC microgrids at distribution level [5], DC shipboard [6], DC aircraft power systems [7] and so on.

However, compared to the AC counterpart, the wide-scale applicability of the DC power system is challenged by the lack of mature protection technologies [8], [9]. Robust fault detection algorithm using current and voltage signal inputs is the building block of any protection scheme. It must be able to reliably distinguish between the faults like short-circuit, and system transients such as sudden load change [8]–[10]. The DC fault current rises rapidly and has significantly different characteristics than the AC fault current. For this reason, the DC fault detection algorithm should be fast enough to identify the fault and send tripping signals to the DC circuit-breakers (CBs) or other interfaced fault isolating devices [11]. Failing to do so might damage the semiconductor devices of the interfaced converters [8].

A. Literature Review

DC fault detection and analysis are gaining increased research interests. Fault detection from the AC side is the simplest of all the detection algorithms [12], [13]. During the fault at DC side, the AC CB after detecting AC overcurrent would isolate the AC generation system. However, this scheme takes longer time to detect and isolate the fault, which makes it unsuitable for DC power system. Current derivative (di/dt & d^2i/dt^2) based fault detection have been successfully demonstrated for detecting the fast changing DC fault currents [14], [15]. The results are satisfactory, but is dependent on high bandwidth measurement devices. Moreover, the derivative method, when utilized in the time-domain, might not be immune to the noise present especially in the real DC current signals. Differential [16] and directional protection [17] algorithms are also presented, leveraging accurate current measurements and high fidelity communication links. Travelling wave-based fault detection technique [18] have also been devised. However, it requires high speed communication links, and is currently limited to the application in the long distance HVDC networks.

B. Motivation of the Study: Frequency-Domain Analysis

The trend in the existing fault detection algorithm has been toward time-domain analysis of the DC fault currents. The rapidly rising DC fault current is expected to have high frequency components which might be an effective indicator of the fault condition. There have been limited research attempts toward the study of frequency-domain analysis of DC fault conditions. The Wavelet Transform (WT) has been applied for analyzing non-periodic and non-stationary DC fault/transient current and voltage signals [19], [20]. With variable window size, it allows for simultaneous time and frequency-domain analysis of the transient signal. However, the frequency-domain analysis in the WT is illustrated by

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detailed coefficients which cannot provide precise frequency content information.

Unlike WT, Short-Time Fourier Transform (STFT) operates over a fixed window length which can provide precise frequency content information for a specified window size [21]. The frequency resolution improves with larger window size and vice versa. This property of the STFT makes it suitable for quantitative analysis of the frequency components in non-stationary signals like fault/transients. This has been previously utilized for the diagnostic applications of induction motors [22] & transformers [23] and for the power quality analysis in AC power systems [24]. For the application to the DC fault detection, the time resolution could be improved by the reduction of the hop size without affecting the frequency resolution. Thus, with the improved time resolution, STFT-based definitive quantitative analysis of frequency components for a particular window length could be a robust technique for the fault analysis in DC systems. The existing research attempts in the STFT-based DC fault analysis are primitive and offers limited theoretical analysis with focus on simulation-based fault current signals [25]. Hence, there is a need for in-depth theoretical analysis of the STFT method and validation with the experimental fault current signals which is the theme of the paper.

C. Organization of the Study

This paper aims to describe the step-by-step procedure for the STFT-based fault detection and establishing the transient analysis in the point-to-point DC system. The DC current signal is passed through predefined fixed size window function, and the discrete Fourier transform (DFT) is computed for quantitative investigation of the high-frequency components. To continuously analyze the DC current, the successive windows are overlapped with each other, determined by the hop size which is less than the window size while the DFT being successively computed. Being in the frequency-domain, it is immune to noise present in the current signal thus overcoming the challenges of the time-domain fault detection methods [14]. Moreover, most of the existing fault detection algorithms are tested primarily using simulation test cases, which might not work effectively with real fault signals. This paper also attempts to prove the feasibility of the STFT-based fault detection method by verifying it primarily on the experimental fault current signals along with the simulated ones. Verifying the applicability of the algorithm with the experimental fault current signals would help in substantiating the claim of its suitability in practical DC system.

The remainder of the paper is organized as follows. Section II describes the representative point-to-point DC system developed in MATLAB/Simulink environment as well as in the scaled-down experimental hardware testbed; vis-a-vis the simulation architecture. Section III covers the analytical derivations of the transient current signals in the DC networks, necessary to perform the STFT operation. Section IV describes the STFT-based fault detection algorithm, and the parameters influencing the operation of STFT. Section V presents the results of the various case-studies, sensitivity and comparative analysis from both simulation and experimental testbed. This is followed by conclusions in Section VI.

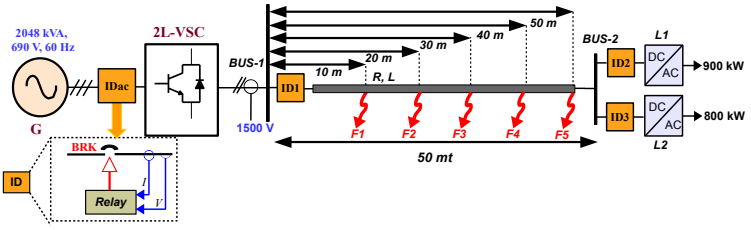


Figure 1. Simulation based DC test system for fault studies.

II. Test System For DC Fault Studies

A. Simulation Test System Description

Single line diagram of the simulation architecture of the point-to-point DC test system is shown in Figure 1. 'G' represents the generation source, chosen to be synchronous generator is interfaced with the two-level voltage-source converter (2L-VSC) at Bus-1. L_1 and L_2 are the loads connected to the Bus-2. The ratings of the various components of the simulation test system are shown in Figure 1. The line resistance and reactance are considered to be 0.128 Ω/km and 0.154 Ω/km [26]. '$F1 - F5$' represents the fault locations in DC line. The fault condition is detected and isolated by the intelligent device ('ID'). The ID comprises of the protective relay, giving tripping command to the fault isolating device represented by 'BRK'. The solid-state circuit-breaker (SSCB) type fault isolating device is considered which has operational time of around 400 μs [27].

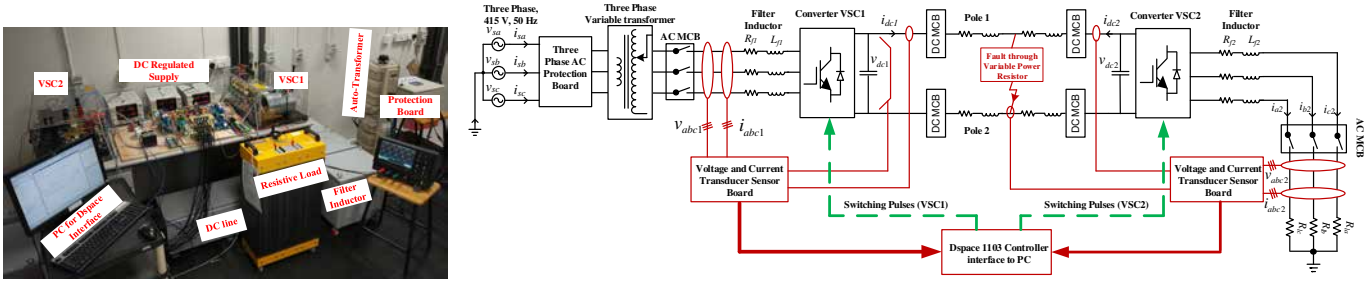
B. Experimental Test System Description

With reference to the simulation architecture, a scaled-down experimental testbed of approximate power ratio of 70:1 and bus voltage ratio of 12.5:1 is developed, as shown in Figure 2(a). The detailed schematic layout of the experimental testbed is shown in Figure 2(b), the parameters being listed in Table I. The testbed is developed with the primary intention of conducting fault studies. Initially, the STFT-based fault detection algorithm is developed and tested on the signals from the simulation test system. Subsequently, the algorithm is validated with actual fault current obtained from the hardware test setup.

TABLE I
Experiment Setup Parameters

Parameters	Values
Supply voltage	3ϕ, 85 V_{rms}, 50 Hz
3ϕ AC Protection Board	40 A, B Type, TP MCB with Shunt trip
3ϕ Variable Transformer	30 kVA, (0-415) V
Converters (VSC1, VSC2)	two-level 30 kVA, 400 V
DC Capacitor	C_{dc} = 2350 μF
DC Bus Voltage	V_{dc} = 120 V
DC Line Paramters	L_d = 1.5 mH, R_d = 0.03 Ω
DC MCB	C60H-DC, C 4 A
Interface Filter Parameters	R_f = 0.1 Ω, L_f = 10 mH
Linear Load	R_l = 20 Ω
Variable Power Resistor	5000 W, (1-16) Ω
DC Solid State Relay	D2D40, 200 V, 40 A

As shown in the experimental schematic, VSC-1 acts as AC-DC converter, maintaining the DC bus voltage at 120 V. For this operation, 3-ϕ, 30 kVA, (0-415 V) variable transformer is utilized to maintain the input AC voltage of VSC-1 at 85 V (line-line rms). VSC-2 acts as DC-AC converter, supplying power to the 3-ϕ AC load. The voltage and current quantities at power level are converted to signal level using the hall effect voltage ($\pm$ 500 V to $\pm$ 15 V) and current ($\pm$ 10 A to $\pm$ 4 V) transducers. These signals are fed to the dSPACE-1103 controller through the analog to digital channels ports. The control algorithm is developed in MATLAB/Simulink, and converted



(a) (b)

Figure 2. (a) Experimental hardware testbed and (b) schematic of the hardware testbed of the DC power system.

for the dSPACE hardware, interfaced by means of Real Time Interface (RTI) toolbox. The pulse-width modulation (PWM) signal generated by dSPACE-1103 controller are fed to the gate driving circuit of the VSC-1 and VSC-2.

Bolted short-circuit across the DC line of the experimental setup is not advisable in the laboratory premises due to safety regulations and additional protection requirements. This might result in tripping of the circuit-breaker of the main incoming feeder of the laboratory. Thus, high impedance short-circuit studies are conducted using a power resistor, which helps to limit the magnitude of the fault current and dissipate the energy of the fault current. The power resistor is controlled by a DC solid-state relay which is activated once the system has reached steady-state. The value of the resistance is adjustable from 1 Ω to 16 Ω to get varying levels of fault currents. STFT based fault detection is validated with the experimental fault current obtained from the high impedance fault resistance of 2 Ω. Sensitivity analysis is conducted by varying the fault resistance provided by the power resistor from 2 Ω–14 Ω while all the experiments being conducted independent of each other.

III. Transients in DC Networks

The short circuit fault and sudden change in the load demand are the most common transients associated with the DC power systems.

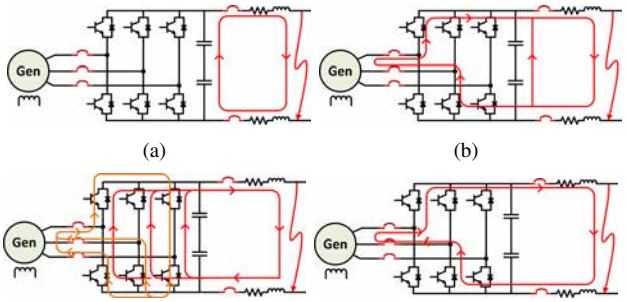
1) Faults in DC Networks: Pole-pole short-circuit is the most severe kind of fault in the DC power system which happens when the positive and negative poles get short-circuited via the fault resistance [8]–[10]. The short-circuit current response of the pole-pole fault is typically a 4-stage process (see Figure 3), which is described with reference to the generation system of Figure 1.

Stage 1: Before the fault inception, the DC-link voltage exceeds the line-to-line voltage of the AC source. As a result, the DC-link discharges almost instantaneously during the fault, reducing the DC-link capacitor voltage.

Stage 2: As the DC-link voltage reduces below the line-to-line voltage of the AC source, the generator starts contributing toward the fault current. At this point of time, the freewheeling diodes are no longer reverse biased, and they start conducting alternatively. The IGBTs may be blocked owing to the overcurrent protection.

Stage 3: The freewheeling diodes start conducting after the IGBTs are suitably blocked. The DC-link capacitor attempts to charge in the reverse direction, but get shorted by the freewheeling diodes. As all the diodes are conducting, the AC source essentially gets short-circuited.

Stage 4: The fault current is sustained by the AC source, with the diode bridge in operation. The load in this case is the DC-link capacitor in parallel with the stray inductance, equivalent resistance of the system and fault resistance.



(a) (b) (c) (d)

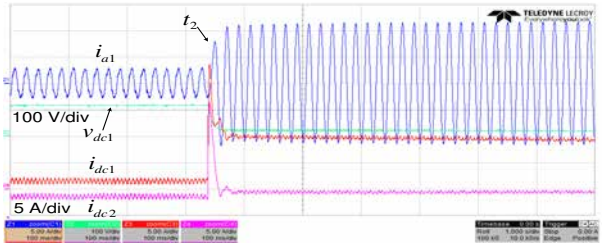
Figure 3. Different stages of the DC fault current, (a) Stage 1, (b) Stage 2, (c) Stage 3 and (d) Stage 4.

2) Sudden Load Change: The loads in DC system are mostly interfaced through the power electronic converters which are dominantly the constant power loads (CPLs). During sudden load change, current rise depends on the nature of the interfaced loads and the control bandwidth of the interfaced converters and is discussed in detail in Section V-G. For the HVDC system, this might result from sudden grid load requirements [4], or change in input power due to intermittent renewable sources. In DC marine/aircrafts, sudden load change might be encountered by abrupt propulsion load demands [6], [7], etc. In this paper, this transient condition is emulated by sudden increase in the AC loads resembling scenario of a typical DC microgrid.

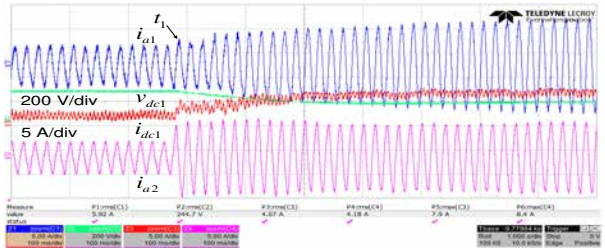
The experimental results for the DC fault and the load change are shown in Figure 4. The annotations of Figure 4 is consistent with Figure 2(b).

A. DC Fault Current Calculations

As described, a typical DC fault current behaviour is characterized by transient discharge from the DC-link capacitors, and steady-state current discharge from the generation source. In case of the synchronous generator interfaced with the 2L-VSC, the fault currents can be divided into DC-link capacitor current discharge, generator sub-transient, transient and steady-state fault current discharge, as shown in Figure 5(a). If there is no fault limiting inductor between the generator and the VSC for the case shown in Figure 1, the fault current contribution from the generator side is capable of damaging the free-wheeling diodes once the thermal capability (I^2t) rating is exceeded [28]. Fig. 5(b) shows the I^2t of the freewheeling diodes during low impedance fault (0.01 Ω) and for ratings consistent with the generation system of Fig. 1. The I^2t rises rapidly during the fault and is dependent on the fault resistance and location. Although the thermal capability for this scenario is reached at around 20 ms, this time is significantly reduced

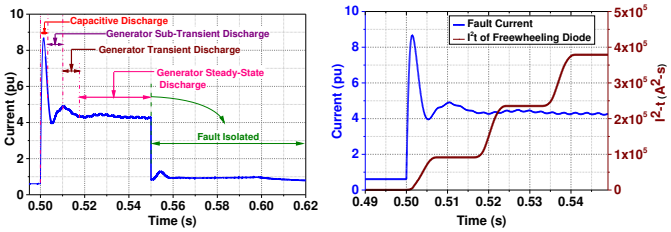


(a)



(b)

Figure 4. (a) Fault current characteristic and (b) sudden load change in the experimental testbed.



(a) (b)

Figure 5. (a) DC fault current contributing sources and (b) change in I^2t of the freewheeling diodes by the AC side fault current contribution. (Base current = 1300 A)

for the worst case scenario i.e. bolted faulted condition. Hence in this paper, the available time for fault detection and isolation is restricted to $\leq$ 5ms.

The DC-link capacitor discharge is the prime indication of faults in the DC networks. The capacitive discharge current during the fault is calculated with the help of transient discharge circuit as shown in Figure 6. This will help in understanding the nature and factors affecting the DC-fault current which is required to devise the necessary detection algorithms. For the pole-pole fault in Figure 6, the fault current is given by:

$$I(s) = \frac{\frac{V(0+)}{L} + sLI(0+)}{s^2 + s\frac{2R+R_f}{2L} + \frac{1}{LC}}. \tag{1}$$

The DC-link capacitor of the 2L-VSC is denoted by 'C', the line resistance and inductance are indicated by 'R' and 'L', 'R_f' is the fault resistance, 'R_G' is the ground resistance, '$V(0+)$' and '$I(0+)$' are the initial voltages and currents through the DC-link capacitor and the line inductor.

The fault current has underdamped (u.d.) nature for $\alpha < \frac{1}{LC}$, and overdamped (o.d.) nature for $\alpha > \frac{1}{LC}$ where

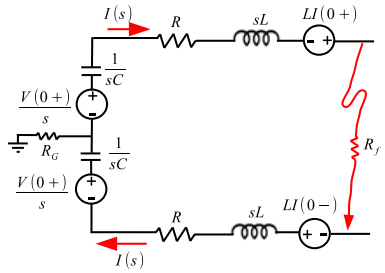


Figure 6. Transient discharge circuit depicting capacitive discharge current for pole-pole fault.

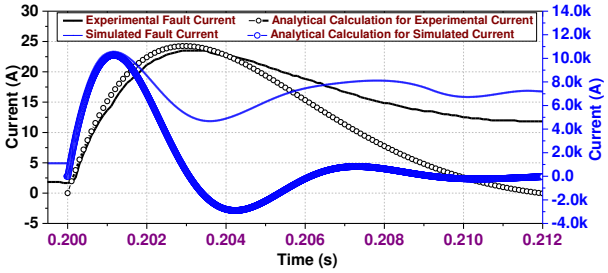


Figure 7. Comparing the analytical DC-link discharge current with simulated and experimental fault current.

$$\alpha = -\frac{2R+R_f}{4L} = -\frac{\sum R_{fault}}{2\sum L_{fault}}, \tag{2a}$$

$$\beta = \sqrt{\left(\frac{2R+R_f}{4L}\right)^2 - \frac{1}{LC}} = \sqrt{\alpha^2 - \frac{1}{\sum L_{fault}\sum C_{fault}}}, \tag{2b}$$

$$\omega_d = \sqrt{\frac{1}{LC} - \left(\frac{2R+R_f}{4L}\right)^2} = \sqrt{\frac{1}{\sum L_{fault}\sum C_{fault}} - \alpha^2} \tag{2c}$$

$\sum R_{fault}$, $\sum L_{fault}$ and $\sum C_{fault}$ are the loop resistance, inductance and capacitance from the generation source to the fault location. The time-domain expression for the fault currents during the over-damped (*o.d.*) and the under-damped (*u.d.*) conditions are given by Eq. (3, 4).

$$i_{o.d.}(t) = \left(\frac{V(0+)}{2L\beta} + \frac{LI(0+)}{2}\right)e^{-(\alpha-\beta)t} + \left(\frac{-V(0+)}{2L\beta} + \frac{LI(0+)}{2}\right)e^{-(\alpha+\beta)t}, \tag{3}$$

$$i_{u.d.}(t) = \frac{V(0+)}{\omega_d L}e^{-\alpha t}sin(\omega_d t) + LI(0+)e^{-\alpha t}cos(\omega_d t). \tag{4}$$

The developed analytical fault current expressions are compared with simulation and experimental fault current signals (see Figure 7). The simulation and experimental fault current signals (i_{dc1} of Figure 4(a)) follow the analytical expressions till the DC-link capacitor discharge contributes significantly to the fault current. Subsequently, the fault current supplied by the AC source becomes dominant, which can be seen by significant deviation between the analytical and the simulation/experimental results.

Nevertheless, the initial fault current due to DC-link discharge is a prime indicator, which will be used in upcoming sections for STFT-based fault detection.

IV. STFT Based Fault Detection Algorithm

A. STFT Definition

The STFT computes the Fourier transform (FT) of a function $f(t)$ over a real and symmetric window function $w(t)$,

which is translated by time 'u' and modulated at frequency 'ω'. The expression of STFT in continuous domain is illustrated by Eq. (5)

$$S_C(u,\omega) = \int_{-\infty}^{+\infty} f(t)w(t-u)e^{-j\omega t}dt. \quad (5)$$

In the real world, the signals are sampled with fixed sampling frequency (f_s), and discrete Fourier transform (DFT) is computed to analyze the frequency spectrum by applying Fast Fourier transform (FFT) algorithm. Thus, the Eq. (5), in discrete domain reduces to Eq. (6).

$$S_D[m,k] = \sum_{n=0}^{n=N-1} x[n]w[n-mH]e^{-j\frac{2\pi nk}{N}}, \quad (6)$$

where N is the number of FFT points, n is the time-domain index of the input sample, $x[n]$ is the input sample, $w[n]$ is the window function, m is the position of the $w[n]$ around which it is real and symmetric, H is the hop size between the successive windows and k is the frequency index. n is generally governed by the length of the $w[n]$. On the contrary to the traditional DFT, time resolution in STFT is dependent on 'H' rather than 'n' and is illustrated by H/f_s (in s) [21].

B. STFT Dependence Parameters

1) Sampling Frequency (f_s): It directly affects the time and frequency resolution of the STFT output. Higher f_s results in improved time and frequency resolution and vice versa. In this paper f_s of the STFT based algorithm is limited to 10 kHz which is consistent with the sampling frequency of the hardware testbed, and is typically used for practical relaying applications.

2) Number of Input Sample (n): It is the non-zero input samples of the input current/voltage on which the windowing function is applied. Increase in n would increase the window size, hence improving the spectral resolution among the present signals of different frequencies.

3) Total number of FFT points (N): Increase of N helps in improving the frequency resolution of the STFT output. Besides, it helps in better approximation of the continuous Fourier transform (CFT) of the input signal. Zero padding of the input signal is done if number of input samples (n) $<$ number of FFT points (N). However, the computation time increases with increase in 'N'.

4) Type of Window Function ($w[n]$): Rectangular, Triangular, Hanning, Hamming and Bartlett are some of the popular window functions available to perform STFT. In this paper, Hanning window function is used for the transient state detection. Further, the comparative analysis with other popular window functions is described in Section V-E.

5) Hop Size (H): It is responsible for the time resolution of the STFT output. Lower is the hop size, better the time resolution becomes. In this paper, H is chosen to be 2 samples which is equivalent to the time resolution of 0.2 ms.

C. STFT Operation on DC Fault Current

The operation of the STFT based fault detection scheme on experimental fault current is shown in Figure 8. $w[n]$ is applied to the input current signal and DFT is correspondingly computed. After the computation, the window function advances by 'H' and DFT is computed again. This process is repeatedly followed and is shown in Figure 8. The windows are denoted by number 1,2,3...12 which are applied to the input current signal and DFT1, DFT2, DFT3...DFT12 are the output discrete fourier transform for each windowing instants.

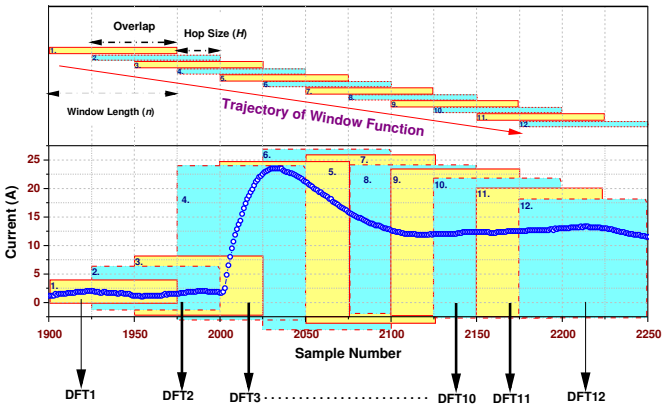


Figure 8. STFT operation on DC fault current obtained from the experimental testbed.

D. Fault Detection by STFT: Analytical Evaluation

The STFT algorithm is applied on the analytical approximation of the experimental DC pre-fault and fault current. The pre-fault current (i_n) is the initial DC current ($I(0+)$) flowing in the testbed. The DC fault current is approximated by the Eq. (1-4), and is shown in Figure 7. The STFT of the pre-fault DC current having finite window length would resemble DFT operation of the rectangular pulse as shown in Eq. (7). The width of the rectangular pulse is determined by the length of the window function.

$$\begin{aligned} |I_n(\omega)| &= \left| \int_{-\tau/2}^{+\tau/2} i_n.e^{-j\omega t}dt \right| \\ &= I_n.\tau.\left| \frac{sin(\omega\tau/2)}{\omega\tau/2} \right|. \end{aligned} \quad (7)$$

The FT of the pre-fault current is a *sinc* function (Eq. (7)) which would comprise of main-lobes and side-lobes decaying with roll-off rate depending on the choice of window functions as shown in Figure 9 (blue color). Since the STFT operation has fixed window size; the frequency resolution, location of the frequency bins and update-frequencies are expected be fixed irrespective of the input current signal. The update-frequencies of the *sinc* function are the frequency bins where the frequency response i.e. the magnitude approaches zero [21]. As per Eq. (7), the values of update-frequencies for continuous and discrete domain are shown in Figure 9. In case of fault, the STFT of the fault current takes the form of Eq. (8) or (9), (derived from Eq. (3) or (4)) depending on the nature of the fault current. The $LI(0+)$ term is neglected for its significantly lower values.

$$|I_{o.d.}(\omega)| = \left| \int_0^{\tau} i_{o.d.}(t).e^{-j\omega t} dt \right| = \frac{V(0+)}{2L\beta} \left[\frac{1 - e^{-(\alpha-\beta)\tau}}{\sqrt{(\alpha-\beta)^2 + \omega^2}} - \frac{1 - e^{-(\alpha+\beta)\tau}}{\sqrt{(\alpha+\beta)^2 + \omega^2}} \right]. \quad (8)$$

$$|I_{u.d.}(\omega)| = \left| \int_0^{\tau} i_{u.d.}(t).e^{-j\omega t} dt \right| = \frac{V(0+)}{2\omega_d L} \left[\frac{1 - e^{-\alpha\tau}}{\sqrt{(\omega_d - \omega)^2 + \alpha^2}} + \frac{1 - e^{-\alpha\tau}}{\sqrt{(\omega_d + \omega)^2 + \alpha^2}} \right]. \quad (9)$$

Considering the window number 4 of Figure 8 where DFT is computed on both pre-fault DC and faulted DC current, the STFT magnitude response would be summation of Eq. (7) and Eq. (9), ($u.d.$ nature of experimental fault current). The resultant STFT response of the fault current is characterized by higher non-zero magnitude at the corresponding update-frequencies. The presence of non-zero magnitude at update-frequencies would be suitable indicator of the transient condition. Moreover, the increased magnitude for higher frequency bins indicates the ingression of the high frequency components during fault conditions. It is to be noted that the rectangular window is used to simplify the analytical calculations in Eq. (7,8,9), and to get the essence of STFT algorithm. Hanning window is used for STFT analysis of experimental and simulated DC current which is described in the next section.

V. Results and Discussions

It can be inferred that the transient state in the DC system is characterized by ingression of high-frequency components and non-zero magnitude at update-frequency bins. For the Hanning window function used for simulation and experimental studies, the update-frequency bins would occur at $2.f_s/n$, $3.f_s/n$, $4.f_s/n$... and so on [21], as shown in Table II.

TABLE II
Update-Frequency Bins for Various Hanning Window Lengths

Window Length [n]	$2f_s/n$	$3f_s/n$	$4f_s/n$
16	1250 Hz	1875 Hz	2500 Hz
32	625 Hz	937.5 Hz	1250 Hz
64	312.5 Hz	468.75 Hz	625 Hz
128	156.25 Hz	234.375 Hz	312.5 Hz
256	78.125 Hz	117.1875 Hz	156.25 Hz
512	39.0625 Hz	58.59375 Hz	78.125 Hz

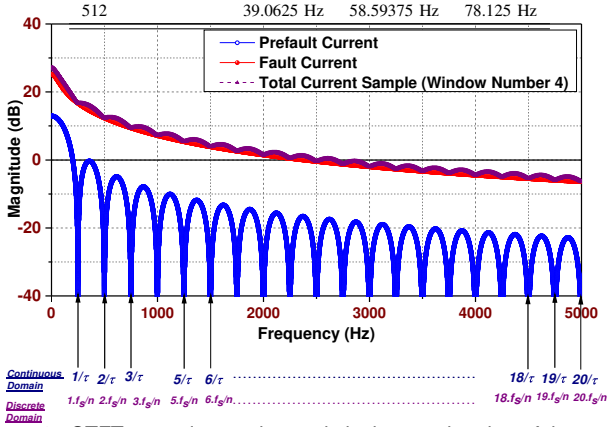


Figure 9. STFT operation on the analytical approximation of the experimental DC fault current.

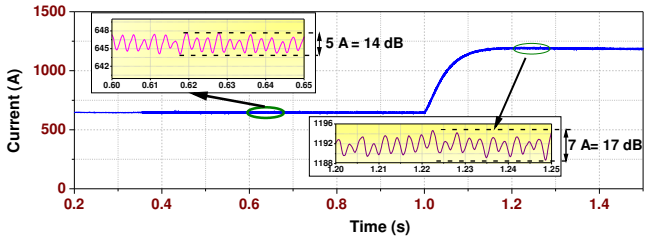


Figure 10. Simulated DC current with load change at 1 s.

A. Selection of Window Length

For the pre-fault DC signal with negligible ripple component such as analytical expressions in Section IV-D, the magnitude at the update-frequencies are significantly negative (in dBs), as shown in Figure 9 (blue color). However, in the DC grid system formed by interfacing 2L-VSC, the DC current would have ripples, affecting the frequency-domain response. The ripples in the pre-fault current might increase the magnitude at the update-frequency bins, causing a false identification of the transient condition. Thus, the window length must be chosen for which the update-frequency bins do not lie within the vicinity of ripple frequencies of the pre-fault DC current.

1) Simulation Test System: The ripple frequency of the DC pre-fault current is six times the AC side frequency (360 Hz; AC side frequency = 60 Hz). This is primarily caused by the conduction pattern of the semiconductor switches of the 3-ϕ 2L-VSC. To illustrate this, the load was changed at 1 s and ripple current components were observed in the simulation test system (see Figure 10). The ripple current of 5 A is present before the load change, and 7 A after the load change. In the time-domain, the magnitude of the ripple component is significantly less as compared to the line current. However, in frequency-domain, the ripple content would result in 14 dB (for 5A ripple content) and 17 dB (for 7 A ripple content) change in the magnitude. This would result in shifting of the frequency response magnitude toward more positive region. Thus on the contrary of highly negative magnitude at the zero frequency bins for ideal DC current, the actual magnitude would move toward more positive side.

The frequency response of the simulated DC signal for various window lengths and corresponding update-frequency bins consistent with Table II are shown in Figure 11. The window lengths must be chosen carefully considering the 360 Hz ripple component. Priority of the selection of the 'n' should be given to the update-frequency bins which do not lie within the range of 360 Hz. By comparing Table II and Figure 11, the window length of 16, 32, 256 and 512 samples might be chosen. By choosing $w[n]$ of 64 samples, the magnitude at first update-frequency bin has positive magnitude, which is caused by the presence 360 Hz ripple component. This is confirmed by performing STFT with increased window lengths (128, 256, 512), where the magnitude at the vicinity of $\approx$ 360 Hz has higher magnitudes. This is also indicated in Figure 11.

2) Experimental Test System: The pre-fault current obtained from the experimental testbed is shown in Figure 12. The experimental test setup has higher line inductance intended to restrict the rate of rise of fault current. The experimental setup has significant third harmonic component, originating from other power electronics-based test setups connected to the same laboratory supply. Hence in this sce-

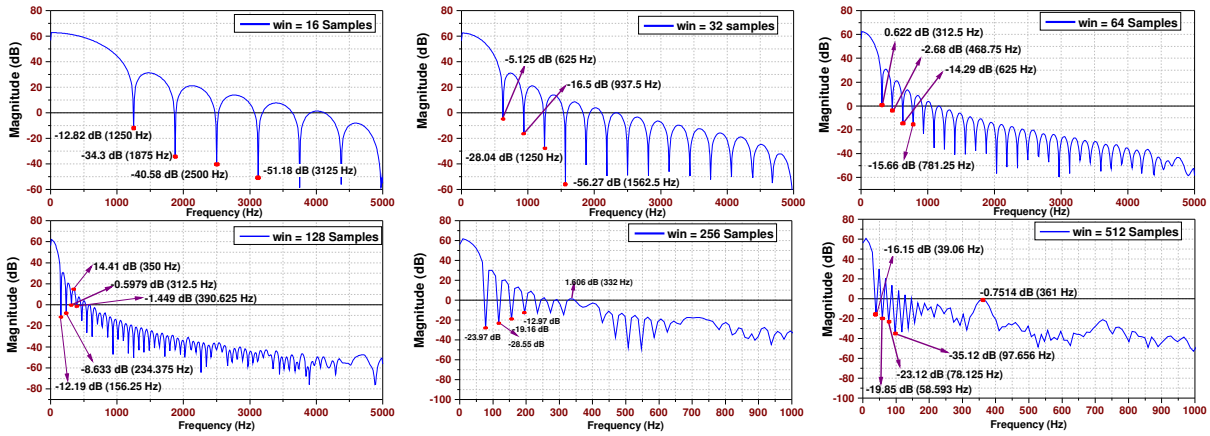


Figure 11. Frequency spectrum of simulated pre-fault current for various window lengths.

nario, the window lengths must be chosen considering the 150 Hz third harmonic component (laboratory setup has 50 Hz AC signal). From the Table II, window lengths of 128 and 256 samples should be avoided as that would result in high magnitude at update-frequency bins (due to 150 Hz component) as shown in Figure 13. The presence of the 150 Hz component can be seen from the increased magnitude at the vicinity of ≈150 Hz frequency for window lengths of 128, 256 and 512 samples in Figure 13.

Thus the reliable operation of the STFT algorithm depends on the selected window size which is different for simulation and experimental test system. This difference is due to dissimilar ripple content of DC current in both cases.

B. Operation During Faults

Following the aforesaid discussions, we choose the window length for the simulated test system to be between 16 and 32 samples. For the experimental test system, the window length is to be chosen among 16, 32 and 64 samples.

1) Simulation Fault Current: The frequency response for simulated fault current for 16 and 32 samples window length is shown in Figure 14. The low impedance fault resistance of 0.01 Ω at $F1$ (Figure 1) is used for simulation test setup.

1. *16 Sample:* The frequency response of the pre-fault current has negative magnitude at desired update-frequency bins. At 0.2 ms after the fault inception, the frequency spectrum starts distorting, however still remaining comparable with the pre-fault frequency spectrum. At 0.4 ms after the fault inception, superposition of high-frequency components is evident from the non-zero magnitude at the update-frequency bins. As the fault persists for 0.6 ms to 1.0 ms, the equiripple sidelobes gets distorted due to the high-frequency components to form an exponential type structure, as per Section IV-D.
2. *32 Sample:* The frequency response of the pre-fault current has non-zero magnitude at the first update-frequency, which is due to the frequency of the ripple currents. At 0.2 ms after the fault inception, the sidelobes are still in equiripple condition, being comparable with the pre-fault current frequency response. From 0.4 ms onwards after fault inception, the sidelobes start distorting as seen from the Figure 14.

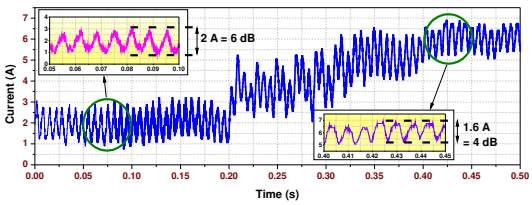


Figure 12. Experimental DC current with load change at 0.2 s.

2) Experimental Fault Current: The frequency response for experimental fault current (i_{dc1} of Figure 4(a)) for 16, 32 and 64 samples window length is shown in Figure 15.

1. *16 Sample:* The frequency spectrum starts distorting 0.8 ms after the fault inception, which can be observed by non-zero magnitude at first update-frequency bin (1250 Hz) and increased high-frequency components, compared to the pre-fault conditions.
2. *32 Sample:* Significant distortion of the sidelobes with 32 sample window length is visible at 1 ms, seen by the non-zero magnitude at first update-frequency and increased ingression of high-frequency components.
3. *64 Sample:* Fault detection with 64 sample window function is much slower than the 16 and 32 sampled window functions. Significant distortion in frequency response is visible after 1.4 ms.

It can be inferred that the time delay for fault detection is dependent on the length of window functions especially, for the high impedance fault in the experimental test setup. For low impedance fault in simulation test setup, the fault detection time is almost same for all the window sizes.

C. Pseudo Code

The prime-identification for the fault condition is the non-zero magnitude at the update-frequency bins for the given window size. Due to the presence of ripples in the output DC current, the magnitude at the first update-frequency could be positive. Hence, relying on the magnitude of the first update-frequency bin would not be a robust solution. Instead, the fact that magnitudes of first few update-frequencies increases beyond a certain set-point, may be used for fault detection algorithm. From the results, the set-point for simulation system and experimental setup can be set at 20 dB and -10 dB respectively, since the simulation based system has higher installed capacity than the experimental setup. Algorithm 1 depicts a generic pseudo-code for STFT based fault detection. The algorithm uses FFT with slight modification for fault detection which could be easily implemented in embedded hardware system proving its practicability in real system.

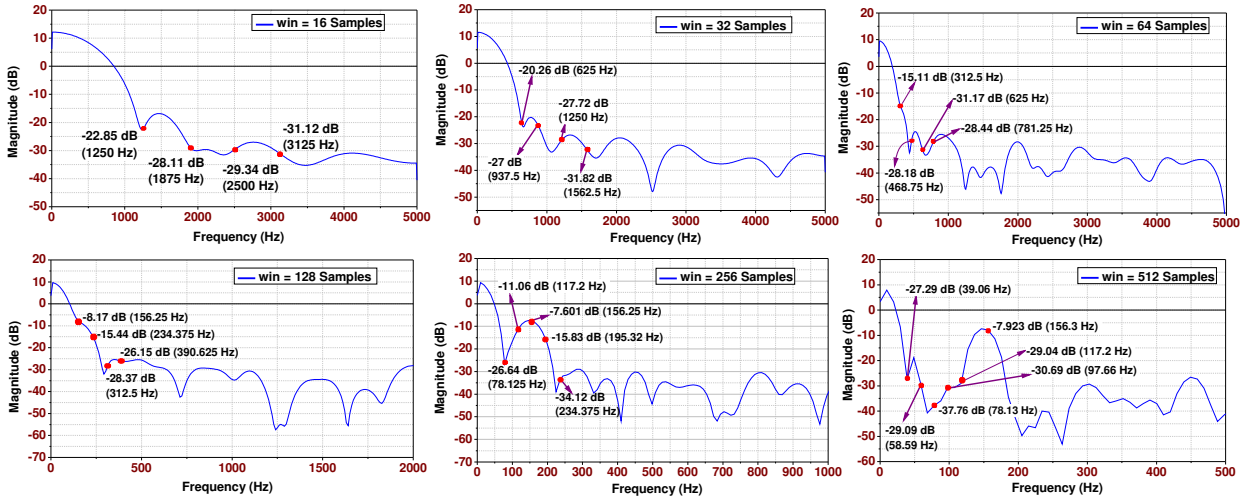
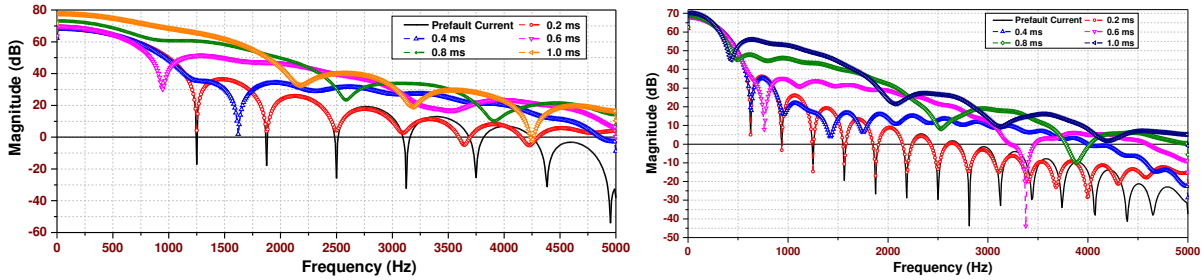
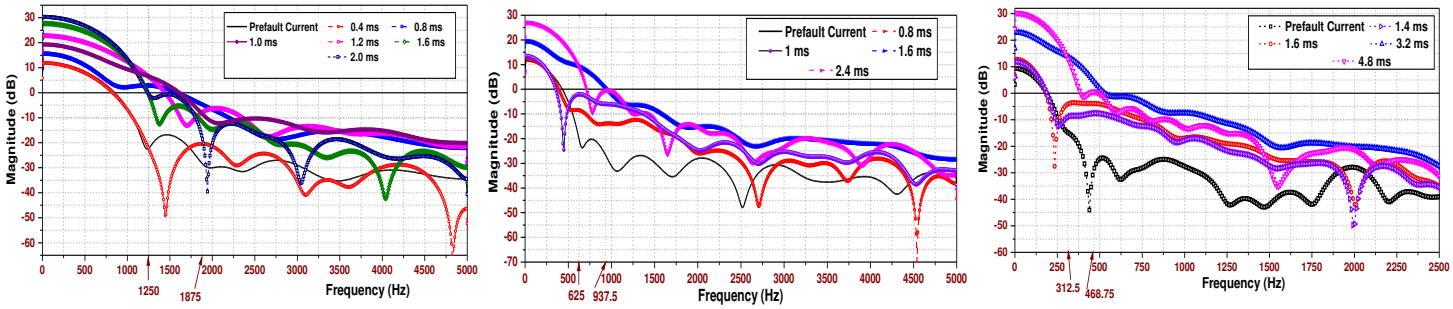


Figure 13. Frequency spectrum of experimental pre-fault current for various window lengths.



(a) (b)

Figure 14. Frequency response of simulated fault current for window lengths (a) 16 and (b) 32 samples.



(a) (b) (c)

Figure 15. Frequency response of experimental fault current for window lengths (a) 16, (b) 32 and (c) 64 samples.

D. Sensitivity Analysis

The STFT algorithm is able to detect the fault current of varying magnitudes and rate of rise in both experimental and simulation test system. To illustrate this, fault resistances of different values have been applied at fixed location in the experimental test setup. The corresponding DC fault currents are depicted in Figure 16. Table III shows the fault detection time when the STFT algorithm is applied with 32 sample and 64 sample window lengths. For the simulation test system, the fault current magnitude and rate of change is further varied by applying fault resistances at different locations (*F1-F5* in Figure 1). The fault detection time for 32 sample window is shown in Table IV. From Table III, IV it can be inferred that the STFT algorithm is fast and is able to detect the low impedance fault in 1 ms and high impedance fault in 2 ms thus suitable for DC protection. Furthermore, the detection timing is dependent on the window size (Table IV) and should be selected as per Section V-A. Lower window size is very sensitive and detects fault in less time, whereas bigger window size makes the algorithm sluggish, taking longer time.

E. Comparison with Other Window Functions

Apart from the Hanning window function, the fault and load change currents obtained from the experimental test set-up is compared with other popular window functions. The magnitude of the first update frequency of the various window functions are compared in Figure 17. It can be concluded that rectangular window function is most sensitive to both

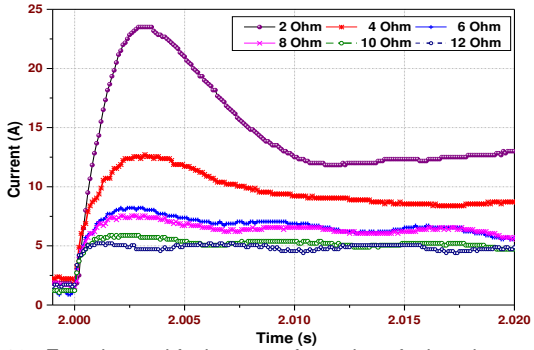


Figure 16. Experimental fault current for various fault resistances.

Algorithm 1 Pseudo-code of STFT Based DC Fault Detection

– Read input current signals (x_{cur}) and sample at sampling frequency of f_s.
– Define operating parameters of STFT such as window size (n), window type (w[n]), number of FFT points (N), hopping size (H). ▷ Section IV-B.
–Frequency resolution: f_s/N; Time resolution: H/f_s
–Define tripping set-point X_{trip}.
while ((H + n) < total input samples of x_{sig}) **do**
  – x = x_{cur}[1:n].*w[n] ▷ Windowing the signal.
  – X = FFT(x,N) ▷ FFT on windowed signal.
  – Store X.
  – Calculate Magnitude ($|X|$ dB.)
  for f=1:fs/N:fs/2 **do**
    Plot f vs |X|
    if |X|> X_{trip} dB at m.fs/n **then**
    ▷ first three update-frequencies i.e. m=2 & 3 & 4 for improved reliability.
      –Fault in the System
      –Trip the CB/Fault Isolating Device.
    else
      –No Fault in the System.
      –Go Back to Step 10.
    end if
  end for
  – x = x_{cur}[1+H:n+H]
  – Go to Step 5.
end while
Print Results.

TABLE III
ABSOLUTE VALUE OF FAULT DETECTION TIME FOR DIFFERENT FAULT RESISTANCES AND WINDOW LENGTHS IN THE EXPERIMENTAL SETUP

Fault Resistance (Ω)	*win = 32*	*win = 64*
2	1.0 ms	1.4 ms
4	1.4 ms	1.6 ms
6	1.4 ms	1.8 ms
8	1.4 ms	2.0 ms
10	1.4 ms	2.2 ms
12	1.4 ms	2.2 ms

TABLE IV
ABSOLUTE VALUE OF FAULT DETECTION TIME FOR DIFFERENT FAULT RESISTANCES AT VARIOUS LOCATIONS IN THE SIMULATION SETUP

Fault Resistance (Ω)	*10m*	*20m*	*30m*	*40m*	*50m*
0.01	0.4 ms	0.4 ms	0.4 ms	0.4 ms	0.4 ms
0.1	0.4 ms	0.4 ms	0.4 ms	0.4 ms	0.4 ms
0.5	0.4 ms	0.4 ms	0.4 ms	0.4 ms	0.4 ms
1	0.4 ms	0.4 ms	0.4 ms	0.6 ms	0.6 ms
2	0.4 ms	0.4 ms	0.4 ms	0.6 ms	0.6 ms
5	0.4 ms	0.6 ms	0.6 ms	0.6 ms	0.8 ms

load change and fault conditions. It could falsely identify load change as fault condition thus spuriously tripping the system. The triangular window is the least sensitive to faults and load change which might delay the fault detection timing. The Hanning window would be the ideal choice as the sensitivity is neither too high nor too low thus providing reliable results for both load change and fault condition.

F. Comparison with Wavelet Transform

To prove the efficacy, the performance of STFT based fault detection method is compared with the popular wavelet transform (WT) based fault detection which is also frequency-

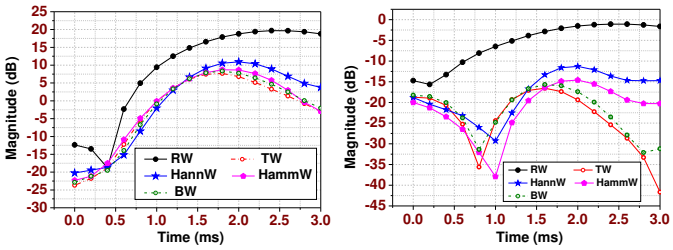


Figure 17. Variation of first update frequency with (a) fault current and (b) load change in the experimental test set-up. [RW: Rectangular Window, TW: Triangular Window, HannW: Hanning Window, HammW: Hamming Window, BW: Bartlett Window]

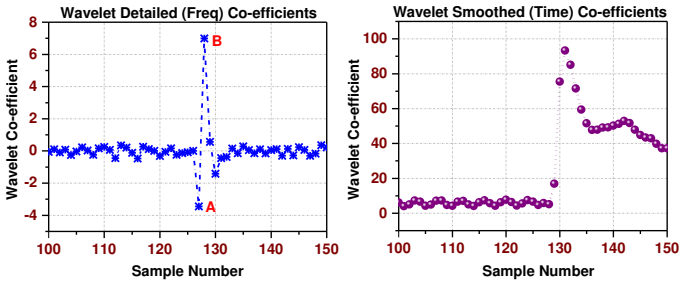


Figure 18. Wavelet transform of the fault current signal obtained from experimental test setup.

TABLE V
STFT V/S WAVELET BASED FAULT DETECTION ALGORITHM

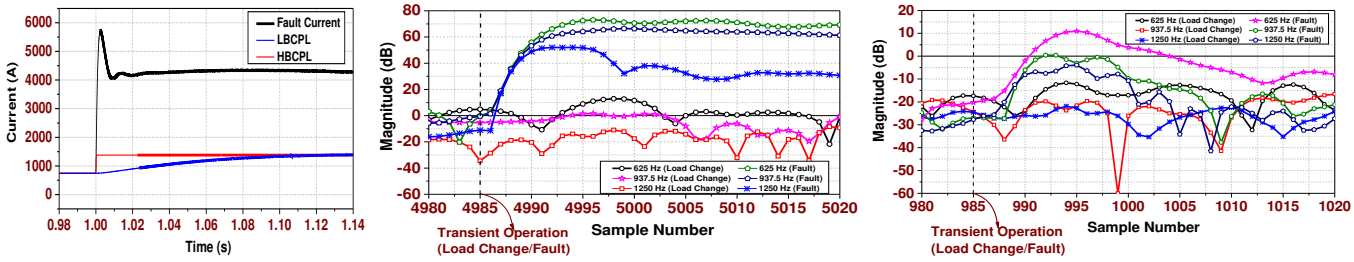
Method	*Fault Detection Time (ms)*	*Computation Speed* x 10^{-5} *(s)* (*)
Wavelet	1.93	4.1253
$STFT_{win=32}$	1.0	2.447

(*): *intel core i5*® based computation system

domain analysis of DC fault current. The comparison has been done for the fault current obtained from experimental test setup (Figure 8). WT of the fault current is computed using db3 at 4^{th} level of decomposition [19]–[21] as shown in Figure 18. The fault signal is reinterpreted in frequency (detailed co-efficient) and time (smoothed co-efficient) domain. The highest detailed co-efficient indicates the presence of high frequency components introduced by the fault transients. Therefore, at 4^{th} level of decomposition, the fault is detected at 128^{th} sample (point B in Figure 18), with detection time of 1.933 ms. The WT detects the fault condition with the abrupt change of detailed frequency co-efficients, whereas the STFT allows for quantitative analysis of the frequency information with precise dB level. Thus, the STFT is more definitive method than the WT, both being frequency-domain methods. With respect to the Section V-C, the performance of STFT is compared with the WT based fault detection and is summarized in Table V. As compared to WT, STFT is computationally efficient and takes less time to detect the fault.

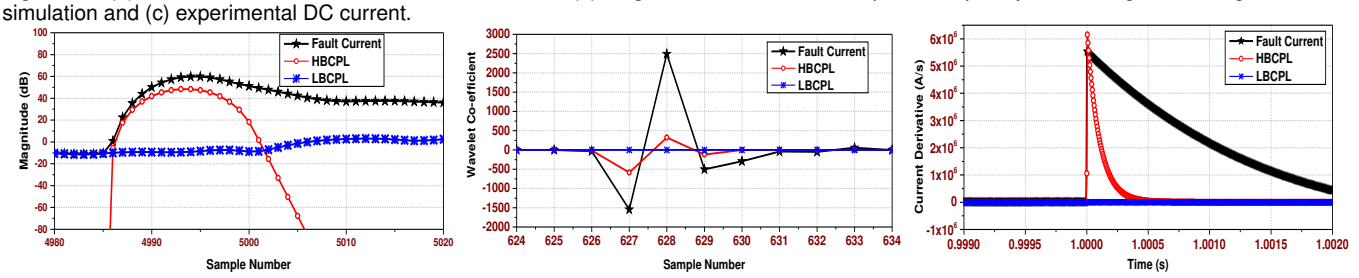
G. Load Change Operation

The rise time of the load current in DC system is dependent on the bandwidth of the current controller and the nature of the interfaced load. For the dominant inductive loads such as motor drives, AC loads, grid side load demands etc., the rise time of the current due to sudden load demand is more than the rise time of the fault current. These loads are termed as 'Low Bandwidth CPLs' (LBCPLs) and is shown in Figure 19(a). For such cases, the magnitude of the first three update-frequency bins for simulation and experimental load change current is



(a) (b) (c)

Figure 19. (a) Variation of fault current, LBCPL and HBCPL, (b) Magnitude of the first three update-frequency bins during load change and fault for simulation and (c) experimental DC current.



(a) (b) (c)

Figure 20. Comparative analysis of the response when (a) STFT, (b) WT and (c) di/dt is applied to the fault current and sudden change of load for LBCPL & HBCPL.

shown in Figure 19(b, c), and is compared with that of fault conditions for better illustration. It can be noticed that the magnitude does not change much during the load change in LBCPLs, helping to discriminate against the fault events.

However, with the emerging power electronic loads having high bandwidth of the current control loop, the rise time of the current due to sudden load change might be comparable with the rise time of the fault current. These loads are termed as 'High Bandwidth CPLs'(HBCPLs) and is shown in Figure 19(a). Figure 20(a) shows the variation of the magnitude of the first update-frequency bin for fault current, sudden change of HBCPL & LBCPL. Compared to LBCPLs, the discrimination between HBCPL and fault condition is difficult, but is still possible in the frequency domain by setting suitable threshold limits. This is further examined by the application of WT (Section V-F) and time-domain based di/dt method [15], both indicating presence of fault during sudden change of load for HBCPL as shown in Figure 20(b, c). In such cases, the fault detection could be complemented with additional conditions such as bus undervoltage. However, the majority of the interfaced loads are expected to be of LBCPL type; the STFT-based fault detection could be used satisfactorily to discriminate against fault conditions.

VI. Conclusion

In this paper, Short-Time Fourier Transform (STFT) based analysis has been established for robust fault detection and transient analysis in VSC based DC system. The main idea is to quantitatively utilize the superposition of the high-frequency components during the transient period.

- This fault detection algorithm has been validated and substantiated by applying it to simulation and experimental test system. Being a frequency-domain analysis, it is immune to the noise present in the fault signal thus overcoming the limitations of the time-domain methods.
- Selection of the window length is an important parameter which should be chosen while considering the ripple content of the DC current. The algorithm provides reliable detection results with 100% accuracy, with window size of 16 or 32 samples for the simulation test system, and 16, 32 or 64 samples for the experimental test system.
- This method is fast and is able to detect the low impedance faults within 1 ms and the high impedance fault in 2 ms with the ability to distinguish between faults and sudden load changing transients. Furthermore, this method is faster and computationally efficient than the wavelet transform based fault detection method.
- The efficacy is supported by performing sensitivity analysis for various fault impedances at various locations.
- As it uses standard FFT, it could be conveniently configured in the embedded system domain as opposed to the other fault detection methods such as wavelet transform.
- From the encouraging experimental results and owing to its faster and easier operation, STFT could be applied to the MTDC system which would be taken up in future.

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