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COMPOUND SEMICONDUCTOR DEVICES FOR LOW-POWER HIGH-EFFICIENCY RADIO FREQUENCY ELECTRONICS

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The power consumption of Radio Frequency (RF) electronics is a significant issue for Wireless systems. Since most wireless systems are portable and thus battery operated, reductions in DC power consumption can significantly reduce the weight and/or increase the battery lifetime of the system. As transmission consumes significantly more power than reception for most Wireless applications, previous efforts have been focused on increasing the efficiency of RF power amplification. These efforts have resulted in large increases in transmit efficiencies with research-grade amplifier efficiencies approaching 100%. In this paper, we describe our efforts on reducing power consumption of reception and other small signal RF functions. Additionally, recent power efficiency measurements on InP HEMT devices for transmission are presented. This work focuses on the needs of today's typical portable Wireless systems, which operate at frequencies up to several GHz.

INTRODUCTION

Wireless communication links are proliferating at a very rapid rate. Common examples include traditional applications like cellular and cordless telephones to new frontiers like Wireless networks for personal computers. Possible Wireless applications appear endless. A common theme to these systems is portability, which typically requires battery operation. Therefore, in order to maintain useful battery life, battery power consumption is a critical issue. This requires the lowest possible power consumption of the Wireless unit's RF signal processing as well as the highest possible transmission efficiencies.

Geometry scaling, which has greatly benefited the digital world, and in fact the digital signal processing typical of a Wireless system, generally does not apply to RF electronics. Certain power levels (i.e. transmit power), noise figure, and dynamic range requirements are fixed by specific system performance needs. This will then require RF device operation at specific optimal bias levels and specific device sizes to achieve these RF performance needs. Nevertheless, each RF function can be individually designed for these specific performance needs using appropriate device technology along with appropriate device scaling. This approach can provide significant power savings.

In this paper, a comparison between various compound semiconductor device technologies for ultra-low-power RF amplification is made. This is followed by an example MESFET-based ultra-low-power amplifier, which demonstrates some of the special issues of using devices at low bias levels for RF amplification. Finally, as an example of a high-efficiency RF device, L-band load-pull data of an InP power HEMT is presented.

DISCLAIMER

DEVICE TECHNOLOGIES

The first step in building a low-power high-efficiency RF amplifier is the selection of the appropriate device technology. Shown in Fig. 1 is a plot of the maximum frequency of oscillation (f_{max}) as a function of quiescent bias power for several different device technologies that we have considered for our applications. The bias voltages used during the measurement of this data were less than 1.5V, which may allow for the eventual operation from a single common battery cell. The device figure of merit f_{max} is the relevant parameter for device comparison as it is *the* frequency for unity power gain from a device. The unilateral transducer gain then increases at a rate of 20 dB/decade from the f_{max} point. Therefore, for an RF amplifier, f_{max} must be at least many times the operating frequency (i.e. at least 10x for 20 dB gain).

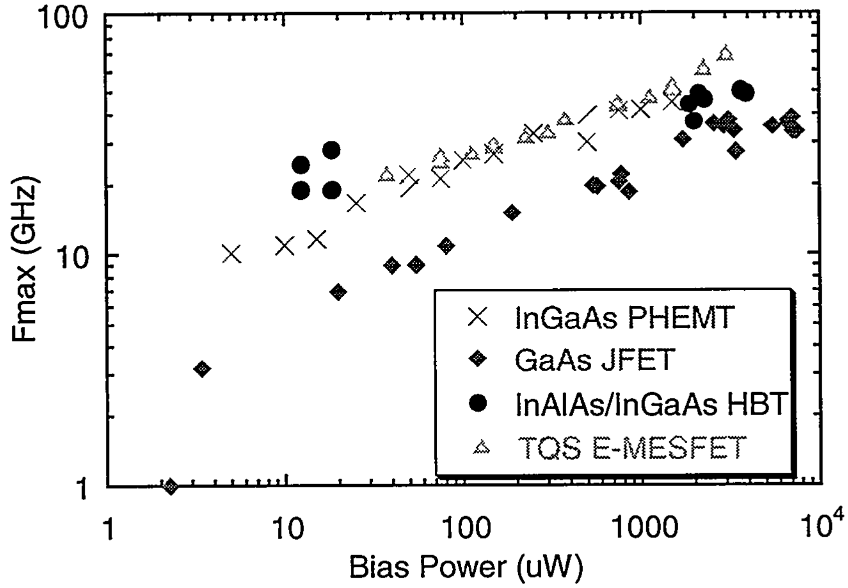


Fig. 1. Comparison of the maximum frequency of oscillation (f_{max}) for several different device technologies.

All of the device technologies shown in Fig. 1 perform reasonably well at low bias levels. It should be noted that since this plot is in terms of terminal bias power, device size plays a significant role in this figure of merit. For the FETs shown; the JFET [1], PHEMT [2], and MESFET devices were 0.3x40 μm^2; 0.2x10 μm^2 and 0.6x300 μm^2 respectively. The HBT was 12.5 μm^2. As shown in Fig. 1, the MESFET provides superior performance to the PHEMT for this case where the PHEMT is 1/30 the width of the MESFET and in the measured bias regime. At lower bias levels, the MESFET would be expected to suffer a greatly reduced f_{max} like that observed for the JFET. In contrast, due to the small size of the PHEMT device, it is expected that high-f_{max} will continue to be well behaved down to very low terminal currents. Thus, it is expected that the small PHEMT device's f_{max} should exceed that of the MESFETs at lower bias levels. Additionally, if the PHEMT was of a comparable width to the MESFET, the PHEMT would have a much higher f_{max}, but at a higher terminal current (larger PHEMT devices were observed to have f_{max}'s of about 100 GHz).

Since our operating frequency is at most several GHz, it is desired to obtain f_{max}'s of greater than 10 GHz at 10 µW bias levels. Several of the device technologies shown approach or exceed this metric. For low-power amplifiers, our current device technology of choice is InAlAs/InGaAs HBTs. HBTs appears to scale very well at low current densities and the use of InAlAs/InGaAs allows for a low operating voltage. Additionally, since high levels of integration are always desired, device technologies like HBTs with good 1/f noise performance are necessary for oscillator applications.

ULTRA-LOW POWER RF AMPLIFIER

To utilize these low-bias level devices in low-power RF circuits, we have found it necessary to use non-customary circuit approaches. Operating a device at low bias levels necessarily implies high terminal impedance. Since the operating voltage requirements remain about constant when the device is scaled, whereas the terminal current levels drop; the device terminal impedance must increase. This makes it very difficult if not impossible to impedance match to the device if conventional common source (emitter) circuit topologies are used. This impedance matching limitation stems from losses that are always present in matching networks and in particular commonly due to inductor loss.

One circuit approach of which we have seen reasonable success is shown in Fig. 2. In this circuit, a common gate input amplifier, which provides lower input impedance, is used to help facilitate the input match while still providing gain. Similarly, the use of a common source amplifier for the output stage helps achieve the output match due to its inherent low output impedance. With such a configuration, we have found the external matching networks easy to realize with standard chip inductors even when operating the circuit at several 10's of µA's of bias current. Unfortunately, this amplifier approach has two drawbacks. First, common gate amplifiers generally exhibit a larger noise figure as compared to a common source amplifier made from the same device. Secondly, a high impedance node exists between the two stages of this amplifier (at R3 in Fig. 2), which results in a bandwidth limitation. In fact, due to this high-impedance node, this amplifier topology is only realizable at Wireless frequencies in an integrated form where parasitic elements can be carefully controlled.

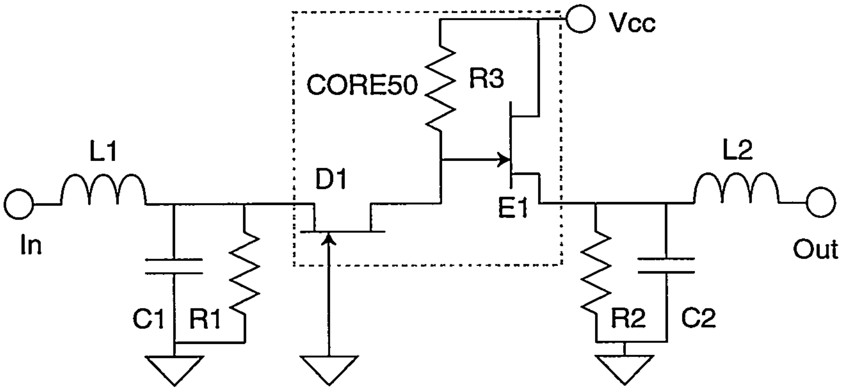


Fig. 2. Schematic diagram of a low power amplifier.

A microphotograph of an amplifier based on the circuit from Fig. 2 is shown in Fig. 3. This amplifier was fabricated using a standard commercial MESFET process [3]. Shown in Fig. 4 is a plot of the measured gain when the amplifier is matched at 217.5 MHz. The operating voltage was 3.6 V with a bias current level of 40 μA. The measured gain of 8.5 dB is similar to the target level of 10 dB. Similar L-band amplifiers have also been designed and tested.

As mentioned above, gain is not the only important performance metric for an RF amplifier. The amplifier's noise figure is also plotted in Fig. 4. The 4.5 dB minimum noise figure is a somewhat higher as compared to amplifiers operated at conventional bias levels, but still acceptable for our typical applications. Additionally, it should be noted that little consideration for noise performance has been made in the current design. Changes in matching conditions and device operating current densities should be able to reduce the noise figure.

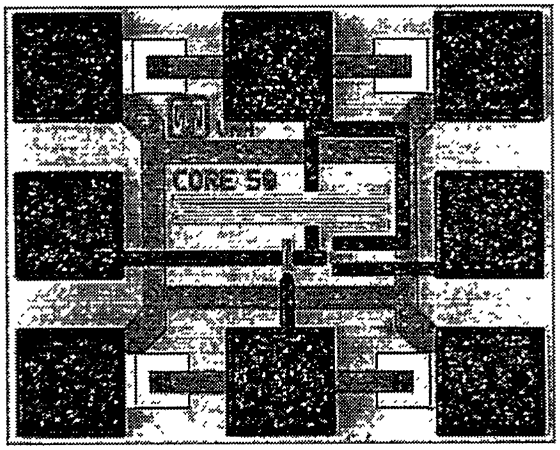


Fig. 3. Microphotograph of a low power RF amplifier fabricated in a commercial MESFET process.

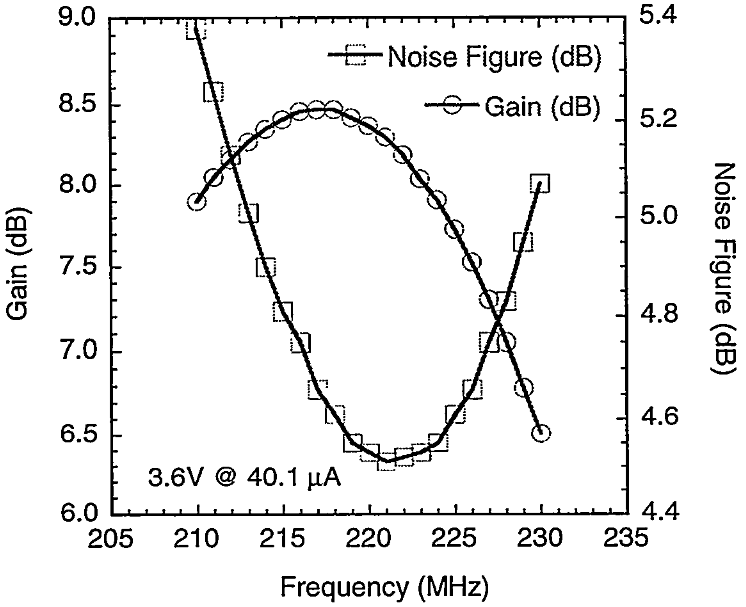


Fig. 4. Measured gain and noise figure of a low power RF amplifier.

Another important property of an amplifier is its large-signal or compression characteristics. Since this amplifier is operating a very low bias levels, it would be expected that it exhibits poor dynamic range. Fig. 5 is a plot of the amplifier's output power as a function of input power at 217.5 MHz. From this plot, one can see that the output power is about -30dBm at the 1dB compression point. This suggests that the amplifier is rather inefficient as the bias input power is 144 µW with a 1 dB compression occurring at microWatt RF power levels. Future designs are planned to incorporate a push-pull output stage, which will significantly improve the dynamic range while still maintaining a low quiescent bias level.

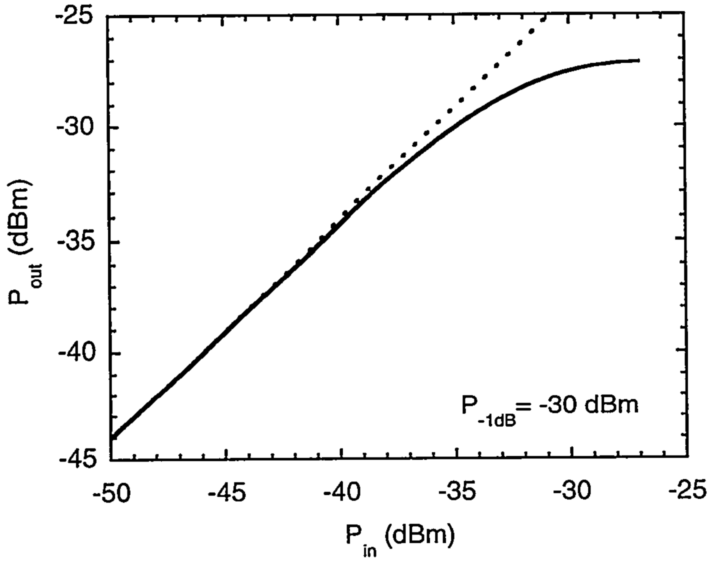
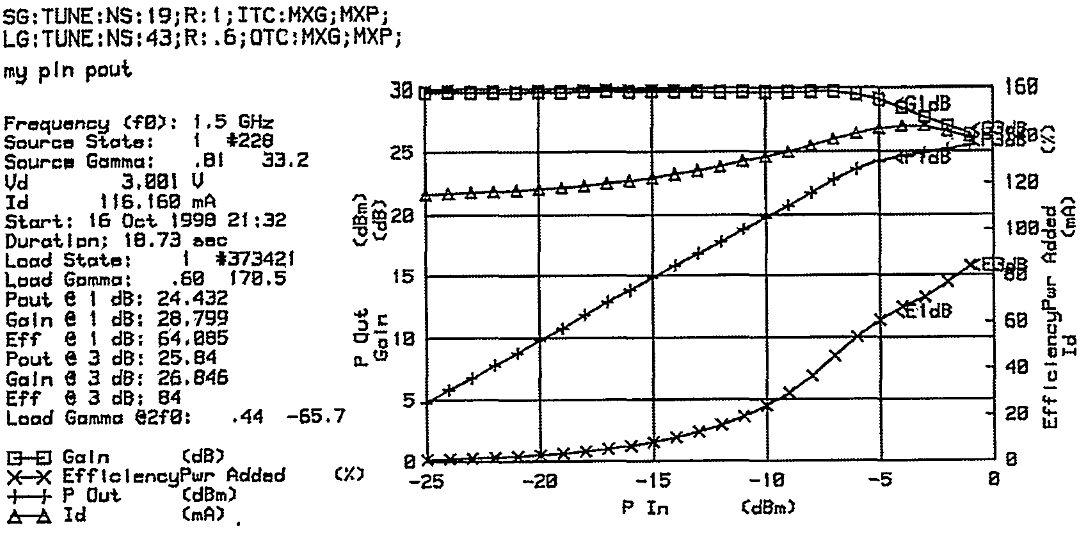


Fig. 5. Measured compression characteristics of the low-power amplifier (217.5 MHz).

HIGH-EFFICIENCY RF POWER AMPLIFICATION

As mentioned above, transmission is one of the main uses of energy in most Wireless systems. The application of advanced FET devices developed for millimeter wave applications promises to significantly improve Power Amplifier (PA) efficiencies in future transmitters. Shown in Fig. 6 are the results of a load-pull measurement at 1.5 GHz of a 0.1x600 μm^2 InP HEMT. These devices, which are similar to the ones described in reference [4], have intrinsic f_T's of over 100 GHz and f_{max}'s extrapolated to 600 GHz. Such devices would appear to have excessive speed for low GHz applications, but high device speed is advantageous for class-E amplification where rapid device turn-on and turn-off improves amplifier efficiency. Additionally, these devices offer high power densities (0.6 W/mm at 1.5 GHz) at low drain voltage (3 V). From this data it would appear that a class-E PA operating at 3V could achieve several Watts output power with 85 % PAE and 28 dB gain.



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SG:TUNE:NS:19;R:1;ITC:MXG;MXP;
LG:TUNE:NS:43;R:.6;OTC:MXG;MXP;
my pln pout

Frequency (f0): 1.5 GHz
Source State:    1  #228
Source Gamma:    .81   33.2
Vd          3.001 V
Id        116.160 mA
Start: 16 Oct 1998 21:32
Duration; 10.73 sec
Load State:      1  #373421
Load Gamma:    .60  170.5
Pout @ 1 dB: 24.432
Gain @ 1 dB: 28.799
Eff  @ 1 dB: 64.085
Pout @ 3 dB: 25.84
Gain @ 3 dB: 26.846
Eff  @ 3 dB: 84
Load Gamma @2f0:   .44  -65.7
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Fig. 6. Load-pull measurement of an InP HEMT at 1.5 GHz with 3 V drain bias. Power density and power added efficiency approach 0.63 W/mm and 85%, respectively when operated at 3 dB compression.

CONCLUSIONS

In this paper, various device technologies were compared for low-power RF electronics applications. Additionally, a low-power amplifier example was presented to demonstrate some of the special issues in successfully using these low-power devices. This amplifier was seen to provide useful gain at 217.5 MHz with only 120μW bias power. Finally, load-pull measurements on an InP HEMT were presented which demonstrates the possibility of extremely high-efficiency power amplification using advanced FET devices.

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