10-22-2001

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Publication Info

Published in *Applied Physics Letters*, Volume 79, Issue 17, 2001, pages 2832-2834.

Hu, X., Koudymov, A., Simin, G., Yang, J., Khan, M. A., Tarakji, A., Shur, M. S., & Gaska, R. (22 October 2001). Si_3N_4/AlGaN/GaN-Metal-Insulator-Semiconductor Heterostructure Field-Effect Transistors. Applied Physics Letters, 79 (17), 2832-2834. http://dx.doi.org/10.1063/1.1412591

AIP | Applied Physics Letters

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Citation: Applied Physics Letters **79**, 2832 (2001); doi: 10.1063/1.1412591
View online: http://dx.doi.org/10.1063/1.1412591
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/79/17?ver=pdfcov
Published by the AIP Publishing

Si_3N_4/AlGaN/GaN–metal–insulator–semiconductor heterostructure field–effect transistors

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(Received 5 July 2001; accepted for publication 24 August 2001)

We report on a metal–insulator–semiconductor heterostructure field-effect transistor (MISHFET) using Si_3N_4 film simultaneously for channel passivation and as a gate insulator. This design results in increased radio-frequency (rf) powers by reduction of the current collapse and it reduces the gate leakage currents by four orders of magnitude. A MISHFET room temperature gate current of about 90 pA/mm increases to only 1000 pA/mm at ambient temperature as high as 300 °C. Pulsed measurements show that unlike metal–oxide–semiconductor HFETs and regular HFETs, in a Si_3N_4 MISHFET, the gate voltage amplitude required for current collapse is much higher than the threshold voltage. Therefore, it exhibits significantly reduced rf current collapse. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1412591]

At present there is considerable interest in high power microwave devices based on GaN–AlGaN heterojunctions. Impressive powers in the range of 5–10 W/mm have already been demonstrated at operation frequencies ranging from 2 to 10 GHz.[1] However, two key problems still remain. First, the gate leakage current for heterostructure field-effect transistor (HFET) devices is typically 10–100 μA/mm at room temperature and it rapidly increases by about an order of magnitude at 300 °C and by about three orders of magnitude at 750 °C.[2] This temperature induced gate leakage deteriorates the device's radio-frequency (rf) performance and increases the low and high frequency noise levels. It also accelerates thermal stress related device degradation. Second, HFETs are known to exhibit current collapse with a high rf-input drive on the gate.[3–6] This phenomenon significantly reduces rf powers below the values expected from dc-transfer curves.

Recently we have proposed and demonstrated a metal–oxide–semiconductor HFET (MOSHFET)[7–9] with dramatically reduced gate leakage currents using a thin SiO_2 insulator layer under the gate. In spite of the four to six orders of magnitude decrease in gate leakage current the saturation current stays the same or even increases. Even at 300 °C the gate leakage current of MOSHFETs remains about four orders of magnitude below that of HFETs.[10] However MOSHFET and HFET devices fabricated from the same wafer exhibit nearly the same degree of current collapse.[11] In other words, SiO_2 layer incorporation under the gate does not affect the mechanism responsible for current collapse in AlGaN/GaN HFETs. On the other hand, several groups have recently shown that Si_3N_4 passivation in the source–gate and gate–drain regions reduces the degree of current collapse.[12,13] However, to date, no clear explanation has been given as to the cause for this reduction. We recently proposed a possible mechanism for current collapse in AlGaN/GaN HFETs.[14] Our proposed model was based on the gate voltage induced strain in the AlGaN buffer and underlying channel. According to the proposed mechanism, a Si_3N_4 passivating layer, being a very hard film, may significantly decrease the degree of current collapse by preventing strain induction in the AlGaN barrier from the applied gate bias. In contrast, for SiO_2, being a soft material, its use as a passivation layers does not affect current collapse. Thus, in principle, using a silicon nitride layer for channel passivation and the gate insulator can overcome both the gate leakage and the current collapse problems. The Si_3N_4 layer can be deposited in the channel region prior to gate fabrication. Indeed, such a device was reported by Chumbes *et al.*[15] They did observe the expected current collapse reduction. However no improvement in the gate leakage current was observed, which they attributed to the poor quality of the gate insulator. We report here a Si_3N_4 metal–insulator–semiconductor HFET (MISHFET) that exhibits simultaneous current collapse and gate leakage current reduction. The gate leakage current was four orders lower than a HFET with identical geometry fabricated on the same wafer. It was thus nearly the same as what was previously reported for a MOSHFET.[9] This gate leakage current improvement was obtained while maintaining excellent dc and rf performance and high temperature stability.

The device structure schematically shown in the inset of Fig. 1 was grown on a sapphire substrate using low-pressure metalorganic chemical vapor deposition (MOCVD). A device fabrication procedure similar to that reported earlier[7–9] was then used. Three sets of devices with identical geometry (gate length 1 μm, source–drain opening 5 μm, gate width 100 μm) were fabricated on the same wafer. They consisted of a HFET, a MOSHFET (100 Å SiO_2 under the gate and in the source–gate and drain–gate regions) and a MISHFET (100 Å Si_3N_4 insulator replacing SiO_2). Both the SiO_2 and the Si_3N_4 layers were deposited using plasma enhanced chemical vapor deposition (PECVD).

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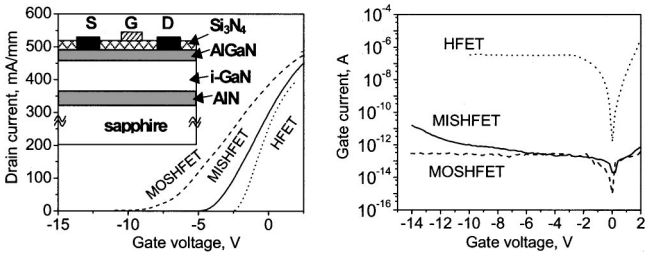

FIG. 1. Gate voltage dependencies of the drain current (a) and gate leakage current (b) for identical geometry HFET, MOSHFET, and MISHFET devices fabricated from the same wafer. The inset shows the schematic structure of the Si_3N_4/AlGaN/GaN MISHFET device.

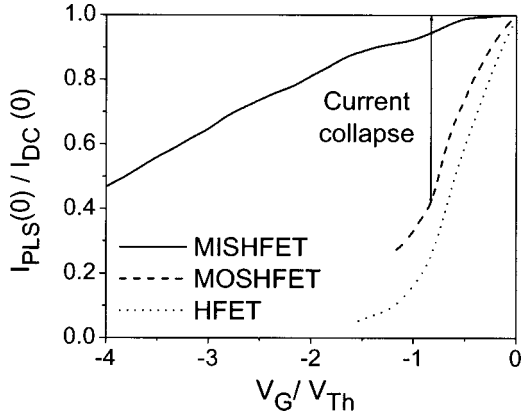

FIG. 2. Dependencies of pulsed drain "return" current (normalized to the dc value) on the pulsed gate voltage amplitude (normalized to the threshold voltage) for HFET, MOSHFET, and MISHFET devices. The gate voltage pulse amplitude (1 μs pulse width at 50% duty cycle) varies from 0 V to a value of V_G. The "return" current is the pulsed current when the gate voltage pulse returns to zero.

In Figs. 1(a) and 1(b) we include the transfer curves and the gate leakage current, respectively, for the three device types. As can be seen either the oxide or the nitride insulator layers reduce the gate leakage by about four orders below that measured for the HFET. Compared to a HFET both MISHEFTs and MOSHFETs have a higher threshold voltage (larger gate to channel separation). However the threshold voltage increase for the MOSHEFT is higher. This results partially from the higher dielectric permittivity of Si_3N_4. For our epilayer structure Hall measurements yielded a sheet carrier density of $n_s \approx 5\times 10^{12}$ cm^{-2}. The threshold voltage for MISHFET, MOSHFET, and HFET devices can be simply estimated from the gate–channel capacitance.[7] For the HFET, taking the thickness of the AlGaN barrier layer to be $d_b = 250$ Å, we find $V_{gt} = qn_s/C_b \approx 2.5$ V (here $C_b = \epsilon_0\epsilon_b/d_b$ is the unit area capacitance of the barrier layer, $\epsilon_b \approx 9$ being the dielectric permittivity of AlGaN layer). This agrees quite well with the measured value of the HFET threshold voltage $V_{\text{th}} \approx 2.5$ V (see Fig. 1). In a similar way the threshold voltages for MOSHFET and MISHFET devices were estimated using the SiO_2 and Si_3N_4 layer thicknesses ($d_{01} = d_{02} = 100$ Å) and their corresponding dielectric permittivities $\epsilon_1 = 3.9$ and $\epsilon_2 = 7.5$. These estimations resulted in a threshold voltage of $V_{\text{th1}} = 4.8$ V for the MOSHFET and $V_{\text{th2}} = 3.7$ V for the MISHFET. As seen from Fig. 1 there is good agreement between the measured and the estimated values of MISHFET threshold voltage V_{th}. This result suggests that the surface charge density at the Si_3N_4/AlGaN interface is low and hence does not contribute significantly to the threshold voltage. However for the MOSHFET the calculated threshold voltage of 4.8 V is significantly lower than the experimental value of about 8 V. Two factors may contribute to this difference. First, the actual thickness of the deposited SiO_2 layer may be higher than 100 Å; second, the surface charge at the SiO_2/AlGaN interface may decrease the voltage drop across the AlGaN barrier layer thus increasing the threshold voltage.

At zero gate bias the saturation currents for the MISHFET, and the HFET, are nearly equal to but lower than that for the MOSHFET. Also, transmission line model (TLM) measurements of the MIS and the MOS structures in our study showed that the SiO_2 layer does not have any effect on the channel conductivity whereas the Si_3N_4 layer decreases it by 20%–30%. This can be explained by modification of the strain and/or spontaneous polarization by Si_3N_4. Since Si_3N_4 is much harder than SiO_2, its deposition over the channel can decrease the tensile stress and hence the two-dimensional electron gas (2DEG) sheet carrier density. In addition, it also forms a much stronger bond to AlGaN due to having a similar anion.

We also measured the gate leakage current for the Si_3N_4 MISHFET as a function of the temperature. It increases from about 90 pA/mm at room temperature to 1000 pA/mm at 300 °C thereby still remaining three to four orders of magnitude below that for HFET. HFET and MOSHFET dc saturation currents decrease with increasing temperature. This temperature dependence is approximately the same as that of the electron saturation velocity.[10] However for the Si_3N_4 MISHFET the saturation current remains fairly constant in the 25–250 °C temperature range. This difference may be due to activation of the surface states at the Si_3N_4/AlGaN interface, or from strain relaxation in the AlGaN layer induced by the Si_3N_4 film. The reduced strain should in turn increase the 2DEG sheet carrier density in the 2DEG at the AlGaN/GaN interface.

In order to compare current collapse effects in the MISHFET, MOSHFET, and HFET devices of Fig. 1 their pulsed $I-V$ characteristics were measured. These pulsed transfer curves are shown in Fig. 2. For these measurements the source–drain bias was fixed at a value well in the saturation regime. The gate voltage was then pulsed using a 1 μs pulse with a 50% duty cycle. The gate–voltage pulse amplitude varied from 0 V (with the channel open) to a value below the device threshold voltage. The "return" pulsed current, i.e., the pulsed current when the gate voltage pulse returns to zero (Fig. 2), was measured. Since the three device types have different threshold voltages, in Fig. 2 we have plotted the gate voltage normalized to the threshold voltage and the pulse current normalized to the dc current at zero gate bias. As seen at a nonzero value of the gate bias pulse, the device current does not return to its dc value I_{dc} ($V_g = 0$). This is a manifestation of current collapse. After a negative voltage is applied to the gate it takes a certain time for the current to recover to its peak value when the gate voltage returns to $V_g = 0$. Therefore, the difference between dc and pulsed values of drain currents at zero gate voltage (illustrated by the line with arrowheads in Fig. 2) is a direct measure of rf-current collapse. As can be seen, this reduction

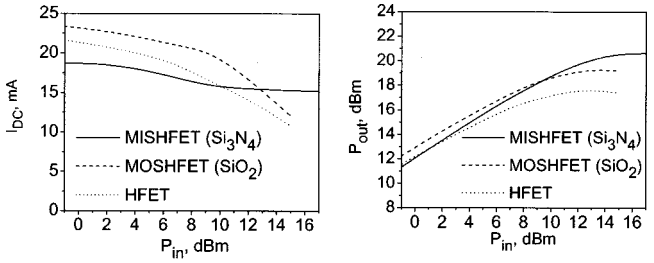

FIG. 3. dc current at the operating point and the rf output power as a function of the input continuous wave rf power measured at 2 GHz for HFET, MOSHFET, and MISHFET devices. The drain bias voltage $V_D=24$ V for all the devices.

in current is present for all the devices. However unlike the MOSHFET and the HFET, for the Si_3N_4 MISHFET the current collapse is only appreciable when the gate voltage amplitude values are several times that of the threshold voltage. Such a gate–voltage swing is never reached in regular class A operating mode. Consequently for class A operation the MISHFET does not exhibit any significant rf current collapse. A comparison of rf power measurements for the MISHFET, MOSHFET, and HFET is shown in Fig. 3. These on-wafer measurements were made at 2 GHz using a Maury automated tuner system. Quite moderate drain bias values of 24 V were used to rule out the effects of self-heating. Along with rf output power the dc current was also measured as a function of the input rf drive at a fixed gate bias. As seen from Fig. 3 for the MISHFET the dc current changes only slightly with an increase of the input rf drive. The slight decrease is close to that expected from device nonlinearity.[11] In contrast, a significant reduction in dc current was observed for the HFET and MOSHFET due to current collapse. This difference is also clearly seen in the output rf power. At low input rf drive the output powers for all three device types are within 1 dB. This difference may arise from gain tuning and impedance differences. However at large input rf drive (saturation) the output power for the MISHFET exceeds that of the MOSHFET and HFET by more than 3 dB. This increase is directly from a reduction of rf current collapse. Note that for all the device types the saturation output power values are in good agreement with those estimated from the drain bias and dc current at the operating point. For example, for the MISHFET the knee voltage was measured to be $V_{\mathrm{kn}}\sim 4$ V; for the drain bias $V_D=24$ V and the operating current at high input rf power, $I_{\mathrm{dc}}\sim 17$ mA, the estimated output rf power in class A mode of operation, would be $P_{\mathrm{out}}\sim(V_D-V_{\mathrm{kn}})\times I_{\mathrm{dc}}/2\sim 0.17$ W, which is quite close to the measured value of P_{out}.

One possible explanation for our observations of reduced current collapse in the MISHFET is based on strain field modification by the applied gate bias. We recently reported that current collapse results from increased source–gate and gate–drain resistance but not from the channel resistance under the gate.[14] A negative gate bias results in an electric field in the same direction as the built-in piezo field at the AlGaN/GaN interface. This should therefore increase the tensile stress in the AlGaN material directly under the gate, which in turn should increase the compressive strain in the AlGaN layer in the source–gate and gate–drain openings. This increase of compressive strain (decrease of tensile strain) should reduce the 2D sheet carrier density, thereby increasing the gate–source and gate–drain series resistance. Only slow processes of the piezoelectric charge adjustment and/or trapping effects are available to these regions to offset this piezoelectric charge reduction. This therefore gives rise to current collapse. Simultaneously, the decrease of the 2D sheet carrier density between the gate and the drain results in current saturation in that region, which therefore creates an additional ''induced gate'' that limits the current and distorts the output signal wave form. However, when these source–drain and gate–drain opening regions are passivated by the hard Si_3N_4 layer, the compressive strain induced in the AlGaN barrier should decrease significantly and hence the degree of current collapse should also be reduced.

In summary, we have reported on a Si_3N_4 based MISHFET in which the use of a nitride insulator in the channel and under the gate simultaneously reduces current collapse and the gate leakage current. The gate leakage current decreases by four orders of magnitude. It increases only by one order when the device temperature is raised to 300 °C, thereby still retaining an improvement of three orders with respect to regular HFETs.

This work, performed at the University of South Carolina, was supported by the Ballistic Missile Defense Organization (BMDO) under U.S. Army SMDC Contract No. DASG60-98-1-0004, monitored by Tarry Bauer, Dr. Brian Strickland, and Dr. Kepi Wu.

[1] S. Sheppard, W. L. Pribble, D. T. Emerson, Z. Ring, R. P. Smith, S. T. Allen, and J. W. Palmour, 58th Device Research Conference, 19–21 June 2000, Denver, CO, DRC Digest, p. 37.
[2] I. Daumiller, C. Kirchner, M. Kamp, K. J. Ebeling, and E. Kohn, IEEE Electron Device Lett. **20**, 448 (1999).
[3] C. Nguyen, N. X. Nguyen, and D. E. Grider, Electron. Lett. **35**, 1380 (1999).
[4] E. Kohn, I. Daumiller, P. Schmid, N. X. Nguyen, and C. N. Nguyen, Electron. Lett. **35**, 1022 (1999).
[5] R. Dietrich, A. Wieszt, A. Vescan, H. Leier, J. M. Redwing, Karim S. Boutros, K. Kornitzer, R. Freitag, T. Ebner, and K. Thonke, MRS Internet J. Nitride Semicond. Res. **5**, 1 (2000).
[6] S. Binari, K. Ikosssi, J. Roussos, W. Kruppa, D. Park, H. Dietrich, D. Koleske, A. Wickenden, and R. Henry, IEEE Trans. Elec. Dev. **48**, 465 (2001).
[7] M. Asif Khan, X. Hu, G. Simin, A. Lunev, J. Yang, R. Gaska, and M. S. Shur, IEEE Electron Device Lett. **21**, 63 (2000).
[8] M. Asif Khan, X. Hu, G. Simin, J. Yang, R. Gaska, and M. S. Shur, Appl. Phys. Lett. **77**, 1339 (2000).
[9] G. Simin, X. Hu, N. Ilinskaya, J. Zhang, A. Tarakji, A. Kumar, M. Asif Khan, R. Gaska, and M. S. Shur, IEEE Electron Device Lett. **22**, 53 (2001).
[10] G. Simin, X. Hu, A. Koudymov, J. Yang, M. Asif Khan, A. Tarakji, M. S. Shur, and R. Gaska, Phys. Status Solidi A **188**, 2 (2001).
[11] A. Tarakji, G. Simin, N. Ilinskaya, X. Hu, A. Kumar, A. Koudymov, J. Zhang, and M. Asif Khan, M. S. Shur, and R. Gaska, Appl. Phys. Lett. **78**, 2169 (2001).
[12] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, IEEE Electron Device Lett. **21**, 268 (2000).
[13] L. F. Eastman, V. Tilak, J. Smart, B. M. Green, E. M. Chumbes, R. Dimitrov, H. Kim, O. S. Ambacher, N. Weimann, T. Prunty, M. Murphy, W. J. Schaff, and J. R. Shealy, IEEE Trans. Electron Devices **48**, 479 (2001).
[14] G. Simin, A. Koudymov, A. Tarakji, X. Hu, J. Yang, M. Asif Khan, M. S. Shur, and R. Gaska, Appl. Phys. Lett. **79**, 2651 (2001).
[15] E. Chumbes, J. Smart, T. Prunty, and J. Shealy, IEEE Trans. Electron Devices **48**, 416 (2001).