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Si-CdSSe Core/Shell Nanowires with Continuously Tunable Light Emission

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ABSTRACT

Uniform Si-CdSSe core/shell nanowires were controllably synthesized by a multisource thermal evaporation route. Both the silicon core and the alloyed CdSSe shell are of high-quality and single crystalline. The silicon core is grown via the gold-catalyzed VLS route with a silicon wafer piece at the high temperature zone as the source. These preferentially grown Si nanowires further serve as templates for the afterward depositions of CdSSe shells using CdS/CdSe powders at the low temperature zone of the furnace as sources. The composition/band gap of the shells can be continuously modulated by the S/Se ratio of the evaporation sources, making these prepared heterostructures have strong and spectral position/color largely tunable light emission at the visible region. These kind of structures may have potential applications in multicolor nanoscaled light-emitting devices. This flexible growth route will also be applicable for controllable synthesis of other Si wire containing heterostructures.

One-dimensional (1D) semiconducting nanostructures are important building blocks for designing nanoscaled optoelectronic devices.[1] Among these structures, radial core/shell nanowire heterostructures in particular have attracted increasing attention recently, due to their special structural characteristics and having diverse applications as functionalized components like field-effect transistor, solar cells, light-emitting diodes, high electron mobility devices, and memory devices.[2−13] Realizing continuously tunable physical properties of such kind of heterostructures should be of interest for their applications in multifunctional optoelectronic devices. Hence, the band gap or sub-band gap of the structures should be largely tunable since it basically determines the electronic and optical properties of the semiconductor structure. Alloying of semiconductors is commonly used to achieve various band gap energies or tunable properties of semiconductor structures. CdS and CdSe, two important II−VI semiconductors with highly efficient light emission in the visible region, are expected to have many applications in nanophotonic devices. In particular, alloying these two compounds can form ternary CdSSe alloys with a complete compositional modulation and correspondingly a wavelength-tunable light emission in the visible region from blue-green to red.[14] Moreover, 1D structures of such kind of alloys show color-tunable optical waveguide properties and can give position-tunable lasing under pulsed light excitation,[15] indicating their potential for nanoLEDs and nanolasers. On the other hand, silicon, the standard electronics material in modern semiconductor industry, has recently attained attraction for photonics due to quantum effects in Si-based low dimensional structures.[16] In this regard, 1D Si-based nanostructured heterostructures are of special interest for potential applications in nanoscaled electronic and optical devices.[9−11] However, to the best of our knowledge, Si-based core/shell nanowire heterostructures with a continuous tuning of the band gap have not been reported. In this work, we developed a multisource thermal evaporation route to controllably synthesize Si-CdSSe core/shell nanowires. Both the silicon core and the alloyed CdSSe shell are high-quality single crystalline, and the composition, i.e., the band gap of the shell can be tuned continuously with a strong and color-tunable light emission in the visible region.

To synthesize these composition-tunable core/shell heterostructures, we used three evaporation sources. One is an oxidation layer-removed silicon wafer piece, which provides the silicon source for the core growth. The other two are CdS and CdSe powders, which are the sources for the growth

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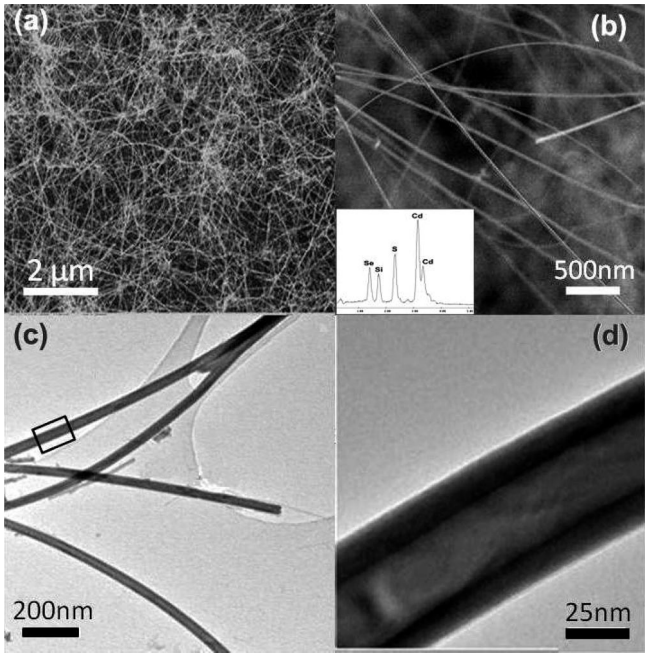

Figure 1. (a,b) Typical SEM images with different magnifications of the as-grown core/shell nanowires; (inset of b) the corresponding EDS spectrum of the sample; (c,d) low-magnification and the locally amplified TEM images of the sample, respectively.

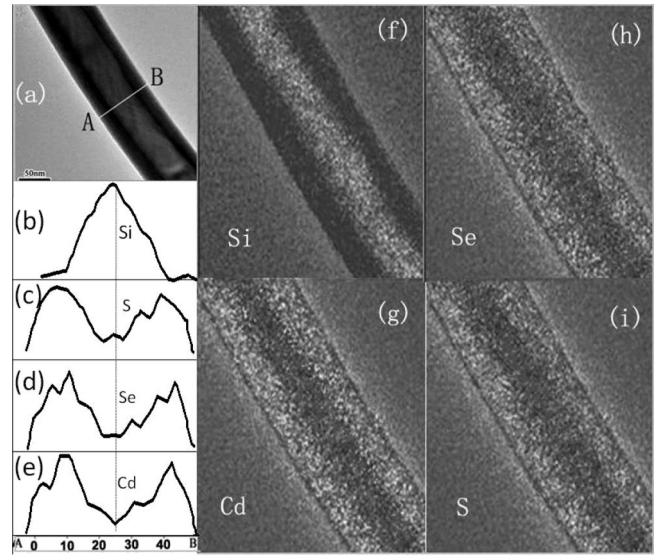

Figure 2. (a) TEM morphology image of one representative wire from the sample; (b−e) the line-element analyses for elements Si, S, Se, and Cd, respectively, along the marked line A−B in image a; (f−i) the respective two-dimensional element mapping of this wire for the detected four elements.

of CdSSe shells. In a typical procedure, a piece of cleaned silicon wafer (0.5 × 2 cm) was etched in 5% HF solution for several minutes to remove the oxidation layer at the surface. Then the silicon piece was rinsed with deionized water and dried with a blower, and was immediately placed at the center of a quartz tube chamber (5.5 cm in diameter, 65 cm in length), which was inserted into a horizontal tube furnace (Carbolite). Some CdS and CdSe powders (Alfa Aesar, 99.995% purity) with a defined molar ratio were loaded into a ceramic boat respectively, and were placed upstream of the gas flow. The distances from the CdS powder and the CdSe powder to the center of the furnace are ∼8 and ∼6 cm, respectively. A piece of quartz substrate (length is 2 cm) sputtered with 6 nm Au film for collecting sample was put downstream of the gas flow, about 12 cm from the center of the furnace. The tube chamber was evacuated and back-flushed with Ar gas until the desired pressure of 100 mbar was reached. A constant flow of argon of 50 sccm was used. The chamber temperature was set to 1080 °C with a heating rate of 40 °C/min, and maintained at its peak temperature for 60 min. After the growth, the furnace was naturally cooled to room temperature. Due to the temperature gradient, the temperature at the substrate was measured as ∼600 °C, and the local temperature at the CdS powder, the CdSe powder, and the silicon piece, are 650, 750, and 1080 °C, respectively. The experimental setup and sample growth parameters are illustrated schematically in Figure S1 (see the Supporting Information).

Figure 1a,b shows the typical scanning electron microscopy (SEM) images of the as-grown core/shell nanowires in different magnifications with diameters of about several tens of nanometers, and length of several tens of micrometers. The inset of Figure 1b is the corresponding energy dispersive X-ray spectroscopy (EDS) of the sample, which shows that the obtained nanowires are composed of the elements Si, S, Se, and Cd. The low-magnification transmission electron microscopy (TEM) image (see Figure 1c) further demonstrates that the obtained nanowires have uniform radial size with a diameter of approximately 50 nm. Figure 1d gives the locally amplified TEM image of the marked area in Figure 1c. The clear bright/dark contrast variation along the length/diameter mainly reflects that the brighter core and the darker shell of the wires are consisting of materials with different mass. This structure is very uniform along the length with the bright interior and the dark shell having a size of ∼30 and ∼15 nm, respectively.

Figure 2a is the TEM morphology image of one representative wire from the grown sample, and Figure 2b−e is its line-element analysis for elements Si, S, Se, and Cd, respectively, along the marked line A−B in Figure 2a. From these element distribution profiles, we estimate that the elemental Si is almost completely located in the middle region, while the elements Cd, S, and Se are mainly distributed in the shell region of the wires. Figure 2f−i gives the respective two-dimensional (2D) element mapping of this wire for the detected four elements. These results further support that the Si is only located in the core region of these wires (see Figure 2f), whereas the Cd, S, and Se are mainly located in the shell regions along the wires. The much lower signals detected in the core region (see Figure 2g−i) are due to the spherical geometry of the shell covered wires. Moreover, the evaluated atomic ratio (S + Se)/Cd from the detected element signals are very close to 1. These elemental analysis results prove that the obtained nanowires are Si-CdSSe core/shell heterostructures with the lighter Si in the core and the heavier CdSSe containing compound in the shell. This result is in good agreement with the observed bright/dark contrast in the TEM images.

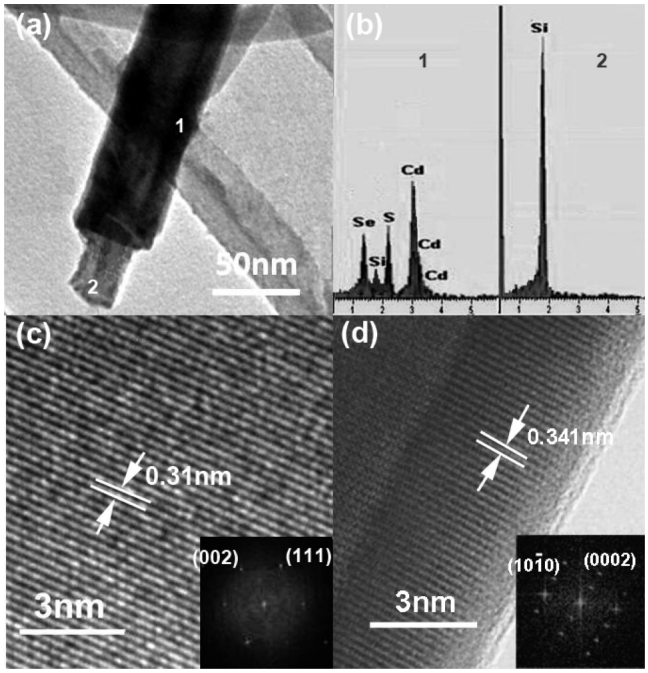

Figure 3. (a) TEM image of a broken core/shell wire from one of the samples after strong sonication; (b) dot EDX from the shell region (marked with "1") and the exposed core end (marked with "2") of the wire shown in image a, respectively; (c,d) corresponding HRTEM images taken from the exposed core and the darker shell region, respectively; (inset of image c) the corresponding fast Fourier transformation of this image; (inset of image d), the corresponding Fast Fourier Transformation of the edge region in this image.

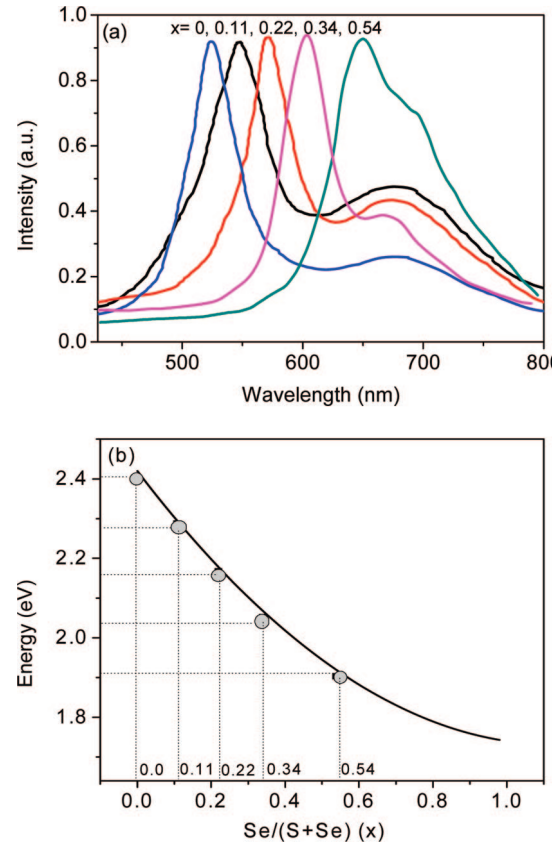

Figure 4. (a) Micro-PL spectra from the as-grown single Si-$CdS_{1-x}Se_x$ core/shell nanowires with $x = 0$, 0.11, 0.22, 0.34, and 0.54, respectively. (b) Fitted band gap at different composition x using eq 1 (solid line), and the corresponding peak energy values of the position-tunable PL emission band shown in image a (solid dot).

Figure 3a shows the TEM image of a broken core/shell wire from one of the samples after strong sonication. As seen here, the outer shell layer was peeled at its wire end during the sonication processing, exhibiting a clear coaxial cablelike structure. This image gives direct evidence that the obtained nanowires are indeed so-called core−shell structures. Figure 3b give the energy dispersive X-ray spectra (EDX) from the shell region (marked with "1") and the exposed core end (marked with "2") of the wire shown in Figure 3a, respectively. Again, Si was only detected in the exposed core (see right curve), and mainly Cd, S, Se were detected in the shell region (see left curve). The additional small amount of Si should come from the adjacent core due to the limited space resolution of the focused electron beam. Figure 3c,d is the corresponding high-resolution TEM images (HRTEM) taken from the exposed core and the darker shell region, respectively. The results indicate that both core and shell are of high quality and single crystalline. Moreover, no apparent oxide layer was found at the surface of the Si core, which is consistent with the result of EDX. The exposed core has a lattice spacing of 0.31 nm (Figure 3c), corresponding to the interplanar *d*-spacing of the {111} lattice planes of the diamond-cubic Si. The fast Fourier transformation (FFT) of Figure 3c (see its inset) further confirms that the crystalline Si core grows with a cubic crystal structure along the ⟨111⟩ direction. Figure 3d shows that the interface between core and shell is very sharp on the atomic scale, and that the depth of the shell along the wire axis is highly uniform. FFT of the shell region (see the inset Figure 3d) confirms the single-crystal hexagonal structure of the CdSSe which grows along the ⟨0002⟩ direction and is in good agreement with the measured lattice spacing of 0.341 nm. The lattice parameters of $CdS_{1-x}Se_x$ ($0 < x < 1$) alloys are in between those of CdS and CdSe, which obey the so-called Vegard's law.[17] According to the Vegard's law for ternary $CdS_{1-x}Se_x$ compounds and using the observed {0002} interplanar distance (half of the *c* value) (see Figure S2 in the Supporting Information), the composition *x* of the CdSSe shell in the above-discussed sample can be determined as $CdS_{0.54}Se_{0.46}$.

When changing the relative amount (molar ratio) of CdS and CdSe powder sources, such kind of core/shell heterostructures can be repeatedly obtained, and the respective composition *x* of the CdSSe shell is found to be tightly related to the molar S/Se ratio of the evaporation sources. Accordingly, series of Si-CdSSe nanowires with different shell compositions (*x* value) were successfully obtained through this route. Since the band gap of the $CdS_{1-x}Se_x$ alloy is determined by the composition *x*, the physical properties of the obtained Si-$CdS_{1-x}Se_x$ heterostructures are accordingly tuned by the *x* value. We confirmed this by room-temperature photoluminescence (PL) measurements with a homemade μ-PL system using a He−Cd laser (442 nm) as excitation source. Figure 4a shows the μ-PL spectra from the as-grown single Si-$CdS_{1-x}Se_x$ core/shell nanowires with $x = 0$, 0.11,

0.22, 0.34, and 0.54, respectively. All the spectra exhibit two emission bands. The sharper band shows a tunable position from 514 nm (green color) to 652 nm (red color) with the composition x changing from 0 to 0.54, apparently coming from the alloyed CdSSe shell-related emission.[14] It is known that the band gap of $CdS_{1-x}Se_x$ ($0 \leq x \leq 1$) alloy is determined by an interpolation between those of the two binaries with additional nonlinear bowing parameter[18]

$$E_g(CdS_{1-x}Se_x) = xE_g(CdSe) + (1-x)E_g(CdS) - x(1-x)b \quad (1)$$

where E_g(CdS) is 2.42 eV, E_g(CdSe) is 1.74 eV, and the bowing parameter b is 0.54 for $CdS_{1-x}Se_x$ at room temperature. Using the alloy composition x determined as discussed above, we can obtain the band gap value of the shell for each composition x. The fitted band gap at different composition x using eq 1 is plotted as solid line in Figure 4b. A good overall agreement is observed between the peak energy of the position-tunable emission band (see solid dots in Figure 4b) and the fitted band gap value at each given x, indicating these bands are surely from the band edge emission of the shells in the heterostructures. The other emission band is broad and centered at around 680 nm for all the grown core/shell nanowires with different x value. The emission position is largely different from the observed defect-related emission band (~1.60 eV) in CdSSe nanowires.[19] A similar emission band was reported in some Si-based heterostructures.[20] Since the diameter of the core is much too large for quantum confinement in Si, the origin of this band is probably related to defects at the interface of the Si nanowire core to the CdSSe shell.

As for the formation of the core/shell nanowires, the silicon wafer piece located in the middle of the tube, that is. the highest temperature, represents the Si source for the core growth of these wires. A lot of holes can be found at the surface of the Si piece after growth which supports our assumption (see Figure S3 in Supporting Information). In a control experiment, Si nanowires were grown on a quartz substrate without loading the CdS/CdSe scource powders into the tube (see Figure S4 in Supporting Information). Such grown Si nanowires can further serve as templates for the deposition of CdSSe shells, which is related to the slow evaporation of CdS/CdSe powders at the lower temperature zone. In such experiment, the evaporation rates (local temperatures) of the sources are very important for the formation of high-quality core/shell nanowires. The evaporation rates of CdS/CdSe powders should be low enough while that of the silicon wafer piece should be high enough, which starts the core Si nanowires preferentially before depositing the CdSSe. At the same time, a slower deposition rate of CdSSe on the Si core helps to get the very uniform shells around the Si wires. A too high evaporation temperature of CdS/CdSe will make it hard to get depth-uniform CdSSe shells and even results in various other kinds of structures, such as sandwichlike and/or biaxial structures coexisting with the core/shell structures in a same sample. In addition, we can find the catalysts still at the top of the core−shell nanowires (see Figure S5 in Supporting Information) during the TEM examinations. The catalyst is directly linked to the Si nanowire core, and the shell of the wire is seemingly extended to cap these catalyst particles. This result indicates that Au catalyst only initiates the growth of Si nanowires in the cores through the VLS mechanism, which is in agreement to the proposed two-step formation mechanism of these core/shell structures. From the above results, no detectable oxygen exists at the surface of the Si core or at the Si/CdSSe interface. The subsequent deposition of a CdSSe layer on the preformed cores may prevent their surfaces from possible oxidation by the remaining trace oxygen in the chamber.

In summary, we developed a flexible multisource thermal evaporation route to controllably synthesize uniform Si-CdSSe core/shell nanowires. The core is cubic structured crystalline Si with the growth along ⟨111⟩ direction and with a diameter around 30 nm. The shell is hexagonal structured CdSSe alloy with the ⟨0002⟩ growth direction and with the width about 15 nm. The composition/band gap of the shells can be continuously modulated by the S/Se ratio of the evaporation sources. PL measurements of single nanowires show that these prepared heterostructures have strong light emission in the visible region with their spectral positions largely tunable. These kind of structures may find important applications in color-tunable nanoscaled light-emitting devices.

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Supporting Information Available: The schematic setup and experimental parameters for the sample growth, the method for shell composition decision, SEM images and EDS profile of the Si piece after growth, SEM image and EDS profile of the collected sample with only Si piece as the source material, and TEM image of one catalyst-containing core−shell nanowire. This material is available free of charge via the Internet at http://pubs.acs.org.

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