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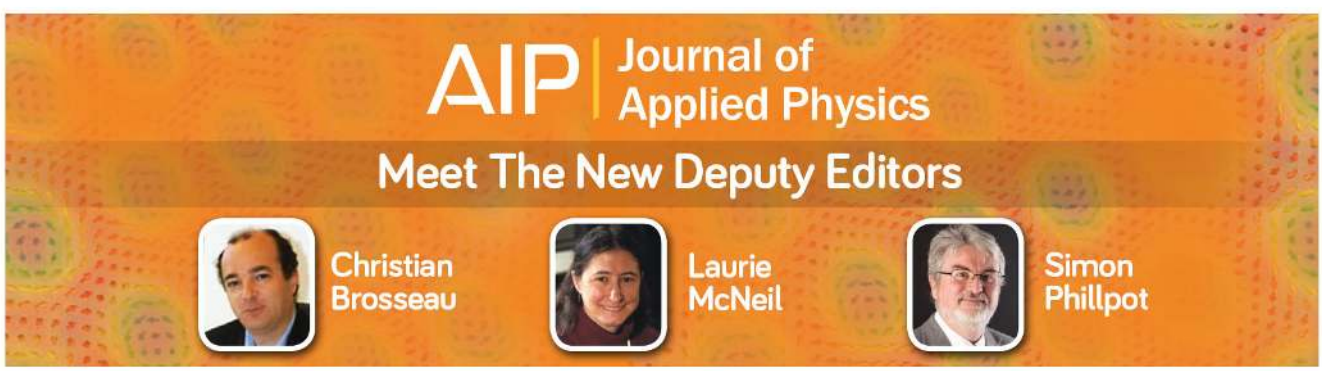

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Si/Ge hetero-structure nanotube tunnel field effect transistor

A. N. Hanna and M. M. Hussain[a)]
Integrated Nanotechnology Lab, Computer Electrical Mathematical Science and Engineering, King Abdullah University of Science and Technology, Thuwal 23955-6900, Saudi Arabia

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We discuss the physics of conventional channel material (silicon/germanium hetero-structure) based transistor topology mainly core/shell (inner/outer) gated nanotube *vs.* gate-all-around nanowire architecture for tunnel field effect transistor application. We show that nanotube topology can result in higher performance through higher normalized current when compared to nanowire architecture at $V_{dd} = 1$ V due to the availability of larger tunneling cross section and lower Shockley-Reed-Hall recombination. Both architectures are able to achieve sub 60 mV/dec performance for more than five orders of magnitude of drain current. This enables the nanotube configuration achieving performance same as the nanowire architecture even when V_{dd} is scaled down to 0.5 V. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4905423]

I. INTRODUCTION

Hetero-structure tunnel field effect transistors (TFETs) have recently been gaining attention for their potential to radically improve drive current, I_{ON}, as well as, achieving lower operation voltages, V_{dd}, by means of steep sub-threshold slope (SS) switching. This is due to the small carrier effective masses of low band gap source materials, which increase the tunneling probability, according to the triangular Wentzel–Kramer–Brillouin (WKB) approximation, and thus the device "ON" current enhances.[1,2] Potential source material candidates for N/P metal oxide semiconductor (MOS) TFETs are Germanium (Ge) and Indium Arsenide (InAs), respectively. Simulation studies using the above materials in a hetero-structure have shown I_{ON} values of 244 μA/μm and 83 μA/μm for Ge n-type TFET (NTFET) and InAs p-type TFET (PTFET), respectively, which corresponded to I_{ON} enhancements by factors of more than 400× and 100×, respectively, over their all-Si planar counterparts.[3] One potential window for getting the optimum performance is combining hetero-structure junctions with new and unique non-planar device architectures. The reason non-planar architectures are desirable is that the mechanism of tunneling in TFET devices can be seen from the inter-band tunneling probability across the tunneling barrier, which is typically calculated using WKB approximation[4]

$$T_{WKB} \approx \exp\left(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3q\hbar(E_g + \triangle\Phi)}\right), \quad (1)$$

where m* is the effective mass, E_g is the band gap, λ is the screening tunneling length, and $\triangle\Phi$ is the potential difference between the source valence band and channel conduction bands. From this simple triangular approximation, we can see that that the band gap (E_g), the effective carrier mass (m*), and the screening tunneling length (λ) should be minimized to increase the tunneling probability. The parameter λ is specifically sensitive to the device geometry, among other factors, such as doping profile and gate capacitance.[3] A small λ value would result in a strong modulation of the channel bands by the gate, and thus smaller barrier for tunneling. It has been shown that the highest tunneling rate and hence the lowest λ values were found for the gate-all-around (GAA) architecture, while ultra-thin body (UTB) double gate (DG) and single gate planar (SG) UTBs have shown higher λ values.[5] However, the theoretical study has also shown that when the transistor channel thickness is scaled down to less than or equal to 10 nm, the λ value of the DG architecture approaches that of the GAA around architecture, 3.8 nm *vs.* 2.4 nm for 10 nm body thickness. The λ values are even equal at body thickness of 2.5 nm.[5]

From device architecture perspective, we have recently shown the unique advantages of conventional channel material silicon (Si) based core/shell gated nanotube (NT) architecture for controlling the device channel over the GAA nanowire (NW) architecture. The nanotube architecture mimics the GAA NW devices by having an outer (shell) gate, as well as, an inner (core) gate inside the nanowire making it a hollow cylindrical structure. The new architecture has shown improved drive current capability compared to vertical nanowires for silicon (as homogeneous material system) over-the-barrier FETs at scaled down body thickness of $\leq$20 nm.[6,7] When compared to an array of nanowires, the nanotube architecture outperforms in terms of drive current capability, CV/I metric (i.e., intrinsic gate delay), power consumption, and area efficiency.[8]

In this paper, we analyze a hetero-structure Si/Ge n-type NT TFET device concept that combines the advantages of a low band-gap source injector and inherent high drive current advantage in NT FET, as shown in Fig. 1. With the above in mind, we hypothesize that the NT TFET's excellent electrostatic control would enable steep turn on characteristics, while maintaining low I_{OFF} values comparable to GAA NW TFET. This transistor architecture in conjunction with a low band gap source material in a hetero-structure configuration

a)Author to whom correspondence should be addressed. Electronic mail: muhammadmustafa.hussain@kaust.edu.sa

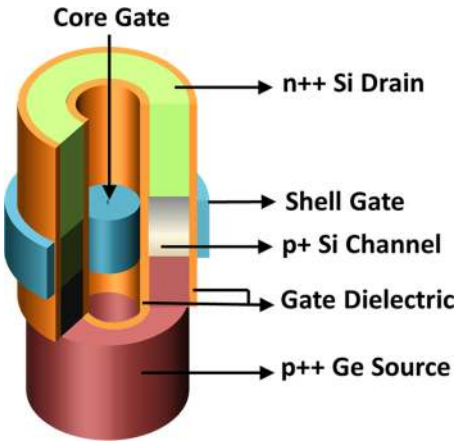

FIG. 1. Schematic of the nanotube heterostructure TFET.

would enable a higher inter-band tunneling rate, when compared to all-silicon TFET structure. For this reason, we have chosen Ge as a source material since it has approximately half the band gap as compared to that of Si (0.66 eV *vs.* 1.2 eV) and smaller effective mass (0.06 m_o *vs.* 0.2 m_o) too.[9] Ge also has a direct band gap at the L-point that is 0.14 eV larger than the indirect band gap at the Γ-point in the E-K diagram.[10] Moreover, theoretical studies show that under high gate electric field, direct tunneling dominates in Ge, as well as, in $Si_{1-x}Ge_x$ with high Ge mole fraction ($x \geq 0.8$) due to the slightly larger direct band gap in Ge.[10] Therefore, engineering the Si/Ge hetero-structure to include an overlap with the gate would potentially induce higher band-to-band tunneling (BTBT) rate due to vertical tunneling within the Ge source where electrons tunnel within the source region in the direction perpendicular to the semiconductor/gate-dielectric interface.[11] Vertical tunneling is more desirable as it allows for a controlled cross sectional area for tunneling controlled by the gate-to-source overlap, where electrons are injected from within the source area to the inverted surface region of the source (in the source-to-gate overlap region). On the other hand, lateral tunneling is limited by the inversion layer thickness of the source channel junction in the "ON" state of the transistor, and thus is limited by the junction's cross section.[11] Source-to-gate overlap could be engineered to achieve desired SS that would allow the scaling down of the supply voltage, V_{dd}. Hence, we have studied the Si/Ge hetero-structure TFET with an intentional gate-to-source overlap for two different supply voltages, namely, $V_{dd} = 0.5$ and 1 V for the GAA and the NT architectures for a fixed body thickness.

II. DEVICE STRUCTURE

To study the benefits of a nanotube architecture over a nanowire on a hetero-structure Si/Ge TFET platform, 3D simulations of a NT (Fig. 1) and GAA NW TFET using Synopsys™ have been carried out since it includes a variety of BTBT models to account for both direct and indirect tunneling processes.[12–14] Both devices are compared for a gate length (L_g) of 30 nm, with 5 nm gate-to-source overlap to induce vertical tunneling within the Ge source.[15] Silicon drain is n-doped with donor active concentration $N_D = 1 \times 10^{19}\,cm^{-3}$, while a p+ Si channel is used with acceptor active concentration $N_A = 1 \times 10^{18}\,cm^{-3}$. A p++ Ge source was used with acceptor active concentration $N_A = 1 \times 10^{19}\,cm^{-3}$, both typical to the already fabricated device used for extracting the "A" and "B" tunneling parameters.[15,16] Both the nanotube thickness and nanowire diameter are kept at 10 nm. The gate is n++ poly silicon in both devices and has a work function of 4.0 eV, and an oxide gate dielectric is assumed with an (effective oxide thickness) EOT of 1.5 nm. A dynamic nonlocal band-to-band (BTB) tunneling model is utilized in conjunction with Shockley–Reed–Hall (SRH) recombination, drift–diffusion physics, and Fermi statistics. The BTBT parameters, "A" and "B" for both Si and Ge are taken from experimentally derived and their values are found in both 17 and 15, respectively. For Ge, the experimentally derived "A" parameter is $1.46 \times 10^{17}\,cm^{-3}\ s^{-1}$ and the experimentally derived "B" parameter was 3.59 MV/cm. For Si, the "A" and "B" parameters are $4 \times 10^{14}\,cm^{-3}\ s^{-1}$, and 19 MV/cm, respectively, which are attributed to indirect(phonon-assisted) tunneling.[17] The experimentally derived values are calculated according to the Kane and Keldysh models for BTBT generation rate in the uniform electric-field limit[18]

$$G_{BTBT} = A\left(\frac{F}{F_o}\right)^P \exp\left(-\frac{B}{F}\right), \tag{2}$$

where F is the electric field, $F_o = 1$ V/cm, and $P = 2$ and 2.5 for the direct and indirect BTBT, respectively. The derived parameters for Ge/Si heterojunction TFET have been extracted from the transistor transfer curve, according to[15,16]

$$I_D = A\,E_s \exp\left(-\frac{B}{E_s}\right), \tag{3}$$

where E_s is the vertical electric field at the semiconductor (Ge) surface in the gate-to-source overlap region of the tunneling, Finally, it is important to note that the experimental data from which the tunneling parameters were extracted for a poly-Ge source that was selectively grown on Si (100) after etching silicon isotropically to induce a 10 nm recess under the gate for an intentional source-to-gate overlap, which is similar to our device structure.

III. RESULTS AND DISCUSSION

Fig. 2(a) compares the normalized transfer characteristics of 10 nm thin NT TFET (with 100 nm inner/core-gate diameter, CG_{dia}) and 10 nm diameter NW TFET at $V_{dd} = 1.0$ V. For normalization, we have used the NW circumference (πd_{NW}), where d_{NW} is the NW diameter, as the normalization length similar to various reports in the literature for vertical GAA NW TFET.[20,21] In the case of the NT, we have used average circumference ($\pi \times (CG_{dia} + NT_w)$), where CG_{dia} and NT_w are the nanotube core-gate diameter and thickness, respectively. This leads to a fair comparison since as we scale down the inner core gate diameter, CG_{dia}, to zero, the normalization length becomes ($\pi \times NT_w$), which is essentially the circumference of a NW with a diameter equal to the NT thickness, $d_{NW} = NT_w$. This is also consistent with previous reports in

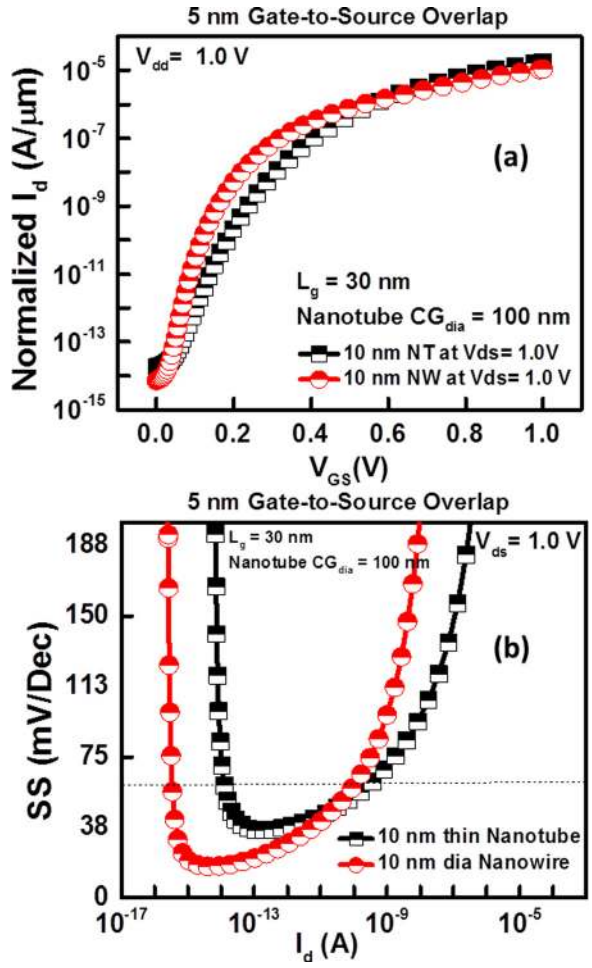

FIG. 2. (a) Comparison of the NT and NW transfer characteristics and (b) subthreshold slopes at $V_{dd} = 1$ V.

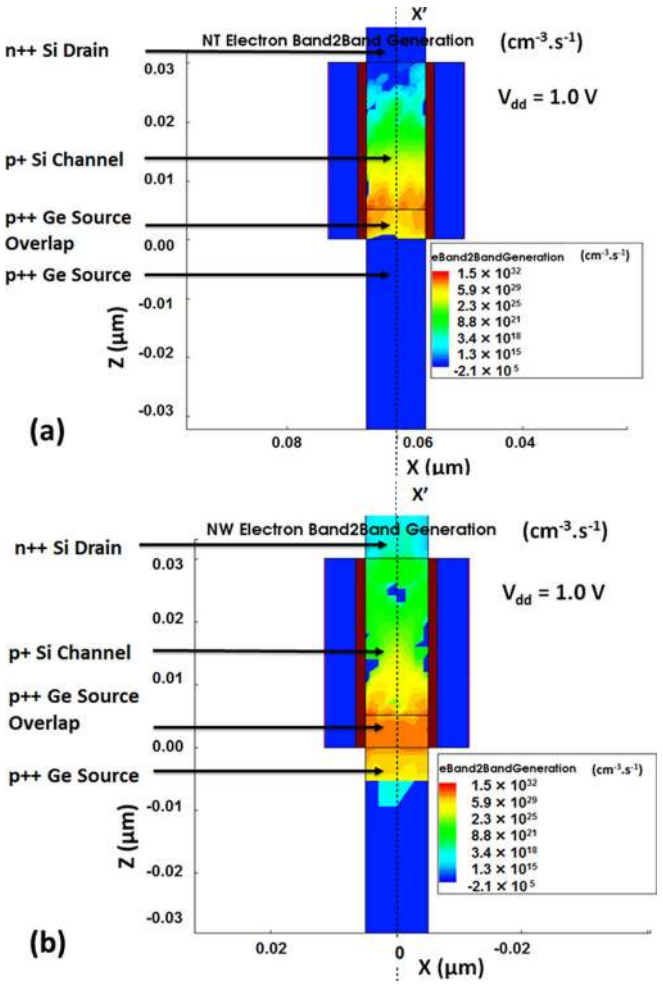

FIG. 3. Color maps showing BTB generation profiles for the (a) NT TEFT and the (b) NW TFET at $V_{dd} = 1$ V.

the literature, where SG, DG, and GAA architectures are compared at a body thickness, measured normal to the gate oxide, equal to the diameter of the NW, d_{NW}, to study the effect of device geometry on the BTBT rates and scanning tunneling length, λ.[5] The non-normalized drain current of the NT TFET, 6.1 μA is 18× times than that of the NW TFET, 0.34 μA, while the normalized drain current of the NT TFET, 18 μA/μm is 1.6× than that of the normalized NW-TFET drain current, 11 μA/μm. The SS values for both devices are shown in Fig. 2(b), where the lowest SS values are 17 mV/dec and 36 mV/dec for the NW and NT TFETs, respectively. Both architectures are able to sustain sub-60 mV/dec SS for about five orders of magnitude of drain current, which is an important requirement for the consideration of TFETs for practical applications.[3] The GAA NW TFET architecture, however, is able to provide lower point SS values as noted above which is due to the tighter electrostatic control and lower scaling tunneling length, λ, as expected from the WKB approximation when compared to the DG and SG architectures.[5] This should potentially lead to higher normalized drain current for the GAA NW TFET; however, in reality, this was not the case. Therefore, we investigated the electron band-to-band generation profile for both the NT and NW TFETs in Fig. 3(a), and Fig. 3(b), respectively, as shown in the color maps. The first thing we observed that vertical tunneling within the Ge source overlap region is more prominent for the NW TFET as expected from the theory due to the smaller λ, and tighter electrostatic control.[5] Hence, the BTB generation rate peaks within the Ge gate-to-source overlap region for the NW TFET. As for the NT TFET, although vertical tunneling is still noticed within the overlap region, BTB generation rate peaks on the Si side of the Si/Ge interface due to lateral tunneling. It is known that within the dynamic non-local BTB tunneling model, the direction of the tunneling path is determined dynamically from the negative gradient of the valence band at the starting position and carriers are generated non-locally at the end of the tunnel path, the conduction band, through both direct and indirect (phonon-assisted) tunneling paths.[18] The tunneling energy is equal to the valence band energy at the starting position and is equal to the conduction band energy plus band offset at the ending position.[18] Therefore, band diagrams were analyzed for the absolute value of the gradient of the hole quasi-Fermi level, $|\text{grad}(E_{qFp})|$ was analyzed along the X-X′ cross sections, lying in the middle of the channel with respect to the x coordinate for the NT and NW TFETs and was plotted Figs. 4(a) and 4(b), respectively. Results reveal two main peaks on both sides of the Si/Ge junction for both NT and NW TFETs. The NW TFET, however, shows a higher absolute

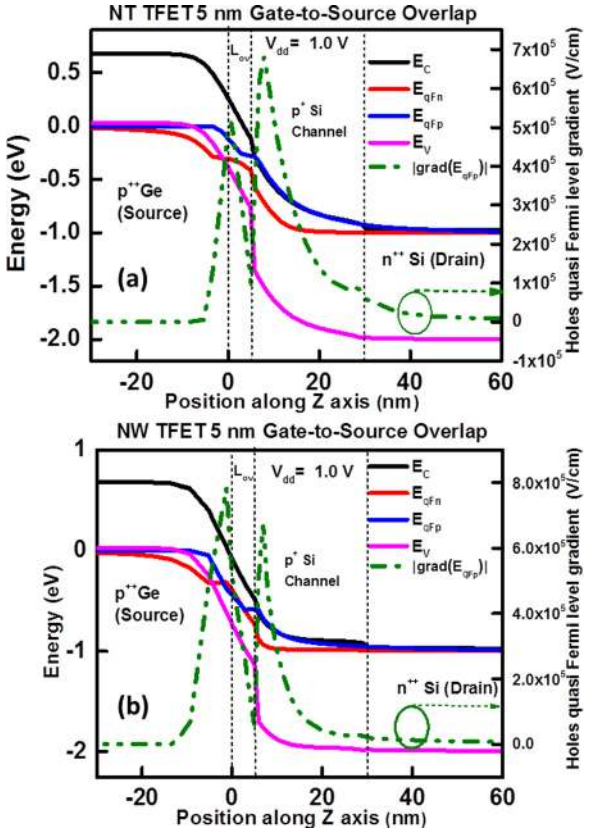

FIG. 4. Band diagram and the gradient of the holes quasi Fermi level, $|\text{grad}(E_{qFp})|$, for the cross sections X-X′ in Fig. 3 for the (a) NT TEFT and the (b) NW TFET at $V_{dd} = 1$ V.

value of the gradient of the hole quasi-Fermi level, $|\text{grad}(E_{qFp})| = 7.4 \times 10^5$(V/cm), within the Ge gate-to-source overlap region when compared to the similar peak for NT TFET, $|\text{grad}(E_{qFp})| = 5 \times 10^5$ (V/cm). The NW TFET also shows a peak within the Si channel, but it has a smaller magnitude, 6.5×10^5 (V/cm), and is less broad compared to the peak due to the peak within the gate-to-source overlap region. This confirms that the tunneling behavior in the NW TFET is mainly due to vertical tunneling with the overlap region, as it corresponded to the smallest tunneling distance, λ. On the other hand, the NT TFET also shows two peaks, with the highest peak on the Si side of the junction as its magnitude is equal to 6.8×10^5 V/cm. Also, the peak on the Si side of the junction is broader than the corresponding peak for the NW TFET. This confirms that lateral tunneling is the dominant tunneling process for the NT TFET, as it corresponds to the shortest λ for the NT TFET. This could explain why the NW TFET achieves lower SS when compared to the NT TEFT.

The electron BTB generation profile for the same cross sections was analyzed for both devices in Fig. 5. The peak for the NT TFET was on the silicon side of the Si/Ge interface, while it was the opposite for the NW TFET corresponding to the same trend for the $|\text{grad}(E_{qFp})|$. The NW TFET has also shown a broader peak compared to the NT TFET that lies largely within the Ge gate-to-source overlap area, with a peak value of 4.5×10^{30} (cm^{-3} s^{-1}), while the NT-TFET peak value is 2.3×10^{30} (cm^{-3} s^{-1}) which is still within the

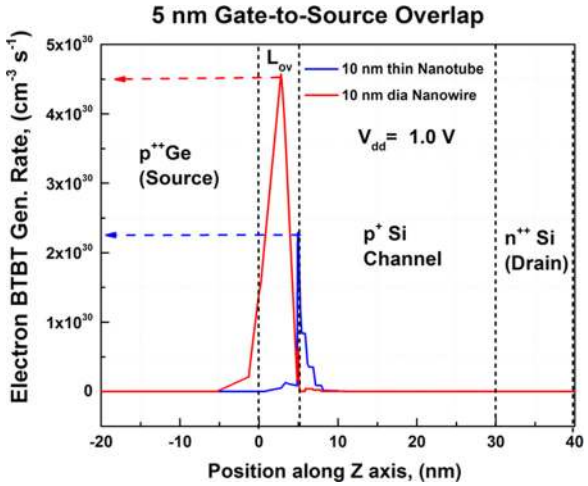

FIG. 5. BTB generation profile comparison across the cross sections X-X′ in Figure 3 for the NT and NW TFETs.

same order of magnitude as the NW TFET. Hence, this again shows that vertical tunneling is more prominent in the case of the NW TFET, while lateral tunneling dominates for the NT TFET, which should have led to a higher normalized current for the NW TFET. However, when analyzing the SRH recombination for both devices, an interesting difference between the two devices arose, as shown in Fig. 6. While the

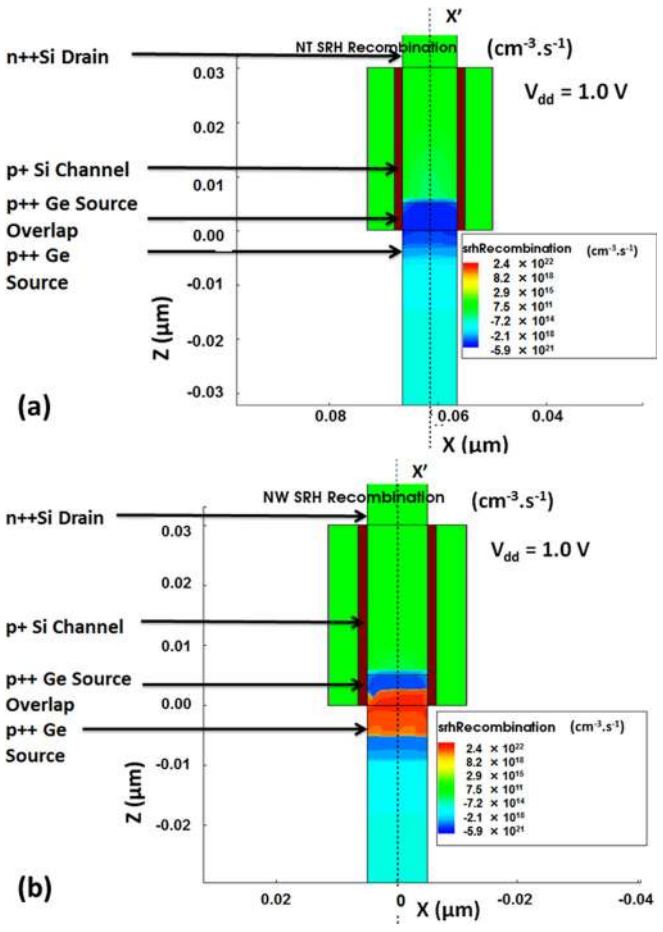

FIG. 6. Color maps showing SRH recombination profiles for the (a) NT TEFT and the (b) NW TFET at $V_{dd} = 1$ V.

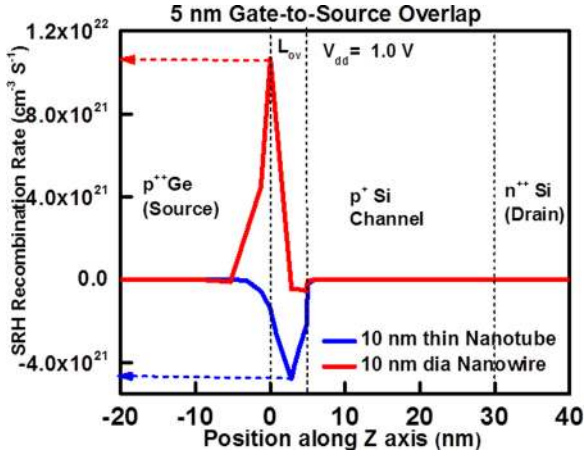

FIG. 7. SRH recombination profile comparison across the cross sections X-X′ in Figure 3 for the NT and NW TFETs.

NT TFET shows a SRH generation behavior, as shown in the color map in Fig. 6(a), the NW TFET has shown an opposite recombination behavior, especially within the overlap region. This could be explained based on the band diagram extracted for the cross sections X-X′ in Fig. 5, which shows overlap of the quasi Fermi levels of electrons and holes within the overlap region, which indicates higher carrier concentration of both electrons and holes within this region. This leads to a high recombination rate for the NW TFET when compared to the NT TFET, as the recombination rate is directly proportional to the product of the electron and holes carrier concentrations, $R_{SRH} \propto np$. The SRH recombination rate is plotted in Fig. 7, for the cross sections, X-X′, shown in Fig. 5. While the NT TFET shows a generation rate of $10^{22}\,cm^{-3}\,s^{-1}$, the NW TFET shows an opposite recombination rate of the order of $5 \times 10^{21}\,cm^{-3}\,s^{-1}$, as shown in Fig. 7. This could explain why a lower normalized current was achieved for the NW TFET when compared to the NT TFET. In addition, the larger cross-sectional area available for tunneling for the NT architecture, which is 44× that of the NW at a body thickness of 10 nm, is another reason for the higher normalized current for NT TFET when compared to NW TFET at $V_{dd} = 1\,V$, as indirect lateral tunneling is limited by the inversion region in the interface.

The performance of the NW and NT TFETs was also compared at $V_{dd} = 0.5\,V$. Fig. 8(a) shows the normalized transfer characteristics of the devices. The NT TFET is able provide higher non-normalized current, $I_{ON(NT)} = 0.134\,\mu A$, which is 5.5× the current provided by the NW TEFT, $I_{ON(NW)} = 0.0243\,\mu A$. However, the NW normalized current, $0.776\,\mu A/\mu m$ is 2× that of the NT TFET, $0.387\,\mu A/\mu m$. The SS values for both devices are shown in Fig. 8(b), where the lowest SS values are 17 mV/dec and 32 mV/dec, for the NW and NT-TFETs, respectively. To understand why GAA NW

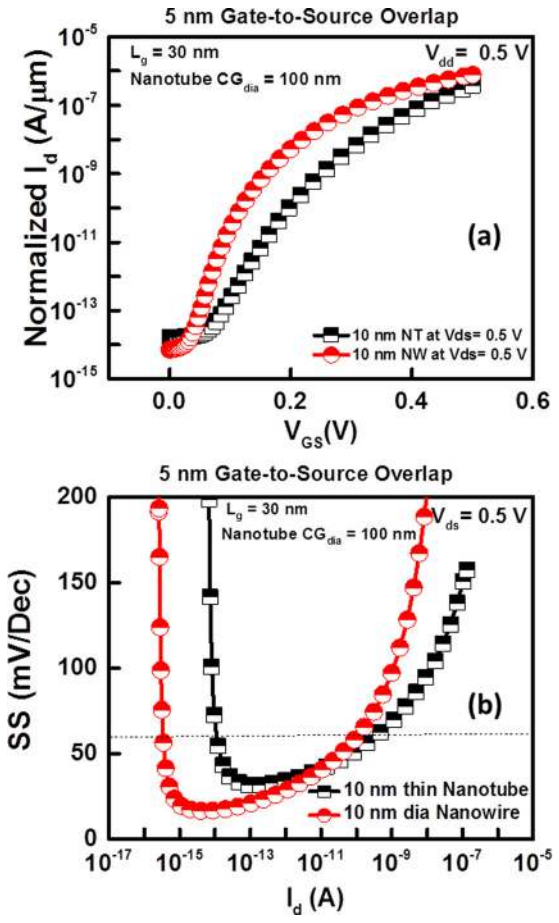

FIG. 8. (a) Comparison of the NT and NW transfer characteristics and (b) sub-threshold slopes at $V_{dd} = 0.5\,V$.

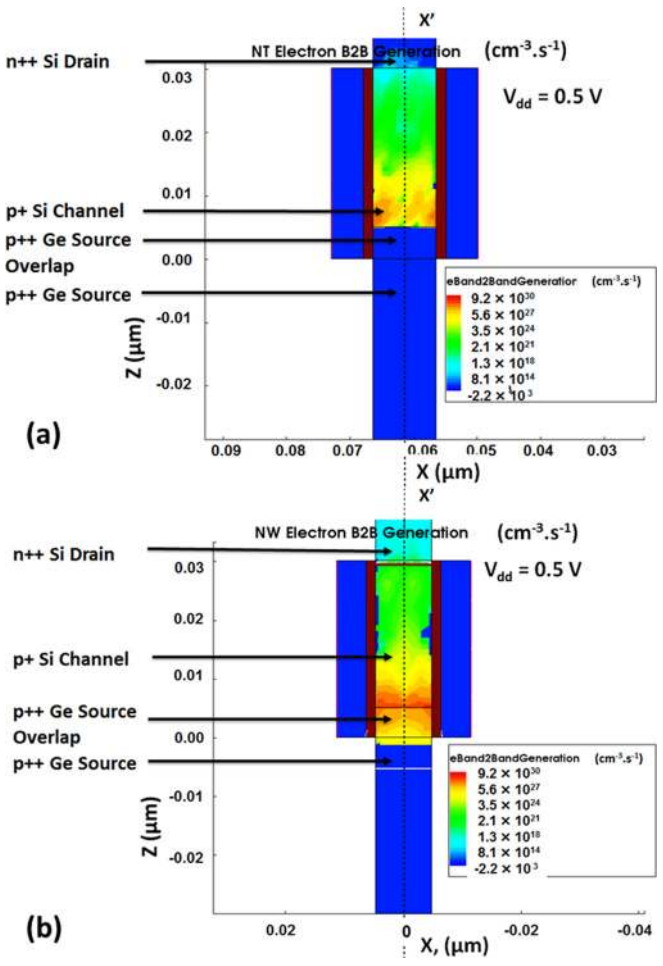

FIG. 9. Color maps showing BTB generation profiles for the (a) NT TEFT and the (b) NW TFET at $V_{dd} = 0.5\,V$.

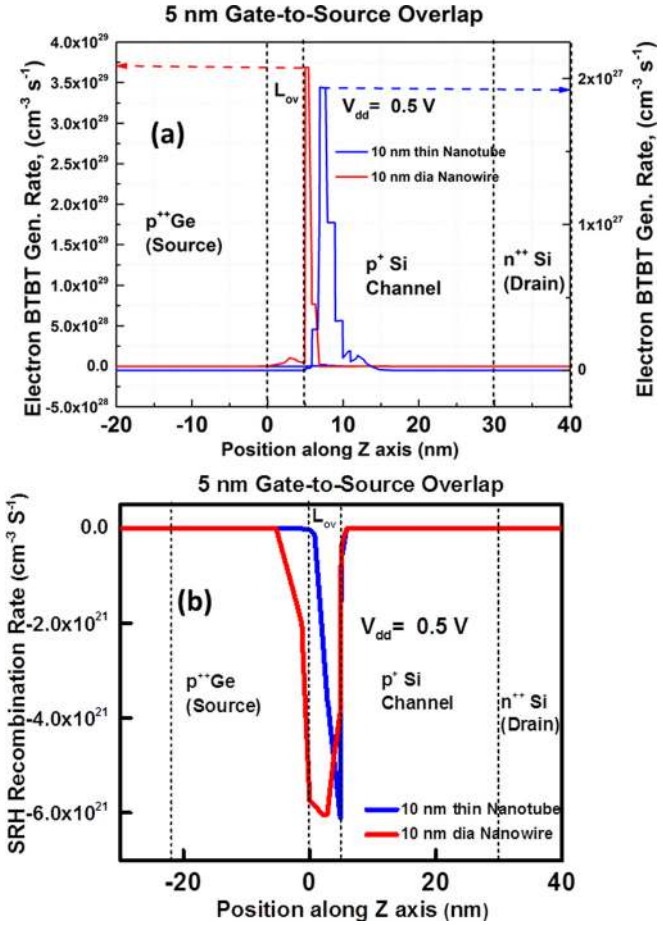

FIG. 10. (a) BTB generation profile and (b) SRH recombination profile comparison across the cross sections X-X′ in Fig. 9 for the NT and NW TFETs.

performed better, we analyzed BTB generation rate in a vertical slice of both devices, as shown in the color maps in Figs. 9(a) and 9(b). For the case of the NT TFET, BTB generation is only due to lateral tunneling from Ge Source to Si channel, which makes the BTB mainly confined into the Si channel area, as shown in Fig. 9(a). While for the NW TFET, vertical tunneling still occurs within the Ge source overlap area, as shown in Fig. 9(b). However, the BTB generation profile peaks inside the Si channel area due to lateral tunneling shown by the rate along the X cross-section in Fig. 10(a) showing a peak of $3.75 \times 10^{29}\,cm^{-3}\ s^{-1}$ for the NW while only a peak rate of $2 \times 10^{27}\,cm^{-3}\ s^{-1}$ for the NT, which is two orders of magnitude lower than that of the NW. Fig. 10(b) shows the SRH recombination profile for both devices, showing generation behavior for both architectures, with wider peak for the NW TFET showing higher generation over a larger slice of the overlap region. Band diagrams, Fig. S1, and color maps of the SRH recombination profile, Fig. S2, for both devices are provided in supplementary materials.[19] This shows why NW outperforms the NT architecture at $V_{dd} = 0.5$ V, since it allows for a higher tunneling rate due to smaller λ value. However, when considering the larger non-normalized current provided by the NT, it makes the architecture more appealing, as it can eliminate the need for high density arraying of NWs, which makes the NT architecture more appealing from fabrication point of view.

Therefore, although the GAA NW architecture is more promising as it could achieve the steepest SS value as can be shown from literature review in Table I, it does not offer an appealing normalized "ON" current, when compared to single gated and double gated architectures. Recent demonstrations of sub-60 mV/dec of have been for all silicon single NW p and n-type TFET of diameter <20 nm which supplies

TABLE I. Summary of state-of-the-art of both homo-junction and hetero-junction TFET demonstration.

References	Technology	Channel material	SS (mV/dec)	I_{on} (A) per nanowire	Ion (μA/μm)	V_{ds} (V)	I_{on}/I_{off}
27[a]	GAA Si NW	Si	120	Not reported	0.1	−0.5	10^6
28[a]	Planar	Si	46	NA	1.2	−1	$\sim 10^8$
29[a]	Planar	Si	120 ∼ 250	NA	84	0.7	$>10^5$
	Planar	Si	120 ∼ 250	NA	109	1	$>10^4$
16[a]	Planar (Ge Source)	Si	40	NA	0.42	0.5	$>10^6$
26[a]	Planar	Ge	50 ∼ 60	NA	10	1	10^7
	Planar	Si	460	NA	∼0.001	1	$>10^2$
30[a]	Planar	Ge	>400	NA	4	0.8	$>10^2$
	Planar	Si	42 ∼ 200	NA	0.04	0.8	10^6
25[a]	Planar	Si	52.8	NA	12	1	10^5
31[a]	Planar	Si	285	NA	0.1	1.5	10^5
32[a]	InAs/Si GAA NW	Si	220	10^{-7}	0.4	1	10^5
13[a]	InAs/Si GAA NW	Si	150	Not reported	2.4	−0.5	10^6
20[a]	Vertical NW	p Si	30	8×10^{-7}	1.2	−2	10^5
21[a]	Vertical GAA NW	i-Si	30–50	1.5×10^{-9}	0.031	2	10^5
33[a]	Lateral GAA NW array	i-Si	30 for $I_{on} = 0.01\ \mu A/\mu m$	NA	64	1.5	10^6
24[a]	InAs/Si vertical NW	InAs	21	Not reported	1	1	$>10^6$
7	Vertical Si NT	i-Si	20	NA	3×10^{-2}	1	$>10^6$
This work	Si/Ge vertical NT (Ge source)	p+ Si	34	NA	18	1	$>10^6$
This work	Si/Ge GAA NW	p+ Si	17	0.34×10^{-6}	11	1	$>10^6$

[a]Asterisk denotes experimental work.

a maximum ON current in the nA regime and a normalized "ON" current of 1.2 $\mu A/\mu m$.[20,21] This is the case for the following reasons. Firstly, the requirement for small diameter NW, typically less than 20 nm for achieving steep SS, limits the current generated per NW due to small cross sectional area available for tunneling. Secondly, both the normalized "ON" current and SS degrade when NWs are arrayed due to sensitivity of parameters like threshold voltage to, for example, variations in NW width, dielectric thickness, and effective gate length, which could lead to degradation of the SS swing for a large array of devices, especially when considering highly doped source and drain junctions.[22,23] Thirdly and most importantly, the state-of-the-art pitch for vertical NW does not offer high current per unit chip area, as has been shown in the recent demonstrations showing NW pitch in the order of 400 nm for both top down[23] and bottom up approaches.[24] On the other hand, $I_{ON} = 100 \mu A/\mu m$ at $V_{DD} = 1.0$ V and $V_{GS} = 1$ V for all-silicon single gated SOI based TFETs with vertical self-aligned top gate structure supplying and for 70 nm thick SOI with 2 nm effective oxide thickness.[25] Even higher drain currents have been shown for double gate strained-Ge hetero-structure TFET with a drive current of 300 $\mu A/\mu m$ at a SS of 50 mV/dec.[26] That is why we think the NT architecture could be an excellent candidate for as a vertical structure that resembles double gate structure and could provide a higher integration density compared to the NW structure.

IV. CONCLUSION

In conclusion, we show that the NT architecture TFET is able to leverage the advantages of the GAA architecture NW TFET while enabling larger non-normalized drive currents due to the larger available tunneling area. Band diagrams revealed that at $V_{dd} = 1$ V, the NT architecture provide band-to-band generation rate of the same order of magnitude as the GAA NW architecture, while showing lower SRH recombination rate. This leads to higher current per unit chip area and thus enables scaling down of the TFET size without compromising performance. When V_{dd} was scaled down to 0.5 V, the NT architecture is still able to provide comparable normalized current to the GAA NW, while enabling larger non-normalized current due to larger cross-sectional area available for tunneling, thus eliminating the need for arraying, and avoiding the variability issue.

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