ELectronics EXpress

IEICE Electronics Express, Vol.1, No.1, 19–23

SIASCA: Interactive System for the Symbolic Analysis of Analog Circuits

Esteban Tlelo-Cuautle,[a] **A. Quintanar-Ramos, G. Gutiérrez-Pérez, and M. González de la Rosa**

INAOE, Luis Enrique Erro No. 1, Tonantzintla, Puebla, 72000 MEXICO

Instituto Tecnológico de Puebla.

a) *etlelo@m.ieice.org*

Abstract: To improve analog design automation (ADA) of electronic circuits, an interactive system for symbolic analysis called SIASCA is introduced. SIASCA includes schematic capture of a more general class of analog circuits, namely: operational transconductance amplifiers and current conveyors. The options of analysis are focused on calculating simplified symbolic expressions (SEs), representing the dominant behavior of a circuit, for AC and noise analysis. To minimize complexity in manipulating SEs, all active devices are modeled at different levels of abstraction by using nullors. Several examples demonstrate the suitability and usefulness of SIASCA to be used within ADA environments.

Keywords: symbolic analysis, circuit simulators, frequency response, nullor

Classification: Microwave and millimeter wave devices, circuits, and systems

References

[1] G. G. E. Gielen, H. C. C. Walscharts, W. M. C. Sansen, "ISAAC: a symbolic simulator for analog integrated circuits," *Solid-State Circ., IEEE J.*, vol. 24, no. 6, pp. 1587–1597, 1989.

[2] Rob A. Rutenbar, G. G. E. Gielen, and Brian A. Antao, *Computer-Aided Design of Analog Integrated Circuits and Systems*, IEEE Press, 2002.

[3] www.tina.com

[4] www.analog-insydes.de

[5] F. V. Fernández, A. Rodriguez-Vázquez, J. L. Huertas, and G. G. E. Gielen, *Symbolic Analysis Techniques*, IEEE Press, New York, 1998.

[6] C. Toumazou, B. Gilbert, and G. S. Moschytz, *Trade-Offs in Analog Circuit Design*, Kluwer Academic, 2003.

[7] E. Tlelo-Cuautle, C. Sánchez-López, and F. Sandoval-Ibarra, "Symbolic analysis: a formulation approach by manipulating data structures," *IEEE ISCAS*, vol. IV, pp. 640–643, 2003.

[8] J. Aguila-Meza, L. Torres-Papaqui, and E. Tlelo-Cuautle, "Improving symbolic analysis in CMOS analog ICs," *IEEE ISCAS*, Vancouver, May 2004.

[9] C. Sánchez-López and E. Tlelo-Cuautle, "Symbolic noise analysis in analog integrated circuits," *IEEE ISCAS*, Vancouver, May 2004.

© IEICE 2004

DOI: 10.1587/elex.1.19
Received February 07, 2004
Accepted February 23, 2004
Published April 10, 2004

IEICE Electronics Express, Vol.1, No.1, 19–23

1 Introduction

Symbolic analysis is focused on the calculation of simplified symbolic expressions (SEs) [1]-[5], which represent the dominant behavior of an analog circuit. The calculated SEs help the designer to gain insight about the behavior of the circuit. Furthermore, it is very much needed that the calculation of SEs be guided towards an interactive design process by generating analytical design equations, useful for synthesis and optimization procedures [2],[6]. Although nowadays there exist several commercially available symbolic simulators [3],[4], their applications are limited by the size of the circuit, the modeling approaches and mainly by the active devices that they have included in their libraries. Henceforth, this paper is focused on the development of an interactive system called SIASCA, which includes a more general class of active devices, namely [6]: operational transconductance amplifiers (OTAs) and current conveyors (CCII-). SIASCA enhances the capability of symbolic analysis to large-sized analog circuits by using nullors to model the behavior of all active devices at different levels of abstraction [7]-[9].

The structure of SIASCA is described in section 2. The method implemented in the stage of symbolic analysis is summarized in section 3. Several examples are given in section 4. Finally, the conclusion is given in section 5.

2 Structure of SIASCA

The graphical user interface (GUI) of SIASCA has been developed using Visual Java++, and the stage of analysis has been implemented using MAPLE^{TM}. The GUI is shown in Fig. 1, as one sees it includes a more general class of active devices, namely [6]: operational amplifier, OTA, CCII-, bipolar junction transistor and MOSFET.

The schematic capture procedure is executed by selecting objects from the Tools Gallery option. The movement of an object is done on a grid which is coordinated to identify the placement of each object. The basic set of circuits, such as: controlled sources, independent voltage and current sources, resistor, capacitor and inductor can be selected from the Elements button. The schematic of the analog ground appears by default at the beginning of a new Project, in order to set the reference node (0), as it is usually done by any circuit simulator alike SPICE. All objects can be joined by wiring their terminals using the wire object from the option Others in the Tools Gallery. For a wired circuit, an electrical rule checker (ERC) procedure is activated from the Analysis option, in order to generate the net-list of the schematic captured circuit. The net-list can now be used within the stage of analysis.

3 Stage of analysis

The behavior of all active devices is modeled by using nullors [7]-[9], in order to apply a unified analysis approach to circuits which contains only: nullators, norators, admittances, and independent current sources. In this manner, for a nullor circuit, the computation of a SE is reduced to the manipulation of the

© IEICE 2004
DOI: 10.1587/elex.1.19
Received February 07, 2004
Accepted February 23, 2004
Published April 10, 2004

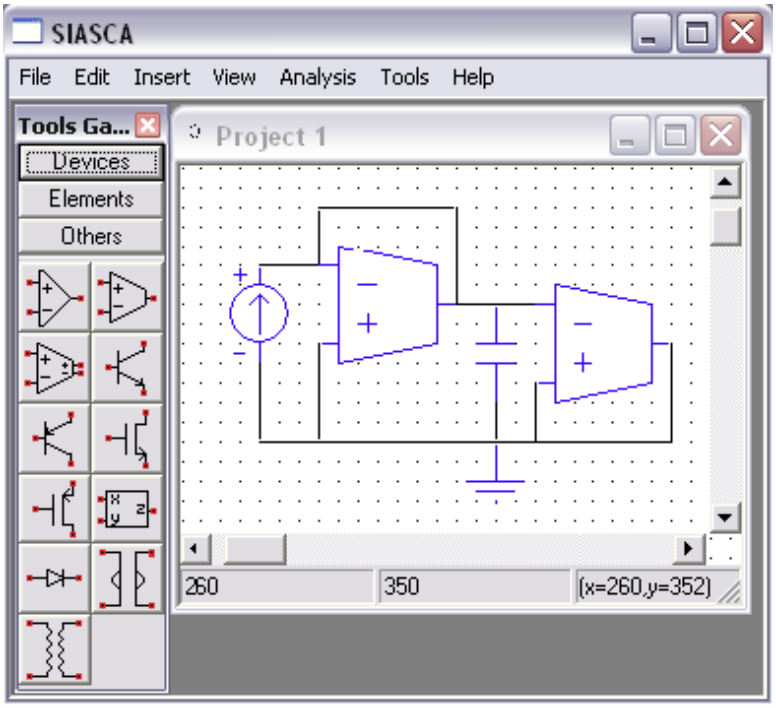

Fig. 1. The schematic capture environment of SIASCA

norator and nullator interconnection relationships (IRs), from which a compacted system of equations (CSEs) is formulated and solved. In short, from the net-list of a nullor equivalent circuit, the stage of analysis implemented in SIASCA can be summarized as follows [7]:

1. Calculation of IRs of norators and nullators.
2. Calculation of IRs of admittances by considering that for each pair of nodes i,j: the admittance is positive for i=j, else it is negative.
3. Apply compacted nodal analysis (CNA) to formulate a CSEs given by i_{CNA}=$Y_{CNA}v_{CNA}$, where:
   (a) Vector i_{CNA} is calculated by considering IRs of norators, and by including all nodes.
   (b) Vector v_{CNA} is calculated by considering IRs of nullators, and by including all nodes.
   (c) Matrix Y_{CNA} of order (m) equal to the number of nodes (n) minus the number of nullors (N), is calculated by considering IRs of admittances, which are associated to the pair of indexes (Row,Col) from the cartesian product among indexes of i_{CNA} and v_{CNA}.
4. The solution to the CSEs is done by applying Cramer's rule.
5. The final symbolic transfer function (TF), is simplified by comparing the relative magnitudes among symbols.

© IEICE 2004
DOI: 10.1587/elex.1.19
Received February 07, 2004
Accepted February 23, 2004
Published April 10, 2004

It is worth to mention that to eliminate non-dominant symbolic terms before the formulation of a CSEs, SIASCA selects the appropriate model to each active device, by considering their biasing and frequency operating conditions by applying heuristic reasoning rules [8]. Furthermore, noise analysis is performed by applying CNA to nullor circuits whose noise sources are added according to the noise models of each active device [2],[9].

4 Examples

Lets consider the low-pass gm-C filter working in current mode and shown in Fig. 1. SIASCA transforms that circuit into the nullor equivalent one shown in Fig. 2 [7]. To calculate the symbolic TF, the analysis stage performs the following calculations:

1. IRs of norators are (2,1), (3,4), (5,0) and (6,0). IRs of nullators are (1,2), (1,3), (5,0) and (6,0).

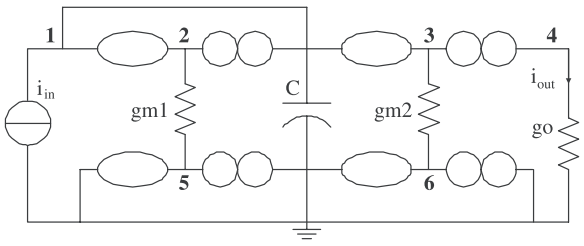

Fig. 2. Nullor equivalent circuit of Fig. 1

2. IRs of admittances: g_{m1} for (2,2) or (5,5), -g_{m1} for (2,5) or (5,2), g_{m2} for (3,3) or (6,6), -g_{m2} for (3,6) or (6,3), g_0 for (4,4), sC for (1,1).

3. By applying CNA to formulate a CSEs of order m=6-4=2:
   i_{CNA}=$[(1,2),(3,4)]^t$.
   v_{CNA}=$[(1,2,3),(4)]^t$.
   The cartesian product among i_{CNA} and v_{CNA} generates:
   Y_{11}=(1,1)+(1,2)+(1,3)+(2,1)+(2,2)+(2,3), Y_{12}=(1,4)+(2,4),
   Y_{21}=(3,1)+(3,2)+(3,3)+(4,1)+(4,2)+(4,3), Y_{22}=(3,4)+(4,4)
   By searching the admittance value of each pair (R,C) in the IRs of admittances to fill Y_{CNA}, the CSEs is given by:

$$\begin{bmatrix} i_{in} \\ 0 \end{bmatrix} = \begin{bmatrix} sC+g_{m1} & 0 \\ g_{m2} & g_o \end{bmatrix} \begin{bmatrix} v_{1,2,3} \\ v_4 \end{bmatrix}, \tag{1}$$

4. Since i_{out}=$g_o v_4$, the solution to (1) for v_4 is given by:

$$v_4 = \frac{-g_{m2} i_{in}}{(sC+g_{m1})g_o} \tag{2}$$

5. Finally, the symbolic TF is given by:

$$\frac{i_{out}}{i_{in}} = \frac{-g_{m2}}{sC+g_{m1}} \tag{3}$$

© IEICE 2004
DOI: 10.1587/elex.1.19
Received February 07, 2004
Accepted February 23, 2004
Published April 10, 2004

For transistor circuits [8], lets consider the schematic capture of the common source amplifier shown in Fig. 3. By executing the Analysis option, the symbolic TF calculated by SIASCA for low frequency is given by:

$$\frac{v_{out}}{v_{in}} = -g_m R \tag{4}$$

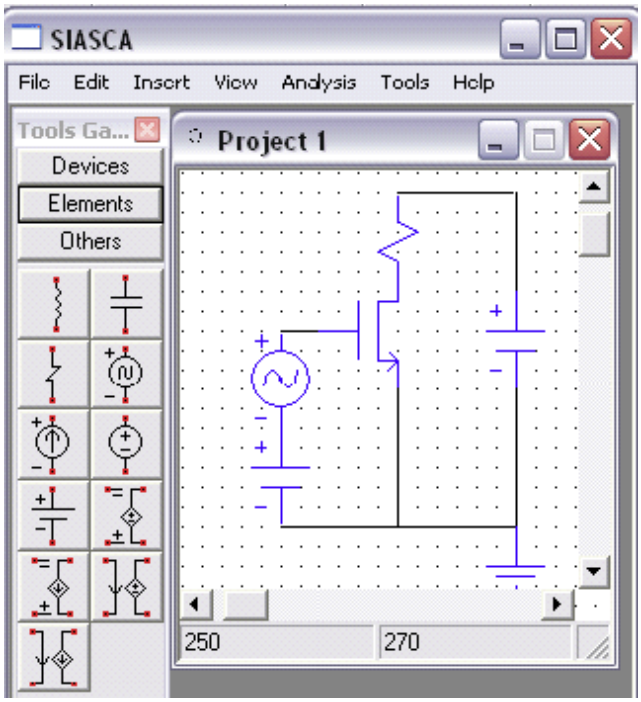

Fig. 3. Common source amplifier

A suitable symbolic noise analysis can be also carried out for analog integrated circuits working in either voltage or current mode [9].

5 Conclusion

It has been described the manner in which the interactive system called SIASCA, calculates simplified SEs of analog circuits whose behavior is modeled at different levels of abstraction by using nullors. The analysis stage improves symbolic analysis by formulating a CSEs through manipulating the IRs of norators, nullators and admittances. The simplification procedures implemented in SIASCA consist on comparing the relative magnitudes among symbols and on selecting an appropriate model to each active device before formulating the CSEs. From the examples given above, it has been demonstrated the suitability of SIASCA to be used within analog design automation environments or for experts analog designers to automate the calculation of simplified SEs useful for synthesis or optimization procedures.

Acknowledgments

This work is supported by CONACYT/MEXICO under project J40321, and CoSNET/MEXICO under project 454.03.

© IEICE 2004
DOI: 10.1587/elex.1.19
Received February 07, 2004
Accepted February 23, 2004
Published April 10, 2004