

SiC and GaN Devices With Cryogenic Cooling

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ABSTRACT This article presents the cryogenically cooled application for wide bandgap (WBG) semiconductor devices. Characteristics of silicon carbide (SiC) and gallium nitride (GaN) at cryogenic temperatures are illustrated. SiC MOSFETs exhibit increased on-state resistance and slower switching speed at cryogenic temperatures. However, cryogenic cooling provides low ambient temperature environment and thus enables the SiC converter to operate at lower junction temperature to achieve higher efficiency compared to room temperature cooling. A cryogenically cooled MW-level SiC inverter prototype is developed and demonstrated the feasibility of operating high-power SiC converter with cryogenic cooling. GaN HEMTs exhibit more than five times on-state resistance reduction and faster switching speed at cryogenic temperatures which makes GaN HEMTs an excellent candidate for cryogenic power electronics applications. The significantly reduced on-state resistance of GaN devices provides the possibility to operate them at a current level much higher than rated current at cryogenic temperatures. A GaN double pulse test (DPT) circuit is constructed and demonstrated that GaN HEMTs can operate at nearly four times of rated current at cryogenic temperatures. Challenges of utilizing WBG device with cryogenic cooling are discussed and summarized.

INDEX TERMS Wide bandgap device, SiC MOSFET, GaN HEMT, cryogenic temperature, cryogenically-cooled converter, device characterization, MW-level converter.

I. INTRODUCTION

WBG semiconductor devices, including SiC and GaN, are attracting increasing attention due to their low specific on-state resistance, high-speed switching and high breakdown voltage. WBG based power converters exhibit significantly improved performance (e.g., higher efficiency, higher power density, and higher reliability) compared to converters using the established silicon (Si) devices.

This article presents the cryogenically cooled applications for WBG semiconductor devices. Cryogenic temperatures usually refer to temperatures below 123 K. This low temperature is usually generated by liquid nitrogen, liquid helium, liquid hydrogen, or liquefied natural gas in industry applications.

The motivation of utilizing cryogenic cooling for power electronics can be summarized from two aspects. First, in some applications such as electric aircraft propulsion systems or other superconducting machine systems where cryogenic cooling is provided, it would be beneficial to the system if the power electronics can be integrated into the cryogenic cooled system. Otherwise, power electronics will be placed inside

thermal insulation containers to maintain room temperature operation which increases system complexity, cost, size and weight. Second, cryogenic cooling may also benefit general power electronics applications because it offers numerous benefits, including 1) several power semiconductor devices, such as Si and GaN, have improved performance at low temperature, with decreased specific on-state resistance and increased switching speed; 2) power semiconductor devices can be operated at higher switching frequencies and thus reducing the weight and size of passive components at cryogenic temperature; 3) less cooling requirement due to low ambient temperature provided by cryogenic cooling; 4) light and/or efficient conductors such as busbar and inductor winding components due to low resistivity of copper/aluminum at low temperature.

For power devices, the Si-based devices characteristics at cryogenic temperatures have been studied in literature [1]–[10]. Si PN diodes show increased knee voltage at low temperature because of the drop in intrinsic carrier concentration. The on-state resistance decreases as temperature

decreases due to the increase of carrier mobility. However, when the temperature further decreases (<100 K), the on-state resistance will increase because of impact from carrier freeze-out [4]. The breakdown voltage declines at low temperature as the mean free path of the carrier increases and higher impact ionization. Similarly, Si MOSFETs show significantly reduced on-state resistances from room temperature to around 100 K as the increased carrier mobility. On-state resistance starts to increase as temperature further decreases because of carrier freeze-out. The threshold voltage increases at low temperatures due to the reduction of intrinsic carrier concentration. The breakdown voltage of Si MOSFETs also decreases as temperature declines due to the mean free path of carrier increases and higher impact ionization. The transconductance increases as temperature drops due to the increased inversion layer mobility. Hence, Si MOSFETs show faster switching speed at low temperature. Si IGBTs show reduced turn-off time at cryogenic temperatures. The static characteristics of Si IGBT is like that of Si MOSFET at low temperatures.

Recently, WBG semiconductor devices characteristics have been investigated at cryogenic temperatures [10]–[18]. Different from Si, SiC MOSFETs show degraded performance with increased on-state resistance at very low temperatures. The on-state resistance of SiC MOSFETs consists of channel resistance R_{ch} and residual resistance R_s . Residual resistance R_s includes drift region, JFET, substrate and contact resistances, and is much higher than channel resistance R_{ch} at high temperatures. R_s decreases as temperature decreases due to high carrier mobility like Si MOSFET. However, R_{ch} has a negative coefficient and becomes dominant at low temperatures and thus the total on-state resistance increases. This is also caused by the increase of the interface state density, since large number of electrons are trapped, and few free electrons are available for conduction of the inversion layer. Freeze-out is also a contributor to the increase of on-state resistance. The threshold voltage increases as temperature declines. The breakdown voltage of SiC MOSFET remains relatively constant when temperature decreases because the impact ionization efficiency does not increase. The switching performance of SiC MOSFET also becomes worse at cryogenic temperatures.

GaN HEMTs show quite different characteristics from MOSFETs at cryogenic temperatures due to their unique structure. The on-state resistance keeps decreasing as temperature drops. The total series resistance of GaN HEMT mainly consists of the drain and source electrodes contact resistances R_c , source to gate resistance R_{SG} and gate to drain resistance R_{GD} which are determined by the two-dimension electron gas (2DEG) sheet resistance, and the channel resistance R_{ch} under the gate region. R_{ch} is usually the dominant part and decreases with the channel mobility increase. The electron mobility keeps increasing until the temperature reduces to around 40 K due to the weak influence of Coulomb scattering. There is no carrier freeze-out in GaN HEMTs. The breakdown mechanism of GaN HEMTs is different from

that of MOSFETs and is more complicated due to their lateral structure. Several mechanisms can contribute to the breakdown of GaN HEMTs including source to drain punch-through, leakage through gate Schottky junction, vertical leakage of substrate, and impact ionization between source and drain. Recent study shows that GaN HEMTs have relatively constant breakdown voltage in a wide temperature range when temperature decreases [15]. The threshold voltage of normally off p-GaN HEMTs should decrease as temperature decreases due to the decreases of acceptor ionization. This matches the test results of GaN Systems devices [15] [51]. However, the threshold voltage of GaN FETs from EPC increases as temperature decreases as reported in [14]. The authors hypothesize that the increment is attributed to a change in the population of the 2DEG beneath the gate as temperature decreases. The gate injection transistors (GITs) from Panasonic and Infineon present a quite constant but slowly increasing threshold voltage as temperature decreases [51]. The cascode GaN devices from Transphorm shows a large increase of the threshold voltage at low temperatures, which is consistent with the behavior of Si devices. The transconductance of GaN HEMTs increases as temperature decreases due to the increase of electron mobility.

For power converters, there are several reports on converters using cryogenic cooling [19]–[25]. The reported maximum power of cryogenically cooled Si-based converter was a 40 kW three-level inverter [23]. The Si MOSFET based inverter design with special considerations of cryogenic temperature was illustrated. For WBG device based converters, the reported maximum power cryogenically cooled GaN-based converter is a 1 kW GaN HEMT based three-level flying capacitor inverter [24]. Loss analysis of the GaN inverter operating at cryogenic temperature was conducted. A 1 MW cryogenically cooled SiC power module based three-level inverter for electric aircraft propulsion applications is presented by the authors [25].

This article first compares the characteristics of the state-of-art WBG devices at cryogenic temperatures. Then, a high power (MW-level) SiC based converter using cryogenic cooling is demonstrated. Next, as the significantly reduced on-resistance of GaN at cryogenic temperature provides the possibility to operate GaN at a current level much higher than rated, the GaN HEMT high current operation with cryogenic cooling is investigated. Finally, challenges of using SiC and GaN with cryogenic cooling are discussed. These topics have rarely been discussed in previous literature.

The organization of this article is as follows. Section II presents the characteristics comparison of the state-of-art WBG devices at cryogenic temperatures. Section III presents a MW-level SiC inverter with cryogenic cooling. Section IV demonstrates the high current operation of GaN HEMT with cryogenic cooling. Section V discusses challenges of using SiC and GaN devices with cryogenic cooling. The conclusions are made in Section VI.

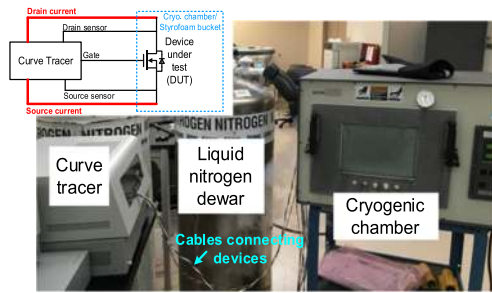


FIGURE 1. Test setup of static characterization at cryogenic temperatures.

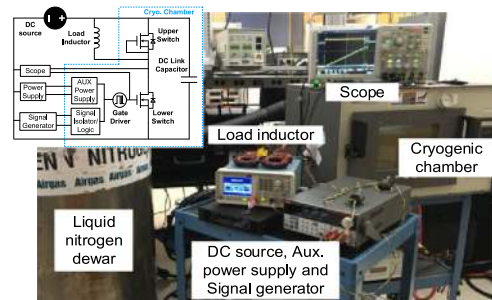


FIGURE 2. Test setup of dynamic characterization at cryogenic temperatures.

II. CHARACTERISTICS OF SiC AND GAN AT CRYOGENIC TEMPERATURES

A. DEVICE CHARACTERIZATION AT CRYOGENIC TEMPERATURES

To perform power device characterization at cryogenic temperatures, a cryogenic temperature chamber with liquid nitrogen is usually utilized in the lab. The temperature inside the chamber can be regulated from room temperature to cryogenic temperature as low as 93 K, and thermal insulation is achieved inside and outside of the chamber. Fig. 1 shows the static characterization test setup. The curve tracer B1505A from Keysight is connected with the DUT to test the output and transfer characteristics. The Kelvin connection need to be adopted to suppress measurement error introduced by long connected cables. Fig. 2 shows the dynamic characterization test setup. The DPT circuit is used for switching characteristics test of the devices. The PCB boards including DUT, gate driver, signal isolator, and auxiliary power supply are put inside the cryogenic chamber while the load inductor and other equipment are located outside. The method details for static and dynamic characterization at cryogenic temperatures can be found in [6].

B. SUMMARY OF SiC AND GAN DEVICES CHARACTERISTICS AT CRYOGENIC TEMPERATURES

With device characterization setup illustrated above, state-of-art SiC MOSFETs and GaN HEMTs in the 600 V~1.2 kV and tens of Amps range are characterized. The investigated devices are listed in Table 1.

TABLE 1. Investigated state-of-art SiC, GaN, and Si devices

Index	Producer	Name	Voltage/Current
T1	Wolfspeed	C3M0075120K (SiC)	1200V/30A
T2	Rohm	SCT3030KL(SiC)	1200V/72A
T3	ST	SCT50N120(SiC)	1200V/65A
T4	GaN Systems	GS66516T(GaN)	650V/60A
T5	Infineon	IPZ60R040 C7(Si)	600V/50A
T6	Infineon	IPW90R120 C3(Si)	900V/35A

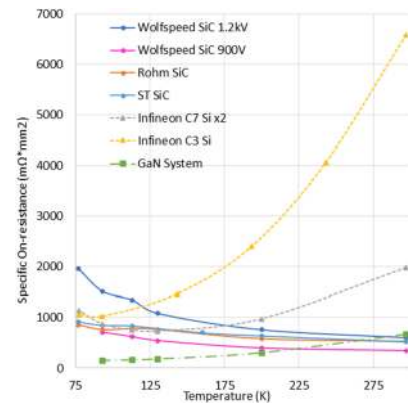


FIGURE 3. Specific on-state resistance versus temperature for SiC, GaN and Si devices.

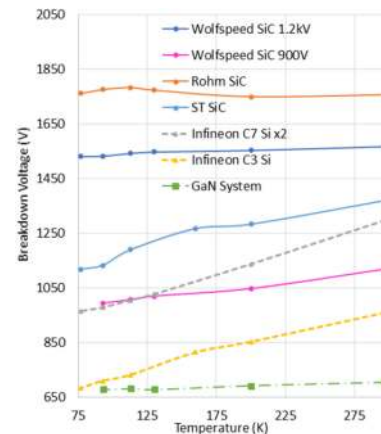


FIGURE 4. Breakdown voltage versus temperature for SiC, GaN and Si devices.

Fig. 3 shows the specific on-state resistance comparison of the selected devices. Both Si MOSFET and GaN HEMT show significantly reduced specific on-state resistance at cryogenic temperatures. At very low temperature (< 100 K), the specific on-state-resistance of Si MOSFETs begin to increase due to carrier freeze out but that of GaN HEMT keeps decreasing. Meanwhile, all SiC MOSFETs show significantly increased specific on-state resistances at cryogenic temperatures. The GaN HEMT has the lowest specific on-state resistance at cryogenic temperatures and achieved $>5X$ on-state resistance reduction compared to values at room temperature. Fig. 4 shows the breakdown voltage comparison of the selected devices. Generally, SiC MOSFETs and GaN HEMTs show relatively

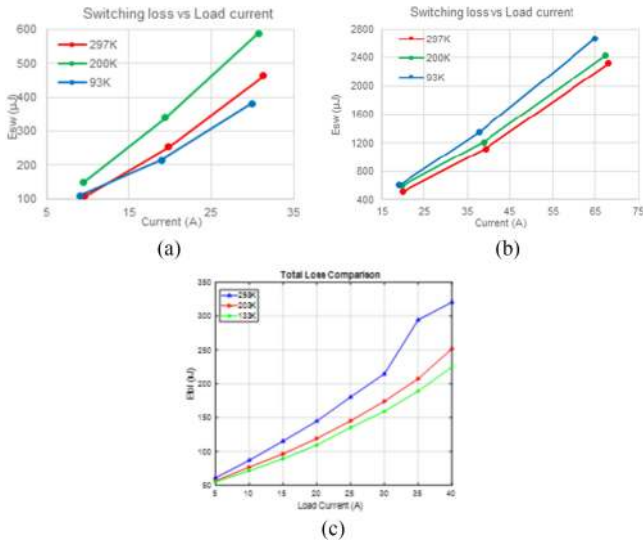


FIGURE 5. Comparison of switching loss of SiC and GaN. (a) T1 at 500 V dc voltage and 1 Ω gate resistance, (b) T2 at 500 V DC voltage and 1 Ω gate resistance, (c) T4 at 400 V dc voltage, 20 Ω turn-on and 2 Ω turn-off gate resistance.

constant breakdown voltage while the Si MOSFETs show reduced breakdown voltage when temperature decreases from room temperature to cryogenic temperatures. Note that the breakdown voltages in Fig. 4 was obtained at a defined leakage current (usually hundreds of uA according to datasheet), which is lower than the destructive breakdown voltages.

Switching loss characteristics depend on specific operation conditions. Fig. 5 summarizes the switching loss of T1, T2, and T4. In general, the switching loss of SiC MOSFETs increases while that of GaN HEMTs decreases as temperature decreases.

III. DEMONSTRATION OF MW-LEVEL SiC CONVERTER OPERATION WITH CRYOGENIC COOLING

This section presents a MW-level SiC power module based inverter using cryogenic cooling for electric aircraft propulsion applications. This 1 MW inverter is dc-fed from ± 500 V bus with three-phase output fundamental frequency up to 3 kHz.

A. DEVICE SELECTION

Based on device characterization results, Si MOSFET and GaN HEMT show better performance at cryogenic temperatures. However, high current power modules (hundreds of Amps) for Si MOSFET or GaN HEMT devices to support a MW inverter are not yet available. More importantly, none of the commercial module packaging technologies are suitable for cryogenic operation. Therefore, high current SiC power module is selected. The SiC power module is not directly cooled down to cryogenic temperatures due to the limitation of module package as well as the degraded performance of SiC at cryogenic temperatures. However, cryogenic cooling will still benefit the inverter as it could provide a lower ambient temperature environment and thus SiC device junction

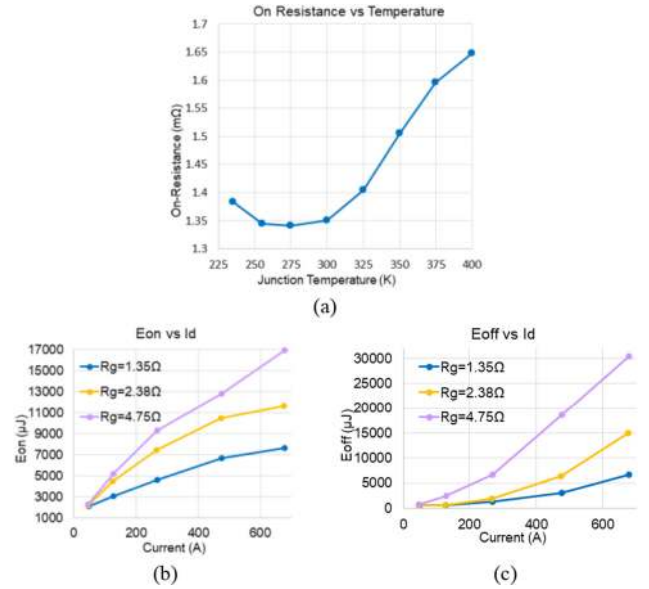


FIGURE 6. The 900V/800A Wolfspeed SiC power module test data. (a) on-state resistance at different temperatures, (b) turn-on loss and (c) turn-off loss at 500 V dc bus voltage with several different gate resistances.

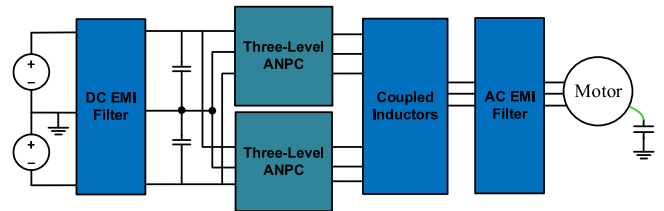


FIGURE 7. The 3L-ANPC based 1 MW inverter system.

temperature could be lower during high power operation and the inverter can achieve higher efficiency compared to the room temperature cooling case. Cryogenic cooling will also benefit the busbars and filter windings in the inverter system.

The 900V/800A Wolfspeed 3rd generation SiC power module is selected to support this 1 MW inverter. Fig. 6(a) shows its on-state resistance at different temperatures. The power module is characterized at temperatures not below 225 K because of the silicone gel of this module package could be damaged below 225 K. The lowest on-state resistance is achieved at temperature around 257 K and the cooling system can be optimized to keep the device junction temperature near this temperature for rated operation. The cooling design is illustrated in next section. Fig. 6(b) and Fig. 6(c) show the tested switching loss.

With the selected power module, three-level active neutral point clamped (3L-ANPC) inverter topology is utilized and two 500 kW inverters are parallel and interleaved through coupled inductors to achieve 1 MW power while reducing harmonic ripples. Fig. 7 shows the inverter system. Dc and ac side EMI filters are employed to suppress EMI noise and meet DO-160 EMI standards in aircraft applications. The switching

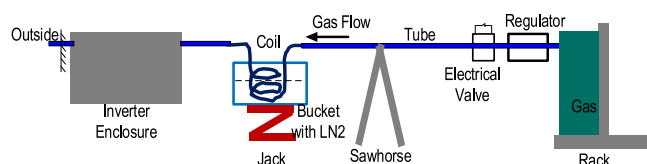


FIGURE 8. Power module cold gas nitrogen cooling concept.

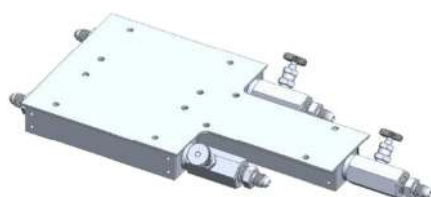


FIGURE 9. Customized modular coldplate.

transient analysis, harmonics analysis, busbar design, and filter design of paralleled 3L-ANPC inverters can be referred in [26]–[32].

B. COOLING SYSTEM DESIGN AND INTEGRATION

As illustrated above, direct liquid nitrogen cooling cannot be used for the SiC power module due to the package limitation as well as increased loss at cryogenic temperatures. Therefore, cold nitrogen gas cooling is utilized for the power stage. Fig. 8 shows the cooling concept. The nitrogen gas goes through coils which are submerged into a liquid nitrogen bucket. The nitrogen gas becomes cooled by the liquid nitrogen and flows through the coldplate for the power module. By adjusting the height of the jack which supports the bucket, the number of turns of the coils that are submerged into liquid nitrogen can be adjusted. The cooling performance of the gas nitrogen system can be controlled by adjusting the flow rate of the gas through a regulator combined with adjusting the turns number of coils submerged in the liquid nitrogen.

The coldplate is custom designed to fit the proposed cooling method as shown in Fig. 9. The coldplate unit in Fig. 9 has three separate channels and used to cool three half-bridge power modules which form a phase-leg of the three-level ANPC inverter. The gas nitrogen flow rate of the three channels can be controlled individually with the valves as shown in Fig. 9. Moreover, tapered fins are used inside the coldplate channel to provide a uniform temperature distribution of all the dies in an individual module.

The filters can use direct liquid nitrogen cooling because of the significantly reduced resistivity of copper used for inductor windings. 3D-printed thermoplastic housing is designed for the inductors to accommodate liquid nitrogen cooling for large inductors and to reduce housing weight.

Therefore, the dual gas and liquid nitrogen cooling strategy is utilized to accommodate the cooling requirement of both the SiC power modules and inductors in the 1 MW inverter system. The cooling system design is shown in Fig. 10. Each

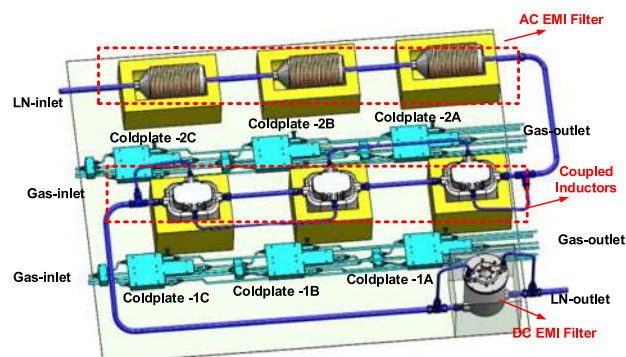


FIGURE 10. The dual gas and liquid nitrogen cooling system for the MW inverter system.

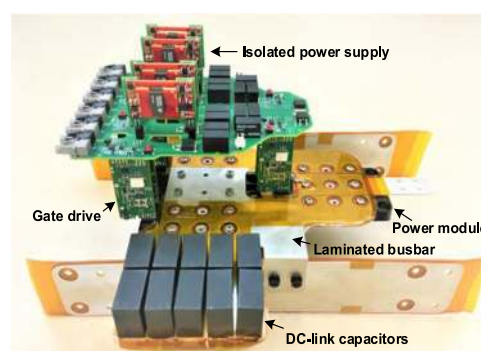


FIGURE 11. A phase-leg of the 3L-ANPC inverter prototype.

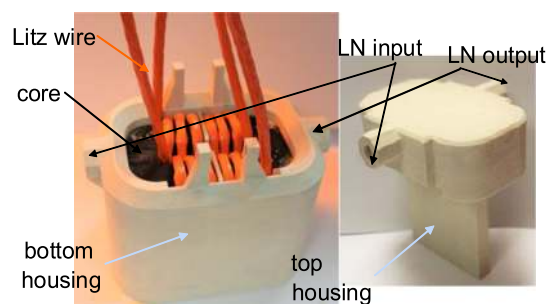


FIGURE 12. Coupled inductor prototype with housing.

500 kW inverter power stage has a gas nitrogen path. The ac side inductors, coupled inductors, and dc side CM inductors all share a liquid nitrogen path. There is no mechanical or thermal interference among the electrical busbars and their connections, the liquid nitrogen flow system, and the gas nitrogen flow system.

Fig. 11 shows the prototype of a phase-leg of one 500 kW three-level ANPC inverter which consists of power module, DC-link capacitors, busbar, gate drive and isolated power supply. Fig. 12 shows the coupled inductor prototype with housing. The integration layout of the MW inverter system with enclosure is shown in Fig. 13. Foams (yellow blocks

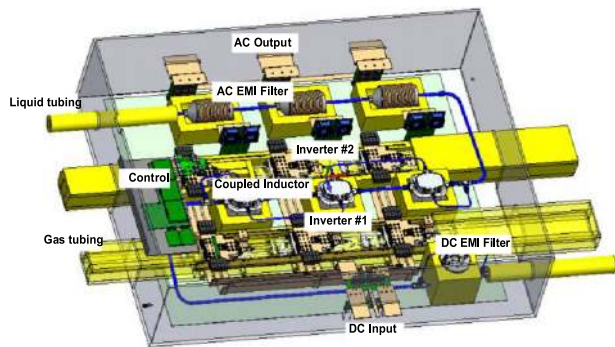


FIGURE 13. The integrated MW inverter system.

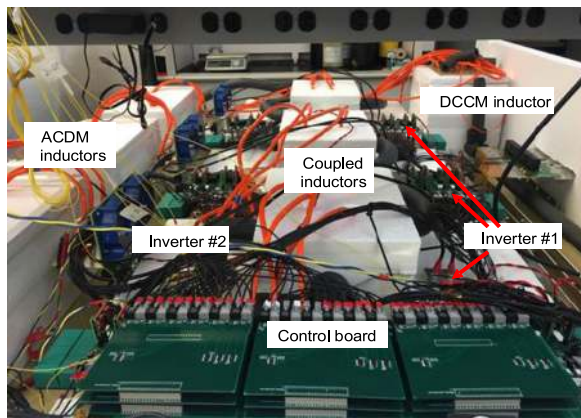


FIGURE 14. MW inverter system hardware.

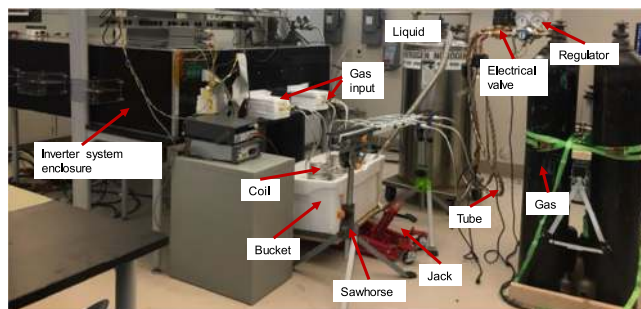


FIGURE 15. Cryogenic cooling setup for the 1 MW inverter system.

in Fig. 13) are attached around the cooling tubes, inductors, and coldplates to achieve thermal insulation between cryogenically-cooled components and other components in the system. Thus, the temperatures of gate driver and auxiliary components are similar to those of a room temperature converter.

Fig. 14 shows inverter hardware inside the enclosure and Fig. 15 shows the cryogenic cooling system setup outside the enclosure with the cooling strategy concept shown in Fig. 8.

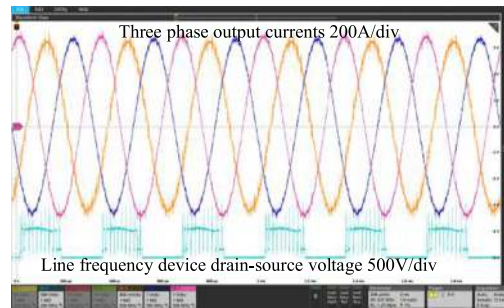


FIGURE 16. Tested waveforms of one 500 kW inverter at full load.

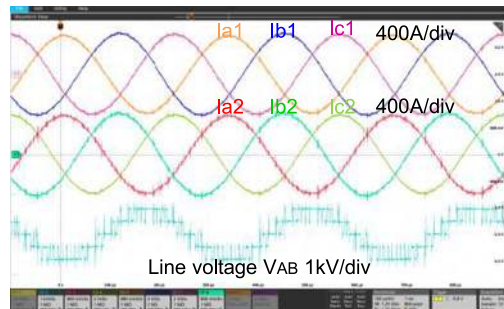


FIGURE 17. Tested two inverters paralleling operation at 1 MVA full load.

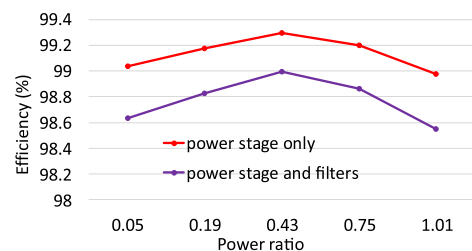


FIGURE 18. Tested inverter efficiency at different loads.

C. INVERTER TESTING WITH CRYOGENIC COOLING

With the cryogenic cooling system illustrated above, the full power testing of this SiC based 1 MW inverter with cryogenic cooling is conducted. First, one 500 kW inverter is tested to full power with cryogenic cooling. Fig. 16 shows the tested three-phase output current waveforms at 1 kV dc bus voltage input. The measured peak current is around 650 A.

Then, two 500 kW inverters paralleling operation is tested at full power. Fig. 17 shows the three-phase current waveforms of the paralleled inverters and a line-to-line voltage waveform. For this test, the ac phase output voltage fundamental frequency components peak voltage is 549 V and ac phase peak current for one inverter is 610 A, and the total apparent power is 1 MVA.

The MW inverter prototype power loss is tested. Fig. 18 shows the tested inverter efficiency at different loads. The power stage efficiency is 99.2% at half load and 99% at full load. If the filter power loss is included, which takes around

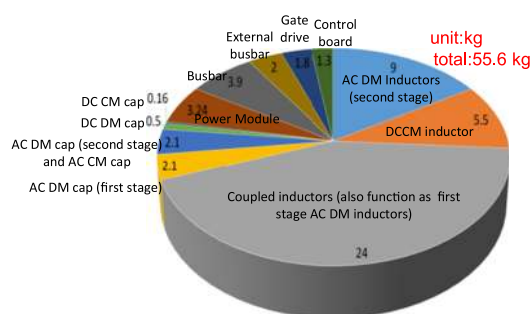


FIGURE 19. Weight breakdown of the inverter.

30% of the total inverter system loss, the efficiency is 98.9% at half load and 98.5% at full load. The MW inverter system weight is measured. Without the enclosure and cooling system, which were not optimized in this prototype, the total weight is 55.6 kg, indicating a specific power of 18 kVA/kg.

It is noted that this MW inverter design assumes the need for inverter ac side to also meet DO-160 EMI standards. Consequently, ac side EMI filter is required. The assumption of the motor load with high fundamental frequency of 3 kHz and therefore low inductance, exacerbates the situation. To reduce the required ac side filter, especially DM filter, the carrier frequency of the two inverters is increased to 60 kHz and interleaved, resulting considerable switching loss. The coupled inductors required for interleaving with their leakage inductance function as DM inductor, also contribute to appreciably higher weight and loss. Fig. 19 shows the weight breakdown of the inverter. In fact, the ac side filter, together with the coupled inductors, contributes about 2/3 of the total inverter system weight. If the ac side has no EMC requirements and only dv/dt filter is needed, the filter weight can be reduced and switching frequency can also be reduced for loss reduction. In this case, the 1 MW inverter system efficiency and specific power can be considerably higher.

With the proposed dual gas and liquid nitrogen cooling strategy, both power stage loss and filter loss of the MW SiC inverter are reduced compared to room temperature converters. However, additional size and weight by the cooling components (outside the inverter system enclosure as shown in Fig. 15) may offset the goal. Cooling system sizing and optimization will be future work to justify the benefit of cryogenic cooling.

IV. DEMONSTRATION OF GAN HIGH CURRENT OPERATION WITH CRYOGENIC COOLING

As shown in Fig. 3(a), GaN HEMTs show the lowest specific on-state resistance at cryogenic temperatures. The significantly reduced on-state resistance provides the possibility to operate GaN HEMTs at a current level much higher than rated at cryogenic temperatures than nominally rated value for room temperature. The high current operation of GaN HEMT with cryogenic cooling is conducted in this section.

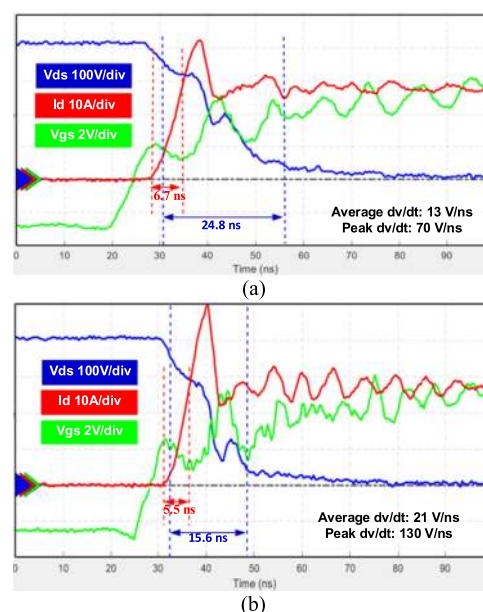


FIGURE 20. Turn-on transient of the rated current dynamic characterization at 400V/30A. (a) 298 K, (b) 133 K.

A. DYNAMIC CHARACTERIZATION AT RATED CURRENT

The dynamic characterization is conducted using the DPT circuit setup as shown in Fig. 2. The selected GaN HEMT is the 650V/30A GS66508T from GaN Systems. The turn-on and turn-off gate voltages are 6 V and -3 V, respectively. The turn-on and turn-off gate resistance are 20 Ω and 2 Ω , respectively. Gate driver IC is Si2871 from Silicon Labs. In the test, when temperature decreases to below 123 K, the output of the isolated power supply and gate drive IC cannot keep at rated voltage and obviously gate voltage drop can be observed. Thus, the dynamic characterization is conducted at temperatures above 123 K.

At low temperatures, the switching speed becomes much faster due to increased transconductance. Fig. 20 shows the turn-on transient waveforms comparison at 400 V dc bus and rated 30 A load at both room temperature and a cryogenic temperature. The voltage fall time and current rise time are smaller in Fig. 20(b) compared to Fig. 20(a), indicating faster switching at cryogenic temperature. The tested average dv/dt and peak dv/dt are 13 V/ns and 70 V/ns at room temperature while the tested average dv/dt and peak dv/dt are 21 V/ns and 130 V/ns at cryogenic temperature. The dv/dt is nearly doubled at cryogenic temperature. Fig. 21 summarizes switching loss at different temperatures. Compared to room temperature case, the turn-on switching loss is reduced by around 30% while turn-off loss is almost kept unchanged at cryogenic temperatures.

B. DYNAMIC CHARACTERIZATION AT HIGH CURRENT

The high current operation test still utilizes the DPT circuit. But the load current will start from the rated 30 A and keeps

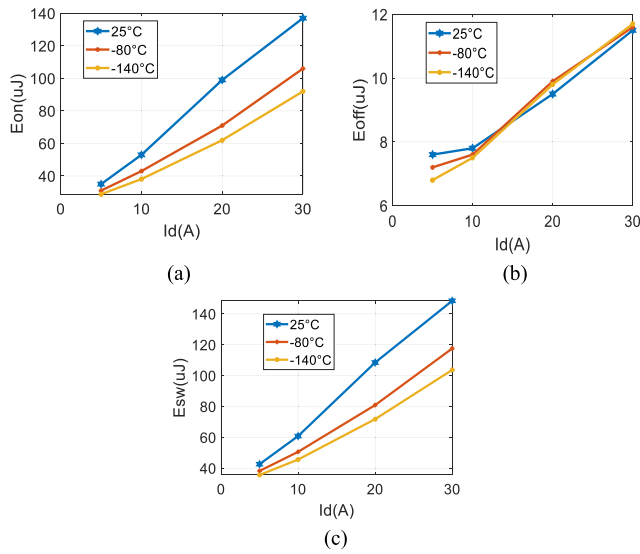


FIGURE 21. Switching loss at different temperatures: (a) turn-on loss, (b) turn-off loss, (c) total switching loss.

increasing until desaturation-based protection triggers or device failure occurs. As GaN device is more sensitive to gate voltage, the gate measurement probe could introduce extra noise and interfere with the gate loop, and result in large oscillation during high dv/dt or di/dt switching transient. Thus, the gate signal is not measured in the high current operation test.

The turn-off transient becomes faster and severe turn-off overvoltage occurs for high current operation. In the test, when load current increases from rated 30 A to 60 A for 400 V dc bus, the turn-off overvoltage exceeds 700 V even though the turn-off gate resistance is increased from 2 Ω to 5.1 Ω . To keep the turn-off voltage below 600 V for safe operation, the turn-off resistance is selected to be 15 Ω .

At the cryogenic temperature, the load current can be increased to 115 A, which is nearly 4 times of the rated current of this device. If further increasing the load current, desaturation protection triggers or device failure occurs frequently. The root cause of this phenomenon is still unclear and could be because the current exceeds the package limit of this device.

Fig. 22 shows the tested switching waveforms at 80 A current, and Fig. 23 shows the tested switching waveforms at 115 A current, both at 400 V dc bus voltage and cryogenic temperature of 133 K. For the 115 A case, the tested average dv/dt is 60 V/ns and peak dv/dt is 130 V/ns. The turn-off voltage is within 600 V. Fig. 24 summarizes the switching loss at high current operation from 40 A to 115 A.

V. CHALLENGES FOR UTILIZING SIC AND GAN WITH CRYOGENIC COOLING

Cryogenic cooling enables better performance for WBG devices (mainly GaN HEMTs) compared to room temperature cooling. Cryogenic cooling also benefits WBG based power

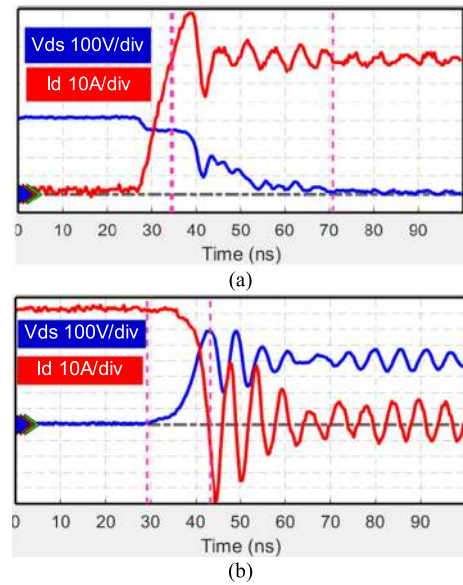


FIGURE 22. High current dynamic characterization at 400V/80A and 133 K temperature. (a) turn-on transient, (b) turn-off transient.

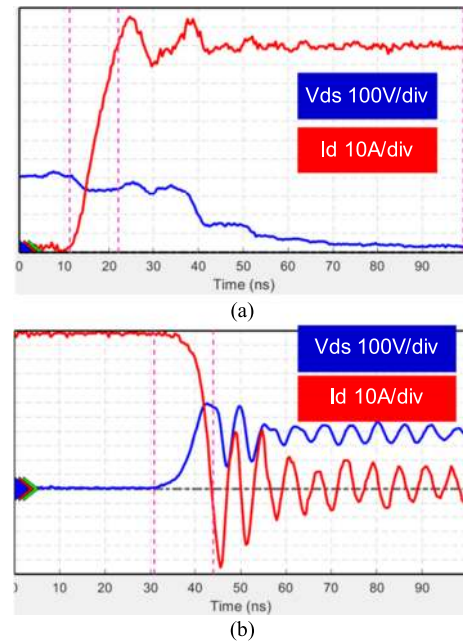


FIGURE 23. High current dynamic characterization at 400V/115A and 133 K temperature. (a) turn-on transient, (b) turn-off transient.

converters due to less cooling requirement provided by low operating temperature as well as by light and/or efficient conductors (e.g., busbars and inductor windings) at low temperature. In the meanwhile, cryogenic cooling also poses new design challenges. Special consideration must be given to the power converter design with cryogenic cooling in order to utilize it effectively and reliably. WBG devices with cryogenic cooling application is in the starting phase and far from technology maturity. Several key issues are discussed below.

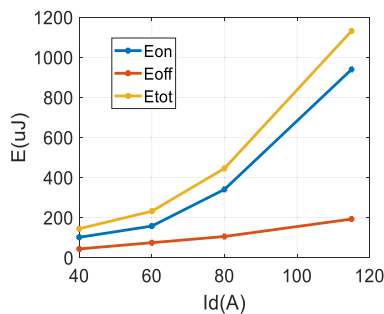


FIGURE 24. Switching loss for high current operation at 133 K.

A. PACKAGING

Packaging device dies into power modules involve electrical, thermal, and mechanical design. Packaging technologies to achieve parasitic minimization, current and thermal balancing among multiple dies, high electric field and high temperature withstand capability are critical for WBG application and being addressed by researchers and device manufactures. However, no commercially available device packages have taken cryogenic operation into account.

One key issue is the encapsulant materials for power module packaging. The most used materials for encapsulant are silicone gel based or epoxy based. Silicone gel cannot survive at cryogenic temperatures [33]. Partial discharge occurs when temperature is below 215 K and will significantly reduce breakdown voltage of the silicone gel. Moreover, degradation of the breakdown voltage cannot be recovered even when temperature returns to room temperature. Thus, most power modules utilizing silicone gel based encapsulants cannot be used at cryogenic temperature. On the other hand, most epoxies can work properly at cryogenic temperatures [34]. Hence, epoxy could be the encapsulate material for device packaging operating at cryogenic temperatures. One potential issue is that epoxy tends to be more brittle at low temperature. Design packaging without encapsulation can also be considered. But the module may suffer from external environmental damages as well as reduced insulation capability. Another issue is the thermal-mechanical stress of packaging material at cryogenic temperature. If thermal expansion coefficients (CTE) mismatch of the packaging material in the multi-layer package structure is not well controlled, the large thermally induced stress at cryogenic temperatures may cause packaging degradation or even device failure.

B. GATE DRIVE AND PROTECTION

Gate driver is a key component to achieve optimal device performance for power converters. Cryogenic cooling posed challenges for gate drive and protection are summarized as follows.

1) Circuit components suitable for cryogenic temperatures

Gate driver mainly consists of driver IC, signal isolator, and isolated power supply. The gate driver IC are usually BJT

based or CMOS based. Si BJT's show poor performance at low temperature. The current gain β of the BJT drops significantly with the decreases of temperature [35]. The base-collector breakdown voltage also decreases as temperature decreases due to the typical P-N diode characteristics. Therefore, BJT based ICs are not suitable for cryogenic temperature. On the other hand, the CMOS based ICs show faster switching speed at low temperature due to the increase of carrier mobility and saturation velocity. The CMOS based ICs could be suitable for low temperature operation. Potential issues with CMOS based ICs is the reliability issues at low temperature, mainly the gate degradation caused by hot carriers [36]–[39]. Potential solution to mitigate the impact of hot carrier effect is to reduce gate voltage at very low temperature so that the electric field is decreased and the possibility for carriers to gain energy to flow into the gate oxide is reduced.

The key issues are the signal isolator and isolated power supply operating at low temperature. The primary side and secondary sides of isolation components suffer from high dv/dt during switching transient. The input-to-output parasitic capacitance provides a path to conduct CM noise induced by dv/dt . For WBG devices with high dv/dt during switching, high CM noise immunity capability or low isolation capacitances is critical for signal isolator and isolated power supplies. The commercially available signal isolators and isolated power supplies with high dv/dt immunity may not function well at very low temperatures. For example, the state-of-art isolated gate drivers Si827x from Silicon Labs shows industry leading common-mode transient immunity which exceeds 200 V/ns and widely used in GaN HEMT circuits. Test results at cryogenic temperatures indicate that this isolator cannot work properly if the temperature is below 120 K. Most isolated power supplies consist of an isolated transformer and a flyback converter. Ferrite core is typically used for the transformer. However, ferrite core loss increased more than 10 times and permeability decreases by a factor of 7~8 when operated at 93 K [32]. The significantly degraded performance of the magnetic may cause malfunction of the isolated power supply. Several isolated power supplies with picofarad level isolation capacitance from Traco Power and Murata are also tested at low temperatures. All the power supplies show reduced output voltage as temperature decreases. One potential solution is to use nanocrystalline core instead of ferrite core for the transformer of the isolated power supply. Nanocrystalline material shows less performance degradation compared to ferrite material at cryogenic temperature [32].

2) Faster switching of GaN HEMT at cryogenic temperatures

GaN HEMTs have increased transconductance and faster switching speed at cryogenic temperatures, resulting in higher dv/dt and/or di/dt . As presented in section IV, the dv/dt during switching transients can double at cryogenic temperatures compared to that at room temperature. The extremely high dv/dt and/or di/dt at cryogenic temperature brings several issues.

a: *Overvoltage*: Overvoltage occurs during turn-off transient or during turn-on transient of its complementary device in a phase-leg configuration. High voltage spikes during switching transient could cause device breakdown. Compared to room temperature operation, the faster switching speed and smaller on-state resistance at cryogenic temperatures exacerbate this issue. Advanced packaging techniques and optimal layout design for parasitics minimization can relieve the overvoltage. Compared to the power loop overvoltage, the more severe issue is the gate loop overvoltage because GaN HEMT has much lower gate voltage withstand capability than Si or SiC MOSFETs. The power loop impacts the gate loop through the device Miller capacitance as well as the common-source inductance. Higher dv/dt and/or di/dt at cryogenic temperature increases the chance of gate damage of GaN HEMT. To mitigate this issue, a kelvin connection of source terminal is required, and shared common trace or wire bond between the gate loop and the power loop should be avoided in the package design. A clear separation of layout in the gate driver PCB between the power loop and the gate loop should also be maintained. Besides, advanced gate control technologies such as active Miller clamp, and dv/dt or di/dt active control can be applied to avoid device failure.

b: *Crosstalk*: The crosstalk between two switches generates a shoot-through current, leading to additional switching losses in both switches and shoot-through failure. Faster switching speed and higher dv/dt at cryogenic temperature also increases the susceptibility of crosstalk in a phase-leg configuration. To mitigate crosstalk without sacrificing fast switching, several gate assist circuits can be adopted [40]–[42].

c: *Sustained oscillation and instability*: Sustained oscillation is also excited by device switching actions. WBG devices and associated parasitic components in the gate loop and the power loop can form an unintentional negative oscillator to produce sustained oscillation [43]–[46]. Although it only occurs at certain conditions, sustained oscillation can result in destabilization of the power circuit and even device damage. It produces a burst of “forced” oscillation which may sustain until bus voltage energy is depleted. The susceptibility of sustained oscillation increases with reduced on-state resistance and with increased device transconductance [44]. At cryogenic temperature, on-state resistance is significantly reduced while transconductance is significantly increased, both contribute to the susceptibility of sustained oscillation. The sustained oscillation and instability issues of GaN HEMT operating at cryogenic temperature need to be investigated. Another mechanism for sustained oscillation is due to the unique reversed conduction behavior of GaN HEMT, which is different from the unintentional negative oscillator described above. Modeling and stability analysis can

be found in [47]. Cryogenic temperature impacts the threshold voltage as well as the transconductance and thus the reverse conduction behavior of GaN HEMTs. How cryogenic temperature impact the reverse conduction related sustained oscillation and stability need to be further investigated.

d: *Protection*: Short-circuit protection is usually integrated in gate drive circuits. Under high dv/dt and di/dt conditions, it is challenging for a short circuit protection scheme to achieve fast response time and strong noise immunity simultaneously. A three-step short-circuit protection method can be considered to mitigate this issue for GaN HEMTs [50]. WBG device short-circuit withstand time is critical for protection response time determination. The short circuit behavior of GaN HEMT is very sensitive to temperature. When short-circuit occurs, the current first increases quickly to a peak value and then starts to decrease because the strong negative temperature feedback realizes the short-circuit current self-regulation [48]. Cryogenic cooling impact on the short-circuit withstand time can be illustrated from two aspects. On one hand, cryogenic cooling provides a low ambient temperature. Thus, higher temperature rise is allowed for the device, which is beneficial to short circuit withstand time. On the other hand, due to the lower initial temperature provided by cryogenic cooling, current increases faster and the short-circuit current peak is also higher. Thus, the energy accumulates faster, which is detrimental to short circuit withstand time. Moreover, the high localized electric field may breakdown the device in addition to thermal-related failure [49]. Therefore, considering these two aspects, the short-circuit withstand capability of GaN HEMTs with cryogenic cooling is unclear and needs further investigation.

C. EMI FILTER

The EMI filter is necessary for power converter to suppress EMI noise and meet EMI standards. First, the faster switching at cryogenic temperature provides the opportunity to operate at higher switching frequency and thus reduce the required passive EMI filters. However, EMI noise will also tend to concentrate in the high frequency range and increases filter design difficulties due to the non-ideal behaviors of the passive filter, i.e., the equivalent parallel capacitance (EPC) of inductor and the equivalent series inductance (ESL) of capacitor, and the coupling effect of filter components at high frequencies. Second, cryogenic cooling could benefit inductor winding but introduce penalty on the magnetic core as illustrated above. Filter housing design optimization to compromise core loss and winding loss and thus maximizing cryogenic cooling benefit requires further research.

D. COOLING SYSTEM

Cryogenic cooling system is more complex and challenging than room temperature cooling system. Special requirements

of cryogenic cooling system include: 1) No leakage. The density of liquid nitrogen is over 6000 times higher than air. If leak happens, it is highly possible to introduce high pressure in the converter enclosure. 2) Good thermal insulation. Temperature of liquid nitrogen is extremely low, and leakage can cause injury. Operators must be protected from cryogenic temperature of converter system. 3) Good air insulation. As the temperature of liquid nitrogen or cold gas nitrogen is much lower than air, vapor in the air can freeze and cause short-circuit in the converter. For safety consideration, the risk assessment should also be considered for cooling system design.

VI. CONCLUSION

This article presents cryogenically cooled application for WBG devices. The state-of-art GaN HEMTs achieve >5X on-state resistance reduction while SiC MOSFETs show significantly increased on-state resistances at cryogenic temperatures. GaN HEMTs show faster switching speed and achieve around 30% switching loss reduction while SiC MOSFETs show slower switching speed and increased switching loss at cryogenic temperatures. Both GaN HEMTs and SiC MOSFETs show relatively constant breakdown voltages in a wide temperature range. A MW-level SiC inverter with cryogenic cooling is developed and demonstrates the feasibility of high-power operation of SiC power modules with cryogenic cooling. This inverter achieves 18 kVA/kg specific power and 99% efficiency which provides a promising motor drive solution for future aircraft propulsion applications. The feasibility of high-current operation of GaN HEMTs with cryogenic cooling is presented. Dynamic characterization results show the 30 A GaN HEMT can operate at 115 A with cryogenic cooling, which is nearly four times of its rated current. The challenges and special considerations of utilizing SiC and GaN devices with cryogenic cooling including packaging, gate drive and protection, EMI filter and cooling system are discussed and summarized, which is critical for WBG devices cryogenic cooled application.

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REFERENCES

- [1] S. Yang, "Cryogenic characteristics of IGBTs," Ph.D. Dissertation, Univ. of Birmingham, Birmingham, U.K., 2005.
- [2] R. Singh and B. J. Baliga, *Cryogenic Operation of Silicon Power Devices*. New York NY, USA: Springer, 2012.
- [3] C. Jia, "Experimental investigation of semiconductor losses in cryogenic DC-DC converters," Ph.D. Dissertation, Uni. of Birmingham, Birmingham, U.K., 2008.
- [4] N. Ahmad, "Carrier freeze-out effects in semiconductor devices," *J. Appl. Phys.*, vol. 61, no. 5, pp. 1905–1909, 1987.
- [5] K. Leong, B. Donnellan, A.T. Bryant, and P. A. Mawby, "An investigation into the utilization of power MOSFETs at cryogenic temperatures to achieve ultra-low power losses," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2010, pp. 2214–2221.
- [6] Z. Zhang *et al.*, "Characterization of high-voltage high-speed switching power semiconductors for high frequency cryogenically-cooled application," in *Proc. IEEE Appl. Power Electron. Conf.*, 2017, pp. 1964–1969.
- [7] Y. Chen *et al.*, "Experimental investigations of state-of-the-art 650-V class power MOSFETs for cryogenic power conversion at 77K," *IEEE J. Electron. Devices Soc.*, vol. 6, no. 1, pp. 8–18, Oct. 2018.
- [8] A. Caiafa, A. Snezhko, J. Hudgins, E. Santi, and R. Prozorov, "IGBT operation at cryogenic temperatures: Non-punch-through and punch through comparison," in *Proc. IEEE Power Electron. Spec. Conf.*, 2004, vol. 4, pp. 2960–2966.
- [9] A. Caiafa, X. Wang, J. Hudgins, E. Santi, and P. Palmer, "Cryogenic study and modeling of IGBTs," in *Proc. IEEE Power Electron. Spec. Conf.*, vol. 4, 2003, pp. 1897–1903.
- [10] J. Qi *et al.*, "Dynamic performance of 4H-SiC power MOSFETs and Si IGBTs over wide temperature range," in *Proc. IEEE Appl. Power Electron. Conf.*, 2018, pp. 2712–2716.
- [11] H. Chen *et al.*, "Cryogenic characterization of commercial SiC Power MOSFETs," *Mater. Sci. Forum*, vol. 821–823, pp. 777–780, 2015.
- [12] S. Chen, C. Cai, T. Wang, Q. Guo, and K. Sheng, "Cryogenic and high temperature performance of 4H-SiC power MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf.*, 2013, pp. 207–210.
- [13] H. Gui *et al.*, "Characterization of 1.2 kV SiC power MOSFETs at cryogenic temperatures," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 7010–7015.
- [14] J. Colmenares, T. Foulkes, C. Barth, T. Modeert, and R. C. Pilawa-Podgurski, "Experimental characterization of enhancement mode gallium-nitride power field-effect transistors at cryogenic temperatures," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl.*, 2016, pp. 129–134.
- [15] R. Ren *et al.*, "Characterization of 650 V enhancement GaN HEMT at cryogenic temperatures," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 891–897.
- [16] R. Cuervo *et al.*, "The kink effect at cryogenic temperatures in deep submicron AlGaIn/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 30, no. 3, pp. 209–212, Mar. 2009.
- [17] J. K. Kaushik, V. R. Balakrishnan, B. S. Panwar, and R. Muralitharan, "On the origin of kink effect in current-voltage characteristics of AlGaIn/GaN high electron mobility transistors," *IEEE Trans. Electron. Devices*, vol. 60, no. 10, pp. 3351–3357, Oct. 2013.
- [18] R. E. Mayo, J. G. Bustamante, and T. L. Beechner, "Wide temperature range operation of GaN HEMTs for power dense energy conversion," in *Proc. IEEE Intersoc. Conf. Thermal Thermomech. Phenomena Electron. Syst.*, 2017, pp. 530–536.
- [19] J. Garrett, R. Schupbach, H. A. Mantooth, and A. B. Lostetter, "Development of an extreme environment DC motor drive full bridge power stage using commercial-off-the-shelf components," in *Proc. Int. Planet. Probe Workshop*, 2006.
- [20] A. J. Forsyth *et al.*, "Cryogenic converter for superconducting coil control," *IET Power Electron.*, vol. 5, no. 6, pp. 739–746, Jul. 2012.
- [21] O. M. Mueller and K. G. Herd, "Ultra-high efficiency power conversion using cryogenic MOSFETs and HT-superconductors," in *Proc. IEEE Power Electron. Spec. Conf.*, 1993, pp. 772–778.
- [22] B. Ray, S. S. Gerber, R. L. Patterson, and I. T. Myers, "77 K operation of a multi-resonant power converter," in *Proc. Power Electron. Spec. Conf.*, vol. 1, 1995, pp. 55–60.
- [23] H. Gui *et al.*, "Development of high-power high switching frequency cryogenically cooled inverter for aircraft applications," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5670–5682, June. 2020.
- [24] C. Barth *et al.*, "Design, operation, and loss characterization of a 1-kW GaN-based three-level converter at cryogenic temperatures," *IEEE Trans. Power Electron.*, vol. 35, no. 11, pp. 12040–12052, Nov. 2020.
- [25] R. Chen, J. Niu, R. Ren, H. Gui, F. Wang, and L. M. Tolbert, "A cryogenically cooled MW inverter for electrified aircraft propulsion," in *Proc. AIAA/IEEE Electric Aircraft Technol. Symp.*, 2020, pp. 1–9.
- [26] H. Gui *et al.*, "Modeling and mitigation of multiloops related device overvoltage in three-level active neutral point clamped converter," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 7947–7959, Aug. 2020.
- [27] H. Gui *et al.*, "Design of low inductance busbar for 500 kVA three-level ANPC converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2019, pp. 7130–7137.
- [28] R. Chen *et al.*, "Analytical analysis of ac and dc side harmonics of three-level active neutral point clamped inverter with space vector modulation," in *Proc. IEEE Appl. Power Electron. Conf.*, 2019, pp. 112–119.

- [29] R. Chen *et al.*, "Coupled inductor design for interleaved three-level active neutral point clamped inverters considering EMI noise reduction," in *Proc. IEEE Appl. Power Electron. Conf.*, 2019, pp. 257–264.
- [30] R. Chen *et al.*, "Modeling, analysis, and reduction of harmonics in paralleled and interleaved three-level neutral point clamped inverters with space vector modulation," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 4411–4425, Apr. 2020.
- [31] R. Chen *et al.*, "Common-mode inductor saturation analysis and design optimization based on spectrum concept," in *Proc. IEEE Appl. Power Electron. Conf.*, 2018, pp. 2583–2588.
- [32] R. Chen *et al.*, "Core characterization and inductor design investigation at low temperature," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 4218–4225.
- [33] T. Vu, J.-L. Auge, and O. Lesaint, "Low temperature partial discharge properties of silicone gels used to encapsulate power semiconductors," in *Proc. IEEE Conf. Elect. Insul. Dielect. Phenomena.*, 2009, pp. 421–424.
- [34] Epoxy Technology Inc. Cryogenic Temperature and Epoxies. 2015. [Online]. Available: <https://www.epotek.com/docs/en/Related/Selected%20Application-%20Cryogenic%20Temperature%20and%20Epoxies.pdf>
- [35] W. P. Dumke, "The effect of base doping on the performance of Si bipolar transistors at low temperatures," *IEEE Trans. Electron. Devices*, vol. 28, no. 5, pp. 494–500, May 1981.
- [36] B. Okcan, P. Merken, G. Gielen, and C. VanHoof, "A cryogenic analog to digital converter operating from 300 K down to 4.4 K," *Rev. Sci. Instrum.*, vol. 81, no. 2, 2010, Art. no. 024702.
- [37] A. Dejenfelt and O. Engström, "MOSFET mobility degradation due to interface-states, generated by Fowler-Norheim electron injection," *Microelectron. Eng.*, vol. 15, no. 1–4, pp. 461–464, 1991.
- [38] Y. Chen *et al.*, "Design for ASIC reliability for low-temperature applications," *IEEE Trans. Device Mater. Rel.*, vol. 6, no. 2, pp. 146–153, Feb. 2006.
- [39] F. Balestra and G. Ghibaudo, *Device and Circuit Cryogenic Operation for Low Temperature Electronics*. New York, NY, USA: Springer, 2013.
- [40] Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Active gate driver for crosstalk suppression of SiC devices in a phase-leg configuration," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1986–1997, Apr. 2014.
- [41] J. Wang *et al.*, "A novel RCD level shifter for elimination of spurious turn-on in the bridge-leg configuration," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 976–984, Feb. 2015.
- [42] S. Yin *et al.*, "A novel gate assisted circuit to reduce switching loss and eliminate shoot-through in SiC half bridge configuration," in *Proc. IEEE Appl. Power Electron. Conf.*, 2016, pp. 3058–3064.
- [43] A. Lemmon, M. Mazzola, J. Gafford, and C. Parker, "Stability considerations for silicon carbide field-effect transistors," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4453–4459, Oct. 2013.
- [44] A. Lemmon, M. Mazzola, J. Gafford, and C. Parker, "Instability in half bridge circuits switched with wide band-gap transistors," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2380–2392, May 2014.
- [45] Y. Sugihara *et al.*, "Analytical investigation on design instruction to avoid oscillatory false triggering of fast switching SiC-MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo.*, Cincinnati, OH, USA, Oct. 2017, pp. 5113–5118.
- [46] J. Chen, Q. Luo, J. Huang, Q. He, P. Sun, and X. Du, "Analysis and design of an RC snubber circuit to suppress false triggering oscillation for GaN devices in half-bridge circuits," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2690–2704, Mar. 2020.
- [47] K. Wang, X. Yang, L. Wang, and P. Jain, "Instability analysis and oscillation suppression of enhancement-mode GaN devices in half-bridge circuits," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1585–1596, Feb. 2018.
- [48] H. Li *et al.*, "Robustness of 650-V enhancement-mode GaN HEMTs under various short-circuit conditions," *IEEE Trans. Ind. Appl.*, vol. 55, no. 2, pp. 1807–1816, Mar./Apr. 2019.
- [49] P. Williford, F. Wang, S. Bala, and J. Xu, "Short circuit study of 600 V GaN GITs," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl.*, 2019, pp. 36–42.
- [50] X. Lyu *et al.*, "A reliable ultrafast short-circuit protection method for E-mode GaN HEMT," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 8926–8933, Sep. 2020.
- [51] L. Nela, N. Perera, C. Erine, and E. Matioli, "Performance of GaN power devices for cryogenic applications down to 4.2 K," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7412–7416, Jul. 2021.



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