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SiC JFET dc characteristics under extremely high ambient temperatures

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Abstract: This paper reports on the measured dc characteristics of a SiC JFET device from room temperature up to 450°C in order to evaluate the device's capability for high-temperature operation. The authors packaged SiC JFET bare die into a dedicated high-temperature package to be able to perform experiments under extremely high ambient temperatures. The experimental results show that the device can operate at 450°C, which is impossible for conventional Si devices, but the current capability of the SiC JFET diminishes with rising temperatures. For example, the saturation current becomes 20% at 450°C with respect to the value at the room temperature.

Keywords: SiC, JFET, high temperature operation, 450°C, packaging

Classification: Electron devices

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1 Introduction

Silicon Carbide (SiC) has several superior characteristics when used as a semiconductor material [1, 2, 3]. In particular, SiC semiconductor devices are expected to have high temperature, high speed and high voltage operation capabilities, which are attributed to the wide bandgap of SiC, and cannot be obtained with conventional Si-based semiconductor devices. This paper focuses on the high temperature operation capability of SiC devices. Although it has been mentioned that SiC semiconductor devices are suitable for high temperature operation, there are few reports on relatively high temperature operation of SiC devices (i.e., < 250°C) [4]. Furthermore, there has been no report on the operation of gate controllable devices such as JFETs at extremely high ambient temperatures. The main reasons are that the SiC JFET is under development and the difficulty in packaging the device for high temperature operation. The latter requires not only that the SiC JFET bare dies be capable of operation at high temperatures, but also the package including the die attach and wire bonds. To this end, the authors mounted the SiC JFET supplied by SiCED [5, 6] in a dedicated thermally stable package. The dc characteristics of the SiC JFET under extremely high ambient temperature conditions up to 450°C were evaluated using an automated experimental setup for high temperature measurements.

2 Specification of the SiC JFET, Package and Measurement Setup

A SiC device can withstand high temperatures because of its material characteristics but it cannot form part of a circuit by itself without packaging that must be suitable for high temperature. The SiC JFET used in the experiments was supplied by SiCED, which was a research sample bare die. The JFET, usually supplied as a cascode device with a Si MOSFET and packaged in the general plastic IXYS i4 package, has a vertical device topology and 2.8 mm^2 surface area with rated 2.5 A drain current and 1200 V blocking voltage. The authors mounted the JFET bare die on a Ni plated JEDEC TO-258 package to allow high temperature operation. The die has Ni or Al based ohmic terminal contacts and metallization on its top surface. The drain terminal is the backside of the die with a final metallization layer consisting of Ni. This drain contact was bonded to the package. The source and gate have 3 μm Al metallization and were wire bonded to the terminal of package with 3 mil Al wire.

Figure 1 shows the experimental setup for measuring temperature dependency of the SiC JFET dc characteristics. All of the equipment and power

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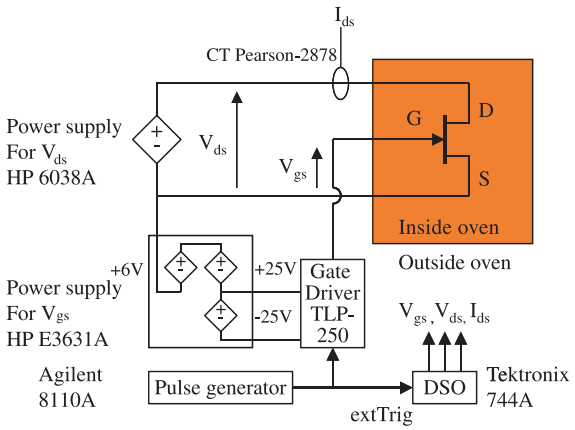

Fig. 1. Experimental setup for characterization of the SiC JFET.

supplies to the device are controlled by a PC with LabView and an IEEE-488 (GPIB) link. The measurements were performed automatically and the data were collected and processed by the PC. There are two power sources; one is used to supply the drain-source voltage (V_{ds}) and the other is used to supply the gate–source voltage (V_{gs}). V_{ds} is swept from 0 V to 20 V to the respective V_{gs}, and V_{gs} was changed as the parameter. The power supply for V_{gs} outputs two level voltages, the higher one is used for the parameter of V_{gs}, and the lower voltage is used to off the JFET. A pulse generator can produce arbitrary width gate pulses and is set to 40 μs to prevent self heating up of the device by conduction current. A digital storage oscilloscope is triggered by the gate signal produced by the pulse generator and performs data acquisition. The PC executes part of the numerical processing and data storage. The control procedures of the instruments in measuring device behaviors and in extracting parameters for the device model are programmed with LabView.

3 JFET dc characteristics for high ambient temperatures

Figure 2 illustrates the I_{ds}-V_{ds} characteristics of a SiC JFET with the gate voltage V_{gs} as a parameter at room, 200°C, 300°C and 450°C ambient temperatures, respectively. Fig. 2 (a) illustrates that the SiC JFET has pentode-like dc characteristics at room temperature. The threshold gate voltage is approximately $V_{gs} = -12$ V, the saturation current for $V_{gs} = 0$ V is about 3.5 A, and a drain-source resistance of approximately 1.33 Ω($\sim$37 mΩ·cm^2). Fig. 2 (b) and (c) shows the threshold gate voltage becomes approximately $V_{gs} = -13$ V at 200°C and $V_{gs} = -14$ V at 300°C, respectively. Fig. 2 (d) shows the dc characteristics when the ambient temperature is extremely high at 450°C, which is beyond the temperature capability of Si-based devices (i.e., 175°C). The pentode-like characteristics of the SiC JFET slightly change to triode-like characteristics and the pinch off drain voltage at $V_{gs} = 0$ V becomes unclear. The saturation current becomes 0.7 A, which is 20% of that at room temperature and the drain-source resistance increases to 10.0 Ω in

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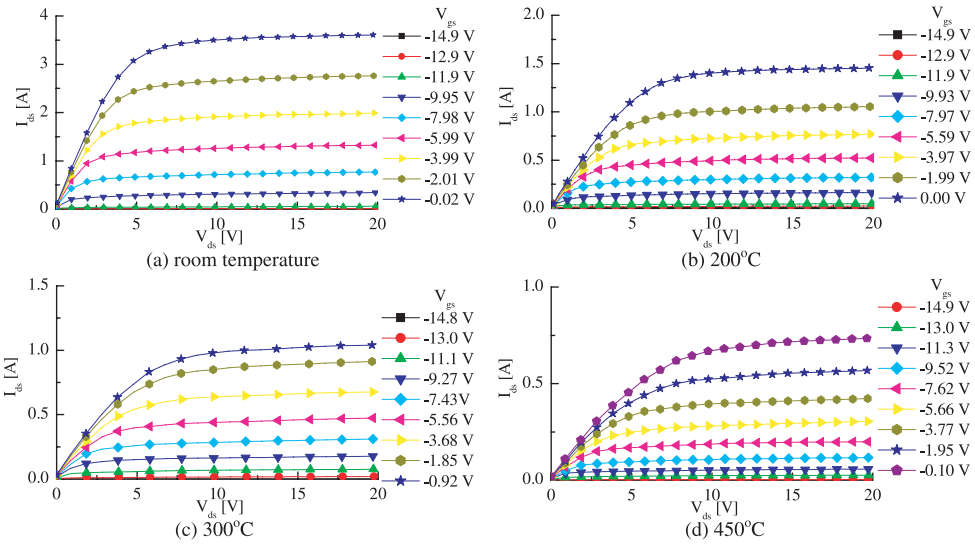

Fig. 2. DC characteristics of the SiC JFET as function of V_{gs}.

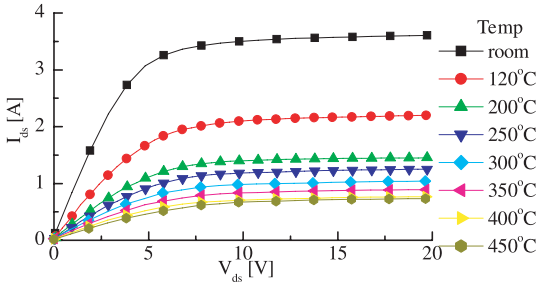

Fig. 3. Temperature dependency of the dc characteristics of the SiC JFET for $V_{gs} = 0$ V.

the linear region for $V_{gs} = 0$ V. The threshold gate voltage becomes slightly more negative to $V_{gs} = -15$ V.

Figure 3 shows the dc characteristics at $V_{gs} = 0$ V for different ambient temperatures. The saturation current decreases in accordance with increasing temperatures; such as 3.5 A at room temperature, 2.2 A at 120°C, 1.4 A at 200°C, 1.0 A at 300°C, and so on. The current reduction becomes smaller at high ambient temperatures. These results indicate that the JFET must be used with the rated current of 0.7 A when operated at 450°C. This figure also indicates that the voltage drop between the drain and source for an operation of 0.5 A changes from 0.7 V at room temperature to 6 V at 450°C leading to conduction losses at 450°C 10 times greater than those at room temperature. However, operation at these high temperatures for Si devices is impossible. The JFET does not require change of gate control since the threshold gate voltage changes by only a few volts, thus it is easy to use in high temperature applications.

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4 Conclusion

This paper investigated the characteristics of a SiC JFET under ambient temperature conditions from room temperature up to 450°C confirming its normal operation. The conventional plastic package cannot be exposed to such high temperatures; therefore the authors packaged the SiC JFET bare die into a thermally stable package. The packaged JFETs were evaluated at the wide ambient temperature range of operation. The measured dc characteristic results indicated that the available current ratings of the SiC JFET decrease with increasing temperatures. The current rating becomes 20% at 450°C with respect to that at room temperature. The threshold gate voltage changes slightly lower with increasing the temperature. However, it can be easily managed by offsetting the gate voltage a few volts higher (negative direction). The ability of extremely high temperature operation shown in this paper indicates that SiC devices hold promise for many applications.

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