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SiGe HMOSFET monolithic inverting current mirror

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Abstract

The authors present the first to their knowledge monolithic inverting current mirror fabricated on heterostructure Si/SiGe technology, using buried silicon channel depletion-mode MOSFET transistors. Characterisation results both at DC and at high frequencies prove that the technology is viable, with the circuit exhibiting remarkably high linearity while combining functionality usually achieved in III-V systems with the robustness and flexibility of a MOS platform. This emerging technology qualifies as an ideal candidate for the building of elemental analogue blocks, where tuning and exploitation of device properties will eliminate the need of further linearisation circuitry, which increases noise, complexity and power consumption. Furthermore, these circuits can also benefit from the high frequency bandwidth associated with strained silicon channels.

Keywords: Analogue electronics; MOSFETs; Semiconductor epitaxial layers; Si-Ge alloys

1. Introduction

It has been demonstrated that strained-silicon surface-channel n-MOSFETS, which use Si/SiGe heterojunctions, exhibit up to 70% enhanced mobility compared to their conventional silicon counterparts [1]. They represent a trend in non-classical CMOS and band-engineered transistors [2], they are compatible with the existing silicon fabrication lines and are bound to dominate the market in the near future. Given this and paying attention to the recent advances in heterojunction strained-silicon modulation-doped FETs (HMODFETs) [3], one has to realise that it is only a matter of time before buried-channel depletion-mode Si/SiGe heterojunction MOSFETs (HMOSFETs) also make their presence strongly felt. Despite this, not much has been published on such devices or, indeed, circuits. We have identified their importance for analogue electronics [4-6] and in this letter we present the first, to our knowledge, monolithic inverting current mirror fabricated with this technology. The circuit is simple and benefits from unrestricted low-voltage operation and large allowable signal swing, both of which are highly desirable characteristics in current mirrors and are not found in conventional CMOS designs, unless complicated architectures are employed [7].

2. Fabrication technology and transistor characteristics

The technology used to fabricate the circuit is detailed in [5]. Briefly, the heterostructure is grown on a SiGe “virtual substrate” [3] by molecular beam epitaxy (MBE). Then, the sites of the transistors constituting the current mirror are electrically isolated on-wafer by chemical etching. Finally, a standard silicon n-MOS sequence is applied for the completion of the fabrication process. During the MBE growth of the

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semiconductor structure, a heavier than in [5] arsenic doping within the SiGe donor layer, ensures depletion-mode operation.

The measured transfer characteristics of individual transistors are shown in figure 1. It is interesting to observe the characteristic double peaking of the transconductance curve, which can be attributed to the presence of mobile electrons not only in the channel but also within the SiGe donor layer itself. This results in a highly linear I_{DS} response versus V_{GS}. The zero gate-to-source bias point lies well within the linear regime of the transistor current curve. At the same point, the transconductance is close to its maximum value and the current is equivalent to 220 mA per millimetre of gate width.

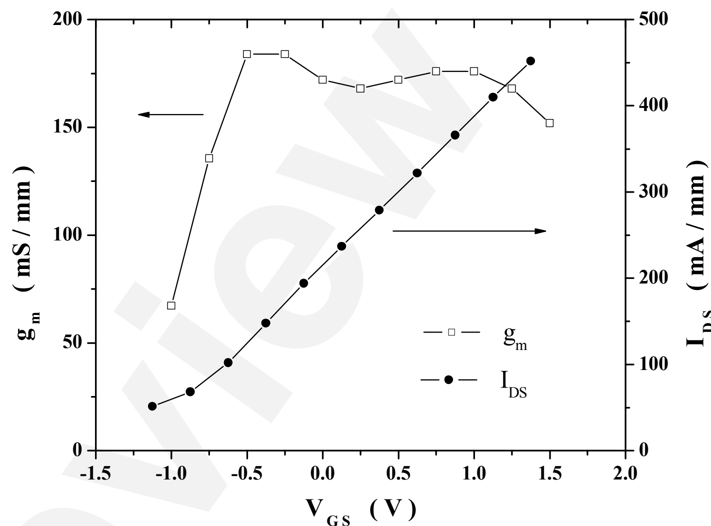

Fig. 1. Typical DC transfer characteristics of individual transistors at saturation. The gate length is 0.3 micrometers.

3. Circuit analysis, measurements and discussion

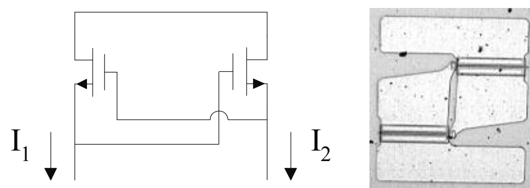

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Fig. 2. The current mirror schematic and an optical microscope image of the circuit. The individual device width is 100 micrometers and the gate length is 1 micrometer. The layout is compatible with RF on-wafer testing for the measurement of S-parameters.

Depletion mode transistors are often required in analogue circuits, where a "normally-on" state is achieved without additional biasing. In conventional CMOS processes this is adjusted using extra implantation steps, at the cost of mobility and speed. Alternatively, equivalent depletion-mode device operation can also be achieved with the inclusion of extra circuitry, at the cost of complexity, area and biasing/power requirements. The modulation doping technique, employed in our case, offers a clear advantage, with the transistors constituting the mirror being inherently normally-on. As the majority of conducting electrons flows within an "intrinsic" silicon layer, there is no mobility degradation, neither is extra circuitry required. Additionally, the transistors still employ a gate oxide, which prevents current leakage through the gate and at the same time allows positive voltage swings, as in normal MOSFETs.

The mirror schematic and a picture of the fabricated circuit are shown in figure 2. An earlier attempt to realize the circuit by wire-bonding discrete transistors is described in [8]. In this present work the circuit is for the first time implemented monolithically, with a layout which allows for RF on-wafer measurements, and in a more mature but not yet fully optimised technology.

The design has been devised for implementation on GaAs MESFET depletion-mode technologies [9]. It is classified as a negative and inverting current mirror. The "negative" notation means that the current mirror has a current source and not a current sink output, while the "inverting" shows that an increase in the input current gives a decrease in the output current.

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Assuming an ideal circuit consisting of a pair of identical square-law MESFETs, each with infinite output resistance and biased at saturation, the large-signal transfer response of the current mirror is:

$$\frac{I_{DS2}}{I_{DSS}} = \frac{I_{DS1}}{I_{DSS}} + 4\left(1 - \sqrt{\frac{I_{DS1}}{I_{DSS}}}\right) \quad (1)$$

The individual transistor current at saturation is:

$$I_{DS} = \frac{kW}{2}\left(V_{GS} - V_t\right)^2 \quad (2)$$

In the above expressions, I_{DSS} is the saturation current at zero V_{GS}, V_t is the threshold voltage and W is the transistor width. The cross-coupled connections between the transistor sources and gates of the circuit mean that $V_{GS1} = -V_{GS2}$. In the case of MESFETs, this imposes biasing constraints on the mirror, since the V_{GS} of the transistors should remain below +0.5 V, to avoid forward gate current breakdown. Obviously, this limitation does not apply in the case of SiGe HMOS transistors, which is another advantage of this particular technology compared to GaAs MESFET technology.

Although the input and output nodes of the current mirror are physically separate, their capacitances are combined in parallel, when looking into the small-signal equivalent circuit. This means that the ports of the current mirror should be regarded as a single node at RF. This particular feature has an impact on the frequency response, as can be seen from the expression for the small-signal AC current transfer characteristics:

$$\frac{I_2(j\omega)}{I_1(j\omega)} = \frac{j\omega C_o + g_{m2}}{j\omega C_o + \left(g_{m1} + g_{o1}\right)} \quad (3)$$

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where C_o is the combined capacitance and g_{o1} is the transistor output conductance at saturation. When the mirror is used in a feedback loop, as is usually the case, the combined capacitance minimizes the number of introduced poles and leads to increased stability margins and better dynamic response.

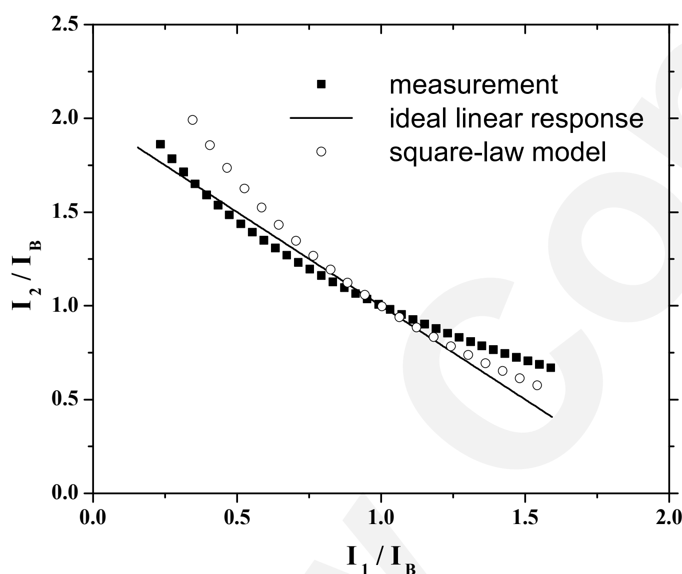

Fig. 3. The measured large-signal transfer response of the current mirror. The solid line corresponds to the ideal linear response. The open circles show the response of the circuit when this consists of textbook square-law MESFETs with infinite output resistance.

The SiGe HMOS current mirror was characterized both at DC and RF by on-wafer probing. Figure 3 shows the measured large-signal DC response of the circuit. The ideal linear behaviour and the response of a mirror consisting of ideal square-law MESFETs, are also included in the graph for comparison. I_B represents the state at which the currents in both branches of the inverting mirror are exactly equal. This is equivalent to the I_{DSS} of an ideal MESFET and in our case is equal to 2.2 mA. The response of the circuit is highly linear for a substantial part of the operating current range. This is due to the individual transistor I_{DS}-V_{GS} characteristics (figure 1). On-wafer S-parameter measurements were performed using a HP 8753D network

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analyser, in order to extract the current gain response (magnitude of H21 versus frequency). The frequency range scanned was from 100 kHz up to 2 GHz and the excitation power level was –30 dBm. The –3 dB point occurs at 200 MHz. This break frequency is half the transistor cut-off frequency f_T, because of the combined gate source capacitance effect mentioned earlier. But by no means does this relatively low frequency reflect the potential of the technology in question, as the specific fabrication run was based on non-optimised material and processing parameters and the transistor performance was poor to start with, the reasons being explained in [6]. It is also reminded that the gate length of the mirror transistors is 1 micrometer instead of the 0.3 micrometers of the stand-alone test devices.

Summarising, the circuit possesses the following key properties:

1. Ability to operate under low voltages, without the restrictions imposed by the threshold voltage in conventional silicon MOS technologies
2. It can endure large signal swings that are not permissible in competing MESFET-based technologies (e.g. gallium arsenide)
3. It has a current source effect with its constituting devices being n-type
4. It boasts inverting operation, offering the advantage of a decreasing output current with increasing current input
5. It benefits from high linearity, without the need of extra circuitry

4. Conclusion

The results of this paper suggest that heterostructure Si/SiGe MOSFET technology, which uses buried silicon channel depletion-mode devices, is a viable platform with huge potential in the field of analogue electronics. At present, this technology is still immature, compared to state-of-the-art commercial technologies, and its development has somehow been hindered by the fact that the starting material involves MBE

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growth on silicon. In that respect it would be unfair to compare it directly with commercial silicon CMOS technologies. But it is important to note that it potentially has the hallmarks to evolve to an enabling platform for specialised applications, where silicon compatibility, high bandwidth, high linearity, high sensitivity and low-voltage low-power operation are needed at the same time. A foreseeable such example includes biomedical engineering applications.

Acknowledgments

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FIGURE CAPTIONS

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