SiGe MMICs for Phased Array Radar Applications

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Abstract- This paper reports the performances of several broadband monolithic SiGe MMICs suitable for phased array radar applications. The amplitude and phase control MMIC designs are based on an optimized SiGe PIN diode offered by IBM 5-HP SiGe foundry process. Utilizing this diode, several control circuitries including a broadband (1-20 GHz) monolithic SPDT switch, a five port transfer switch, a 6-bit phase shifter, and a 5-bit attenuator, all operating over 7-11 GHz are designed. Also, the design and performance of a SiGe HBT variable gain cascode amplifier that combines the functionality of an amplifier and an attenuator into one MMIC is described.

I. Device Design

The IBM silicon-germanium technology permits the integration of advanced MMICs, low power VLSI digital electronics, and low frequency analog circuits in a single high yield process. The availability of several high performance microwave passive and active devices on the same wafer, including SiGe HBTs, PINs, and Varactors, etc., render the IBM SiGe technology a new and exciting paradigm for innovative circuit designs suitable for RF and microwave communication systems. Fundamental to the success of any microwave control function is a high performance PIN device. The performance of the PIN is dependent on its material doping profile as well as its layout. In the IBM 5HP SiGe process, the doping profile of the PIN diode is closely linked to that of the HBT through sharing of three HBT material layers, namely, the buried N+ sub-collector layer, the N-collector layer, and finally the P+ SiGe base layer. These layers have been used to form the cathode, the I region, and the anode of the PIN diode, respectively. The material profile in IBM 5HP process is optimized for achieving a high Ft HBT performance which somewhat limits its collector thickness, and consequently the PIN's I-region thickness to approximately half microns. Since the material profile of the PIN is rigid due to the HBT's performance requirements, the PIN layout design should be optimized to achieve optimum microwave performance. Figure 1 shows the layout of such a vertical optimized PIN design having a square anode contact that is surrounded by a continuous cathode contact. Such a device has a periphery-to-area ratio of only 0.56, an important design factor for minimizing the device forward bias microwave resistance (R_f).

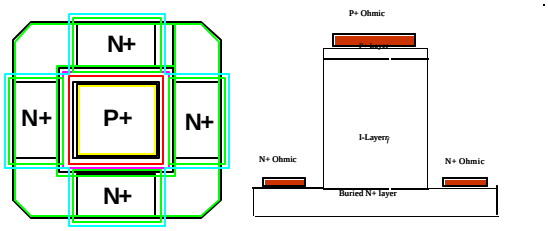


Fig.1. SiGe vertical PIN Diode (Dim: 7 *mm* x7 *mm*)

The forward bias resistance of the PIN diode (R_f) is the sum of the current independent contact resistance (Rc) and current dependent resistance (r_f), caused by the conductivity modulation of the intrinsic region. The current dependent resistance is due to the injection of the holes and electrons into the intrinsic region from the forward biased P^+ and N^+ contact regions. This resistance is given by:

$$r_f = \frac{l_i^2}{2\overline{m}tI_{dc}} \qquad (1)$$

Where:

l_i : Thickness of intrinsic region

$\overline{m}$: Average electron and hole mobility

t : Minority carrier life time

II. Device Performance

Fig. (2a) illustrates a fully fabricated 80 mm^2 shunt device in a 50 Ohm system. As it can be seen, the buried PIN is accessed by six vias that connect the device terminals to the input-output launching pads. The transmission lines are formed on a 15 microns thick polyimide layer that is deposited on the surface of the SiGe substrate. Good agreement has been obtained between the modeled and the measured dc current-voltage characteristics of the diode as shown in Figure 2(b, c). The diode follows a parallel plane diode behavior, given by equation (2), over seven orders of magnitudes.

$$I = I_s\left(\exp\left(\frac{qV}{nKT}\right)-1\right) \qquad (2)$$

The measured and modeled data on saturation current (Is), the ideality factor (n), and the junction revere breakdown voltage (Vb) are found to be: $I_s = 1.2\times10^{-17}$, $n = 1.1$ at $T = 300\,K^\circ$, and Vb=18 V. The value of (n) has a significant

effect on the performance of the PIN diode [1-2]. Figure (2d) illustrates the RF performances for typical 50 mm^2 and 80 mm^2 diodes when placed across or in series with 50 Ohm CPW input-output transmission lines. As can be seen, good broadband performance has been obtained for both series and shunt devices at a low dissipation power of 2.0 mW. Table below summarizes the extracted values for junction capacitance and the total forward biased resistance (R_f) for both devices.

PIN Area $(\mu m)^2$	IL (dB) @ 10 GHz	Iso.(dB) @ 10 GHZ	Cj(fF) @ -1V	Rf (Ω) Vf=1V
80 Shunt	0.5	18.0	32	3.5 @ 2 mA
50 Series	0.7	18.0	20	9.0 @ 2mA

The measured and modeled performance for a typical integrated series-shunt diode pair (50 mm^2 series, 80 mm^2 shunt) is shown in Fig. 2e. To achieve a broadband RF operation for this structure, the distance between the two diodes was set to approximately 10 mm , thereby minimizing its associated parasitics.

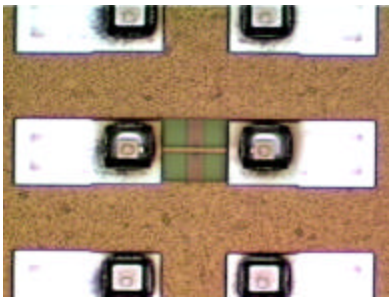


Fig. 2a. Shunt diode across 50 Ohm CPW lines

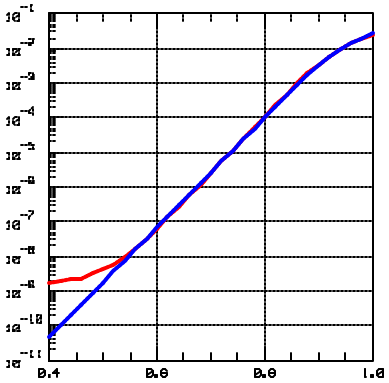


Fig. 2c. Log I (Amp) vs Voltage (V)

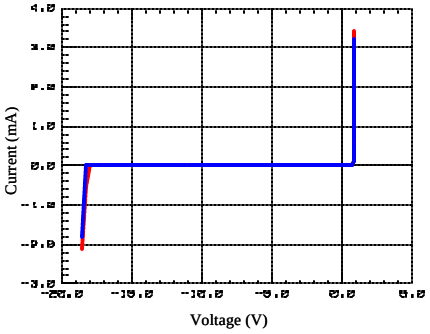


Fig. 2.b. DC IV characteristics

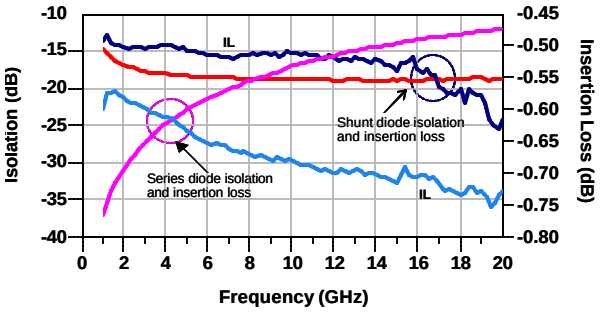


Fig. 2d. Microwave performance of series and shunt diodes. (If=2mA, Vf=1.0V, Vr=-1V)

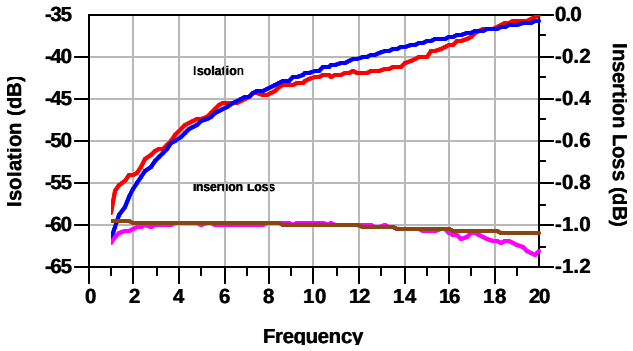


Fig. 2e. Measured & modeled performance of an integrated series-shunt diode. (If=2mA, Vf=1.0V, Vr=-1V)

III. Broadband (1-20 GHz) SPDT Switch

The series-shunt integrated diode structure described above was used to design a broadband SPDT switch with on-chip resistive biased networks that operates over 1-20 GHz bandwidth. All aspects of the circuit design and device modeling were performed using Agilent ADS simulators [3]. Figure 3(a) shows the SPDT switch schematic having a series-shunt diode combination in each arm. This topology was chosen as the best compromise between minimizing the insertion loss and maximizing the switch isolation. On-chip resistive bias networks were also employed to ensure broadband switching performance and smaller chip size as illustrated in Fig. (3b).

The 1500 Ohm bias resistors in this design use 340 ohms per square polysilicon thin film resistors and the MIM capacitors are based on 0.7 fF/ mm^2 thin dielectric film (SiO^2) capacitors. Referring to Fig.3 (a), a through-path between ports 1&2 exists when Vb2=-6.8V and Vb1=0, causing the series diode to become forward biased at 2 mA while the shunt diode is reversed biased. Similarly, an isolation path exists between ports 1&3 when Vb3 is set at (3.8 V, 2mA). The total dc power consumption for this design is only around 22 mW for a typical switch. As shown in Fig. (3c), a through-path loss of 0.9-1.3 dB and an isolation path loss of 60-40 dB over a wide frequency range (1-20 GHz) have been measured. Also shown is the close agreement obtained between the switch measured and simulated data. A similar chip without the on-chip resistive bias networks was also measured, requiring only 4.0 mW of dc power for maintaining the same switch performance. The input port power handling capability of the switch is shown in Fig. (3d) indicating the 1-dB insertion loss compression

point occurs at around 19 dBm when measured under the nominal bias condition described above. The switching speed and the third order intercept point are both evaluated at 10 GHz. The switching speed is found to be less than one nano-second and the third order intercept point around 30 dBm at -3 dBm input RF power.

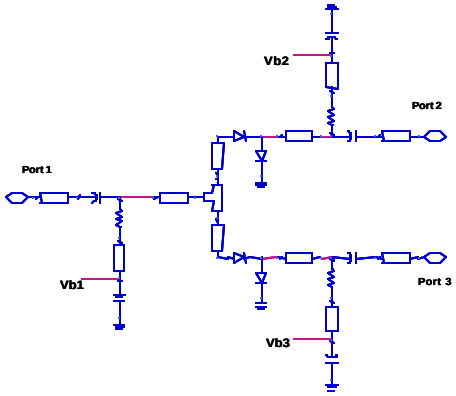


Fig. 3a. SPDT switch schematic

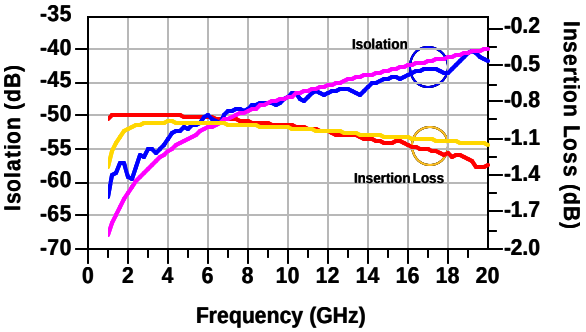


Fig. 3c. Measured and modeled switch performance

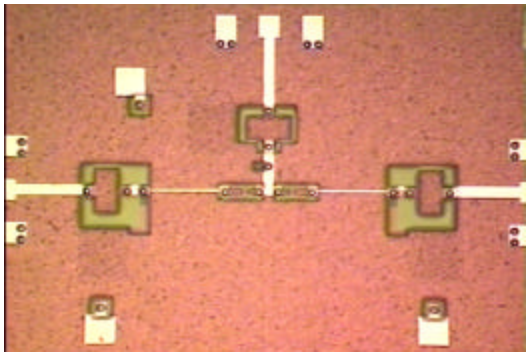


Fig. 3b. SiGe SPDT Switch chip (1.0mmx 0.42mm)

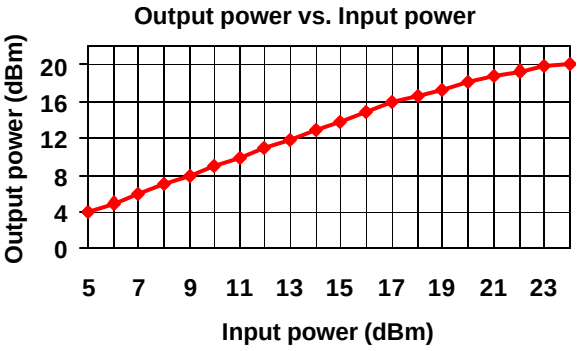


Fig. 3d. Switch input power 1-dB compression

IV. X-band SiGe MMICs

IBM's SiGe BiCMOS 5HP process offers the potential to integrate high levels of microwave circuitry with analog and digital circuits. Microwave functions traditionally performed by Gallium Arsenide MMICs can now be combined with the analog/digital functions of Silicon based ASICs on a single chip. As an example of higher microwave integration levels, several X-band SiGe MMICs, including a transfer switch, a 6-bit phase shifter, a 5-bit attenuator and a variable gain cascode amplifier is described in this section. The post SiGe topside process is described in details in section V.

Transfer Switch: Figure 4 (a) shows the circuit schematic of a 5-port Transfer switch containing 10 optimized SiGe PIN diodes. The circuit design is suitable for applications where Common Leg Circuit (CLC) architecture [4] is employed for the realization of phased array T-R modules. In the CLC topology, the transfer switch would enable the amplifier gain control and phase control circuitries to be shared by both transmit and receive signal paths. The switch design is based on a series-shunt 50 mm^2 diode combination as the best compromise between minimizing the insertion loss and maximizing the switch isolation. The simplicity of the circuit design is the result of the low parasitic capacitance and resistance of the SiGe PIN diodes leading to a compact chip size shown in Figure 4(b). The switch measured insertion loss, isolation, and return loss are shown in Figures 5 (a, b) respectively. The transfer switch demonstrates a path loss of 1.4-2.1 dB and an isolation of >55 dB across 7-11 GHz. The measured input and output return losses are better than 10dB over the same frequency band (Figure 5b).

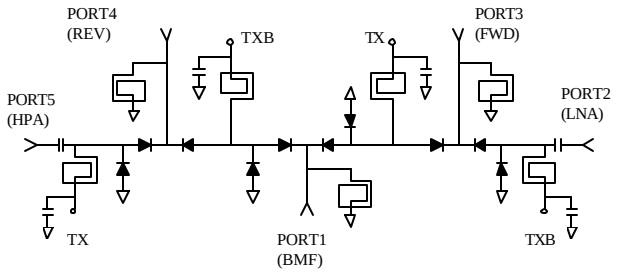


Fig. 4a. Transfer switch schematic

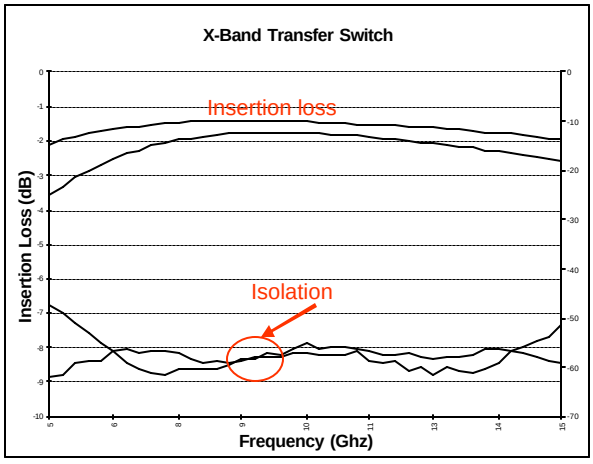
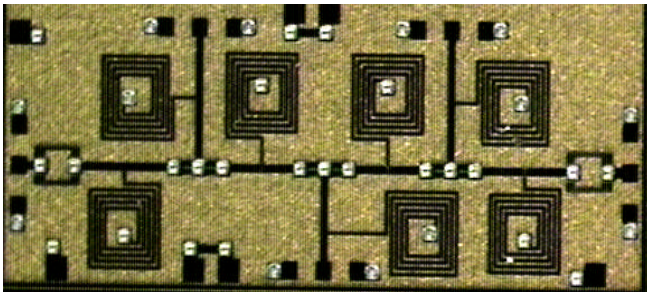


Fig. 5a. Switch measured insertion loss & isolation



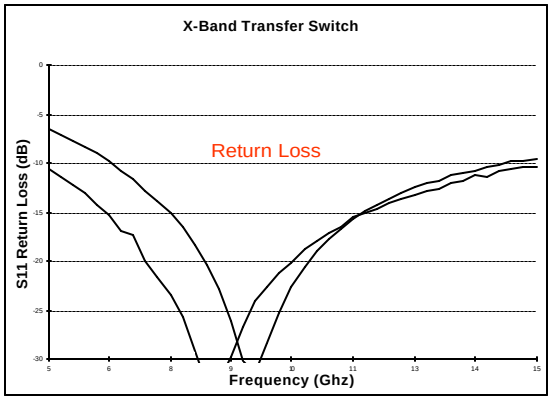


Fig. 4b. Transfer switch chip (3.2mmx 1.4 mm)

Fig. 5b. Switch measured return loss

6-bit Phase shifter: The phase shifter design consists of six digital bits (180, 90, 45, 22.5, 11.25, and 5.625 degrees) cascaded in a linear arrangement. This provides 64 phase states between 0 and 360 degrees in increments of 5.625 degrees. The 180, 90, 45, and 22.5 degree phase bits switch between PI and/or T-type high-pass/ low-pass phase shift networks using two single pole double throw PIN diode switches. The 11.25 and 5.625 degree phase bits use a simplified topology of capacitive and inductive elements to achieve their phase shifts [5]. These phase bit topologies are selected due to their broad bandwidth performance and relative insensitivity to process variations. The schematics for these phase bit circuits are shown in Figures 6 and 7.

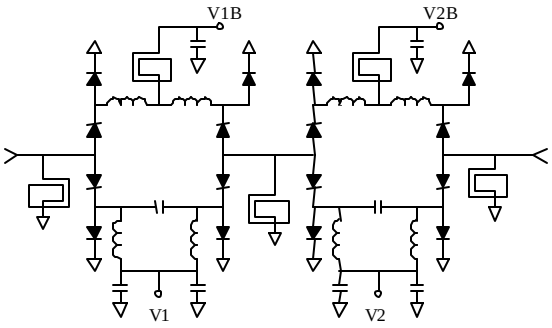


Fig. 6: 180 & 90 and 45 & 22.5 Phase 2-Bit Schematic

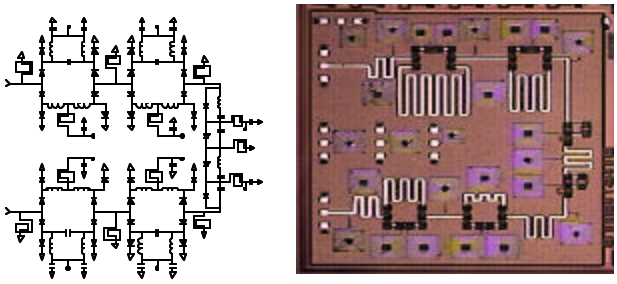


Fig. 8. 6-Bit Phase Shifter chip (3.8mm x 3.8mm)

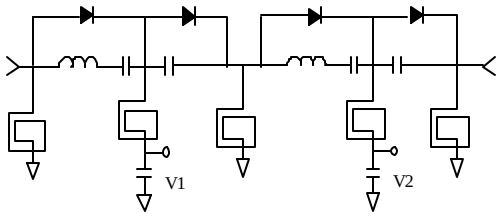


Fig. 7: 11.25 and 5.625 Phase Bit Schematic

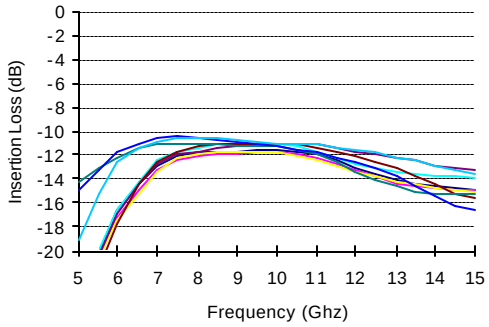


Fig. 9. Measured Phase Shifter Insertion Loss

SiGe PIN diodes (7μm x 7μm) are used for switching functions. Diode biasing is provided through spiral inductors in combination with MIM bypass capacitors. The 180, 90, 45, and 22.5 degree phase bits require two complementary bias inputs of ±1v. The 11.25 and 5.625 degree phase bits use the same voltages but require a single bias input. The completed 6-bit phase shifter chip and its associated circuit topology are shown in Figure 8. Programmable current sources were used

to bias each on-state diode at 2.5mA. Total current for the phase shifter was 45mA. Figures 9 through 11 summarize the measured performance of the primary phase states over 5 to 15 GHz, where 7 to 11 GHz is the design band. In the reference state, all phase bits were switched to their high-pass state. At 9 GHz, the measured output 1dB gain compression is 3dBm with a TOI of 17dBm. Post measurement simulations indicate that the overall circuit performance can be improved with additional topside technology improvement leading to improved circuit loss for spiral inductors, transmission lines, and Input/ Output (I/O) connections of the phase shifter.

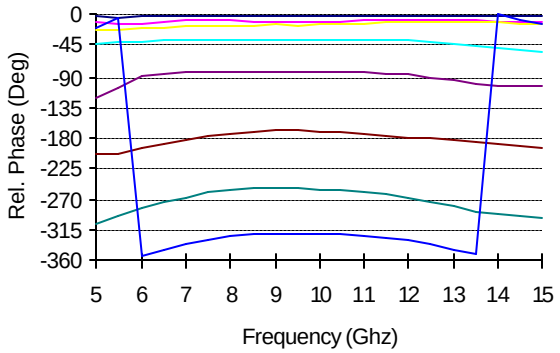


Fig. 10. Measured Phase Shifter Phase performance

(5.625, 11.25, 22.5, 45, 90, 180, 270, 355)

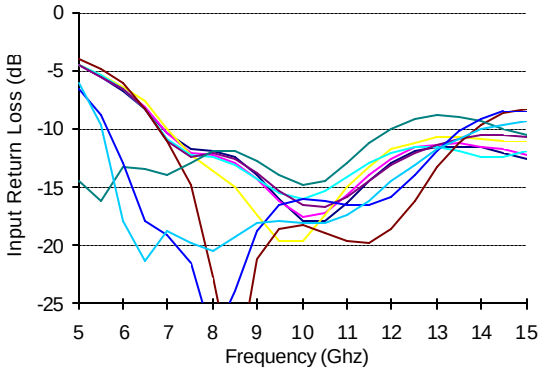


Fig. 11. Measured Phase Shifter Input Return Loss

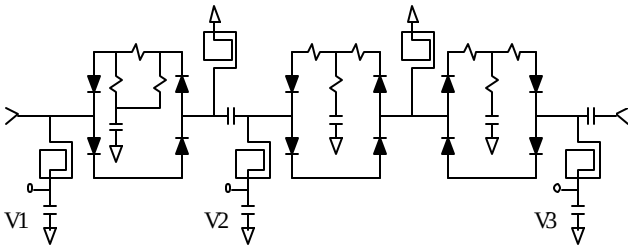
Attenuators: The optimized PIN diode described above is also used to design a 5-bit, 2-chips attenuator consisting of a 1, 2, 4, 8, and 16 dB attenuation bits. The 5-bit attenuator is divided into two cascadable designs, a 3 bit attenuator and a 2 bit attenuator to be used inter-dispersed between amplifier gain stages to optimize phased array radar system performance. The schematic of the two attenuator designs are shown in Figures 12 and 13. The attenuation bits are realized by two broadband single-pole double-throw (SPDT) switches that switch between a transmission line in the reference path and a resistive PI or T network in the attenuation path. The switched path design scheme was selected because of several highly desirable performance characteristics described below:

The attenuation performance is broadband and is mainly a function of the transmission lines and the resistive network, both of which are fairly independent of frequency. The attenuation performance is relatively insensitive to diode variations where changes in diode “ON” resistance affect both paths equally. The configuration also allows a simple

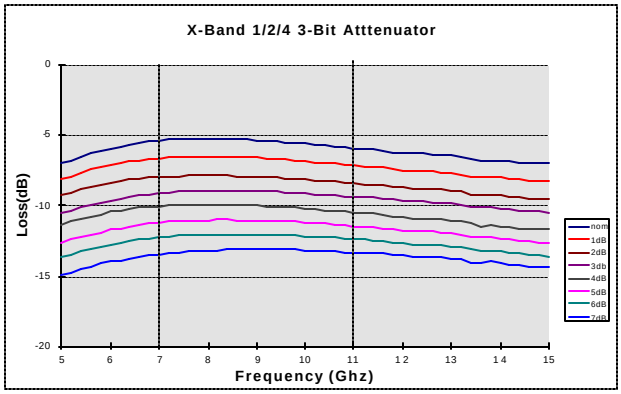
means to reduce the insertion phase difference between states. Characterizing the resistive network for phase shift, the transmission line in the reference path can be adjusted so that the phase shift is minimized.

The broadband SPDT switch used in the attenuator designs consists of a single series 50 mm^2 PIN diode in each arm. Additional diodes were not required for higher isolation due to the low off capacitance of the diodes, and the frequency band of operation. Resistive PI and T networks were selected because of their ability to provide good broadband 50ohm matches and easily realizable component values. All the resistors in the attenuator designs use 340ohms per square polysilicon resistors. Spiral inductors are used as RF chokes, together with 10pF MIM capacitors employed for PIN diode biasing. The spiral inductors provided effective low loss RF to DC isolation due to the topside processing and the ground plane shielding of the silicon substrate. The 10pF MIM capacitors are used in the designs to provide RF bypassing and DC blocking. The attenuator's bias scheme was selected to minimize the DC current and the size of the circuit layout.

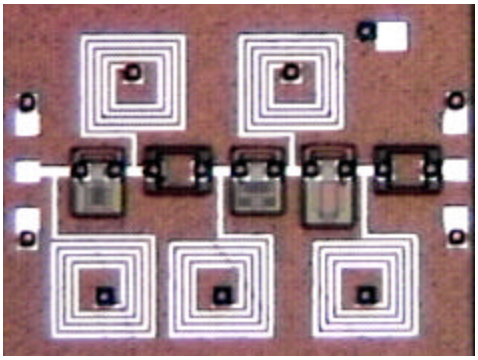
Figures 12-13 show the measured performance of the 3 bit (1, 2, and 4 dB) and 2 bit (8 and 16 dB) attenuator chips. All the attenuation bits show good relative attenuation performance.

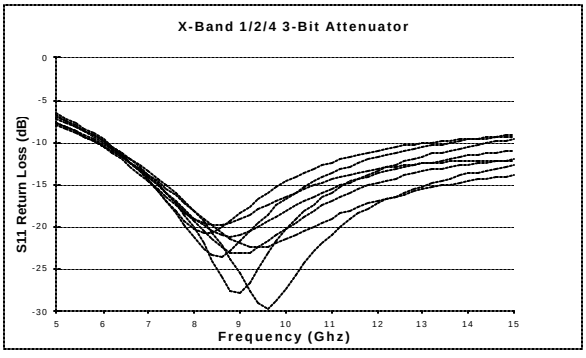


3 bit attenuator circuit schematic



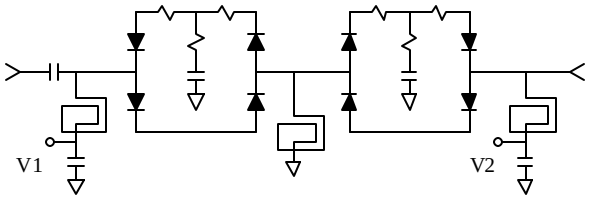
Measured attenuation



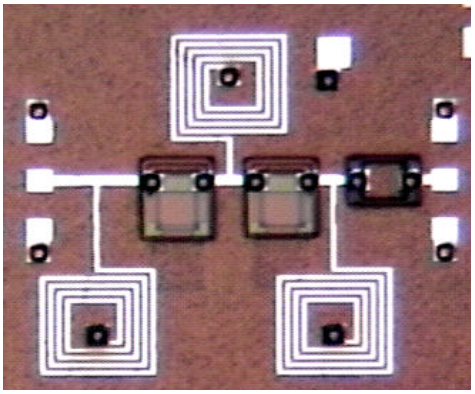


3 bit attenuator chip (1.8mm x 1.8mm) Measured return loss

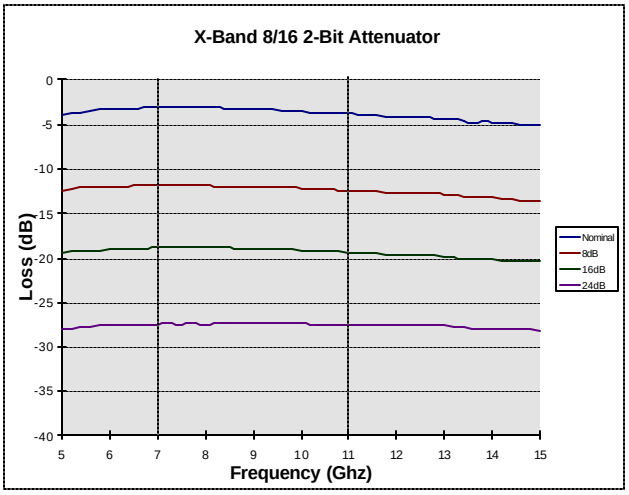
Fig.12. 3-bit SiGe PIN attenuator



2 bit attenuator circuit schematic



2 bit attenuator chip (1.3mm x 1.5mm)



Measured attenuation

Fig.13. 2-bit SiGe PIN attenuator

Cascode variable gain amplifier: In conventional radar systems, signal amplification and attenuation are generally accomplished by two separate circuits consisting of attenuator bits and amplifier gain blocks. In this section, we describe a more compact and efficient design technique that is based on a single chip HBT cascode amplifier.

The cascode amplifier is composed of two 0.5x20x10 μm^2 graded epitaxial base SiGe HBT NPN transistors having a f_T of 47 GHz and f_{max} of 70 GHz. The common-emitter, common-base configuration is modeled with two NPN transistors and

characterized as a single 3-terminal device at Vc = 4v and Ic = 100 mA. The G_{max} of the combined device is 29-25 dB in the 7-11 GHz frequency range. Gain control is achieved by adjusting the base bias of the common-base section. For the amplifier to exhibit good VSWR, it is important for the match of the composite device to remain invariant to the changes in base bias required to set the attenuation. The plot in Figure 14 shows the desired minimal change in S11* and S22* of the common-emitter, common-base 3-terminal configuration over the required bias conditions. The circuit schematic of Figure 15 shows the common-emitter, common-base cascode configuration of the variable gain amplifier. The benefits of using a cascode device include the inherent reduction of the Miller capacitance multiplication effect [6], which enhances the high frequency response of the amplifier, and provides a compact 2-stage structure. As shown in Figure 15, lossy matching techniques were used in designing the cascode amplifier which offers the benefits of low VSWR, flat gain, and compact chip size as shown in Figure 16. The lossy match networks also help stabilize the cascode device. Polysilicon resistors and MIM capacitor available in the SiGe process are used in the matching networks. The shunt spiral inductors function both as matching and bias networks.

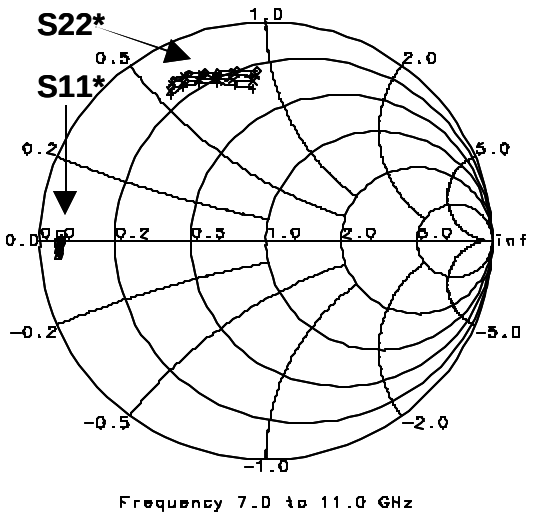


Fig. 14. S11* and S22* of common-emitter, common-base configuration at Vc=4.0v, Vb1=0.93v, Vb2=2.0~3.0v

The RF performance of the variable gain amplifier is evaluated by using on-wafer probe testing. An HP8510 network analyzer and a spectrum analyzer are used to characterize the small signal and TOI performance of the amplifier. The variable gain control performance of the amplifier is achieved by current limiting the common-base HBT in the cascode device.

In the 7-11 GHz band, the amplifier exhibited a maximum forward gain of 12.5 dB with 16 dB of gain control in steps of 1 dB. The gain control is achieved manually in an open loop configuration. The measured input and output return loss of the amplifier are found to be 7.5 dB and 12.5 dB respectively. The amplifier also achieved an output TOI of 21 dBm and an output P_{1dB} of 13 dBm at 8 GHz. The measurements are in agreement with the simulated amplifier performance. The variable gain performance of the amplifier is plotted in Figure 17. The forward insertion phase difference between maximum gain state and minimum gain state was measured to be –25 degrees. The phase delta between the maximum gain state and minimum gain state are plotted in Figure 18.

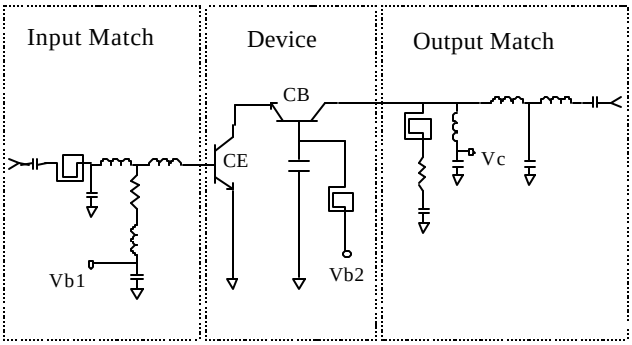


Fig. 15. Cascode amplifier circuit Schematic

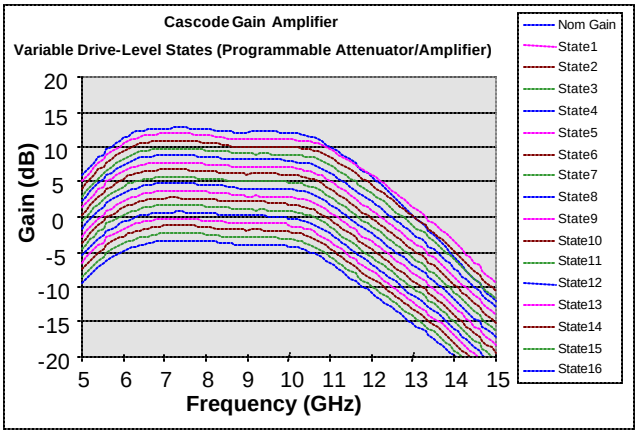


Fig. 17. Cascode amplifier variable gain performance

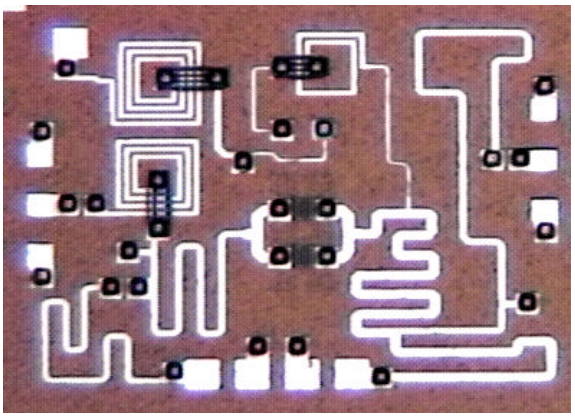


Fig. 16. Cascode amplifier chip (1.2mm x1.6 mm)

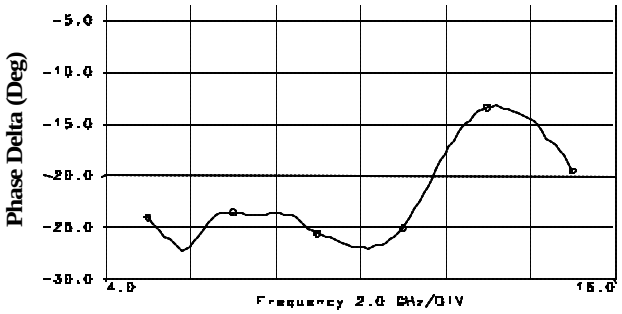


Fig. 18. Insertion phase delta between maximum and minimum gain states.

V. Topside Polyimide Technology

The present IBM SiGe BiCMOS IC process is based on conductive Silicon substrates. Therefore, to realize a low loss medium for transmission lines (TRLs), a topside polyimide process has been developed. In the standard IBM 5HP SiGe

process, there are five levels of AlCu interconnect metalization. The top-most layer of this metal system is used as a RF ground-plane for the microstrip transmission lines in a polyimide process. Such a ground-plane must have openings to allow connections between the TRLs above and the active and passive devices below.

The first step to create MMICs from the completed Si wafers is to deposit a polyimide layer on top of the ground-plane metalization layer (top metal). After polyimide deposition, vias are etched to contact devices below the ground plane. The polyimide thickness is 15 microns. Figure 19, shows the cross-sectional view of the IBM Si based MMICs using microstrip TRLs on polyimide. As shown in Figure 20, the transmission line loss for a typical 50 Ohm microstrip line on polyimide is about 1.20 dB/cm at 10 GHz.

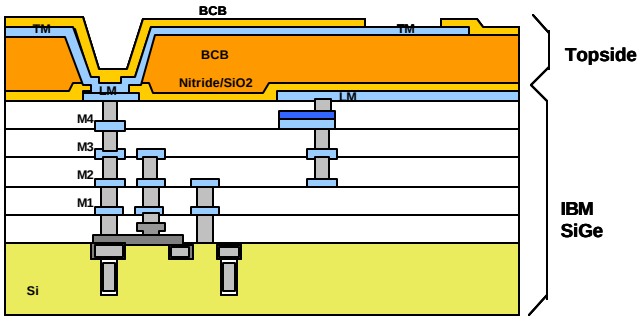


Fig.19. Cross-sectional view of the topside process

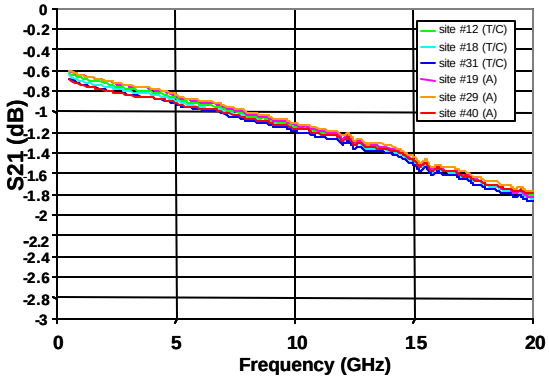


Fig.20. Loss vs frequency for 50 Ω, one Cm. TRLs on 15.0 microns polyimide

VI. Conclusion

The design and measured performance of several broadband SiGe MMICs including a broadband (1-20 GHz) monolithic SPDT switch, a five port transfer switch , a 6-bit phase shifter, and a 5-bit attenuator, all operating over 7-11 GHz are described. Also, the design and performance of a SiGe HBT variable gain cascode amplifier that combines the functionality of an amplifier and an attenuator into one MMIC is described. The amplitude and phase control MMIC designs are based on an optimized SiGe PIN diode. The broadband (1-20 GHz) resistive bias SPDT switch "ON" arm demonstrates a path-loss of less than 1.3 dB while its "OFF" arm maintains an isolation of greater than 40dB across 1-20 GHz while consuming only 22 mW of dc power. The switching speed, the 1-dB insertion loss compression point and the third order intercept point were found to be <1 nsec, 19 dBm, and 30.0 dBm respectively. The transfer switch is a five port

design containing 10 PINs and demonstrates a path loss of 1.4-2.1 dB across 7-11 GHz, the isolation over the same band is > 55 dB.

The 6-bit phase shifter design successfully demonstrates the feasibility of using SiGe technology for microwave phase control circuit designs. The 5-bit attenuator bits are realized by two broadband single-pole double-throw (SPDT) switches that switch between a transmission line in the reference path and a resistive PI or T network in the attenuation path. The X-band variable gain cascode amplifier design is based on IBM's SiGe HBTs. The amplifier has shown promising results as a variable gain amplifier. A maximum gain of 12.5 dB and a minimum gain of –3.5 dB has been achieved over 7-11 GHz. The input and output return loss of the amplifier is 7.5 dB and 12.5 dB respectively, over all the variable gain states. The availability high performance PIN diodes and other microwave devices including SiGe HBTs, Varactors, etc. renders the IBM SiGe technology a new and exciting paradigm for innovative circuit designs suitable for RF and microwave communication systems.

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