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Sigma-Z-Source Inverters

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***Abstract*— To increase the boost capability with minimum passive components, existing transformer based Z-source inverter (ZSI) topologies require the turn ratio to be increased. This results in larger transformer windings to be used in high dc-ac voltage gain applications. This shortcoming is addressed in this paper by introducing a sigma-Z-source inverter that improves the dc-ac voltage gain by reducing the turn ratio leading to a lower winding transformer. The proposed topology is compared with the TZ-source inverter as they used the same number of transformers and capacitors configured in an X-shaped network. The comparison shows that the sigma-Z-source inverter will have a higher dc-ac voltage gain at a turn ratio lower than 1.618 for a given shoot-through duty cycle allowing the use of smaller transformers. Simulation and experimental results have validated the effectiveness of the proposed sigma-Z-source inverter.**

***Index Terms*—Boost inversion ability, ΓZ-source inverter (ΓZSI), Sigma-Z-source inverter (ΣZSI), single-stage boost inverter, TZ-source inverter (TZSI), Z-source inverter (ZSI).**

I. INTRODUCTION

TRADITIONAL voltage source inverters (VSI) can only provide bucking mode during dc-ac inversion. Therefore, the input dc voltage fed to the VSI has to be greater than the ac output. Moreover, the gating of both semiconductors on a single leg of the inverter causes shoot-through that is undesirable. These shortcomings can be overcome by the Z-source inverter (ZSI) [1]. By cascading the Z-source network in front of the VSI, the inductors in the Z-source network are charged during the shoot-through period and the energy is released to the VSI during the active states. This boosts the dc-link voltage and provides a single stage buck-boost dc-ac power conversion. The ZSI has been used widely in applications such as photovoltaic system [2-4], electric drive [5, 6] and uninterrupted power supply [7]. Nevertheless, the traditional ZSI suffers from limitations such as limited boost capability, discontinuous input current and high inrush current.

Many research works to improve the conventional ZSI have been reported. They include the reduction of inrush current, lowering of components stress and improving of the input current profile [8, 9]. To improve the boost capability of the ZSI, works on the modulation techniques [10] and modifying of the Z-source network have also been investigated. The purpose of achieving higher dc-ac output voltage gain of ZSIs is to maximize the modulation index M to improve the power quality and reduce the semiconductors stress. One approach is to introduce passive components into the Z-source network such as the capacitor assisted quasi-ZSI [11], switched-inductor ZSI [12], and switched-inductor quasi-ZSI [13]. Moreover, these topologies allow cascading to achieve higher voltage gain [11, 14]. Although the boost capability is better, they are greater in size, higher in loss and cost due to additional use of passive components [15].

An alternative is to use a transformer in the Z-source network. The trans-ZSI, trans-quasi-ZSI and improved trans-ZSI have been proposed in [16-18] by replacing the inductors in the Z-source network with a transformer. The voltage gain of these single transformer based ZSI topologies is raised by increasing the turn ratio resulting in large transformer windings for high voltage gain applications. This shortcoming can be addressed by using the Γ-source network [19] that reduces the turn ratio to increase the voltage gain or the Y-source network [20] that allows optimal windings to be used by offering many combination of turn ratios to achieve the required voltage gain.

To further improve the boost capability in single transformer ZSI topologies, the TZ-source inverter (TZSI) [15] uses two transformers in the Z-source network. This allows lower turn ratio transformer to be used when compared to the T-source inverter, trans-ZSI and improved trans-ZSI. Similar to the single transformer based ZSI topologies, the turn ratio of the TZSI is raised to increase the voltage gain.

In this paper, an alternative topology of TZSI that overcomes the shortcomings of having high turn ratio to increase the boost capability is investigated. The new configuration is named sigma-Z-source inverter (ΣZSI). It is realized by shifting the secondary transformers' windings of the TZSI to be in series with the network capacitors forming two Γ-source

networks. Consequently, its boost capability can be increased by reducing the turn ratio of the transformers. Moreover, its transformer design is less sensitive to the turn ratio.

The performance of the proposed topology has been compared with the TZSI. Both approaches use two transformers and two capacitors in an X-shaped configuration to realize their source network. The study shows that the ΣZSI will achieve a higher dc-ac voltage gain at a turn ratio lower than 1.618 for a given modulation index and shoot-through duty cycle allowing lower winding transformers to be used. This results in smaller size and lower leakage transformers.

The proposed ΣZSI has been validated by simulation and experimental results. It is observed that the results match well with the theoretical analysis. The outline of this paper is as follows: In Section II the ΣZSI is introduced with circuit analysis on its achievable voltage gain. Section III compares the proposed ΣZSI with TZSI. Section IV reports the simulation and experimental results and Section V concludes this paper.

II. Proposed Sigma-Z-Source Inverter

Fig. 1 shows the proposed ΣZSI where two transformers are used to replace the inductors in the Z-source network. Different from the TZSI, the transformers' secondary windings W_{12} and W_{22} are in series with capacitors C_1 and C_2. This results in two Γ-source networks mirroring each other forming a sigma-source network.

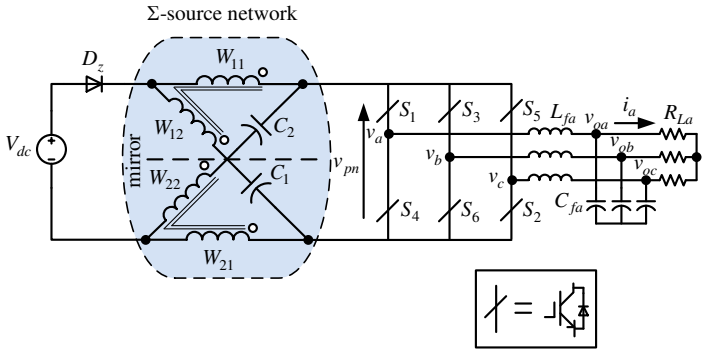

Fig. 1 Proposed sigma-Z-source inverter.

A. *Generalized Sigma-Z-source inverter*

The study of the dc source at different locations for the Z-source inverter (ZSI) has been reported in the literature [9, 15, 21]. In the improved ZSI [9], the position of the dc source is placed before and after the voltage source inverter (VSI) achieving reduced inrush capability and lower capacitor voltages stress. On the other hand, the embedded ZSI [21] position the dc source in front of the inductor in the Z-source network to smoothen the input source current. For transformer based ZSI, the dc source of the TZSI can be placed at locations like the improved ZSI and embedded ZSI to realize the similar characteristics [15].

Similar to the TZSI, the proposed ΣZSI can achieve the characteristics of the improved ZSI and embedded ZSI by changing the dc source position. Fig. 2 illustrates the three possible locations of the dc source.

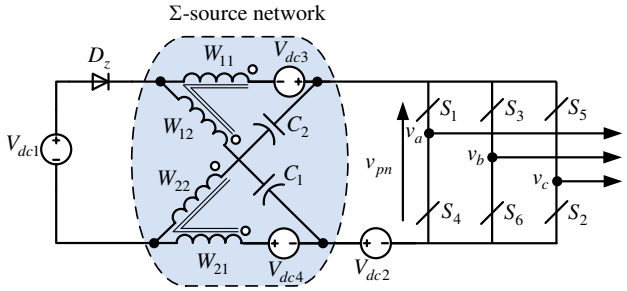

Fig. 2 Possible dc source location for the proposed sigma-Z-source inverter.

When the dc source is placed at V_{dc2}, the improved ΣZSI is realized with inherent soft start capability as the capacitor voltages of C_1 and C_2 are dependent on the shoot-through duty cycle. This reduces the inrush current of the dc source and VSI. Moreover, the voltage stresses on C_1 and C_2 are reduced by the dc source magnitude. When the dc source is placed at V_{dc3} or V_{dc4}, the embedded ΣZSI is realized that reduces the inrush current and reduces the voltage stress on one of the capacitors. Moreover, the dc source current becomes continuous. As the topology becomes asymmetrical, oscillation is observed at the capacitor voltage and the dc source current. To overcome this oscillation, the dc source can be divided equally and placed at both V_{dc3} and V_{dc4}.

B. Circuit analysis and achievable output voltage gain

Analogous to the traditional ZSI, the proposed ΣZSI has six active and two zero states during the buck mode. During the boost mode, the shoot-through state is introduced during the zero states to boost the dc-link voltage. In the sequel, the ΣZSI with the dc source at V_{dc1} presented in Fig. 1 is used for analysis without loss of generality. The two main operating states for the ΣZSI namely the shoot-through and non-shoot-through state are shown in Fig. 3(a) and 3(b) respectively.

During the shoot-through state, one or all the legs of the VSI are shorted causing the transformers' windings to charge through capacitors C_1 and C_2. Applying Kirchhoff's laws to the shoot-through state as shown in Fig. 3(a), the capacitor voltages V_{C1} and V_{C2} and currents i_{C1} and i_{C2} can be written by

$$\left.\begin{aligned} &-V_{Ci} - v_{Wi2(sh)} + v_{Wi1(sh)} = 0 \\ &i_{Ci(sh)} = i_{Wi2(sh)} = -i_{Wi1(sh)} \\ &i_{pn(sh)} = i_{sh} \quad i_{dc(sh)} = 0 \\ &i_{Wi1(sh)} = -i_{Wi2(sh)} / n_{\Gamma i} + I_{mi} \end{aligned}\right\} \text{for } i = 1,2 \tag{1}$$

where the subscript '*sh*' represents shoot-through state, v_{Wi1} and v_{Wi2} are the winding voltages, i_{sh} is the shoot-through current and $n_{\Gamma i} = W_{i1}/W_{i2}$ are the turn ratios of the transformers for $i = 1,2$.

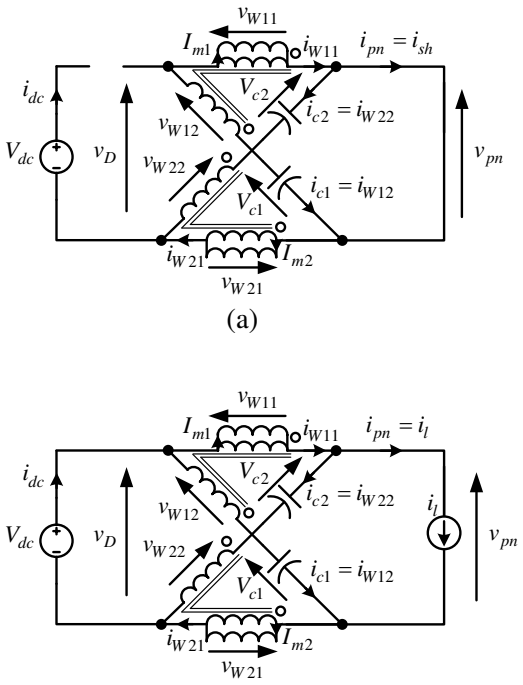

Fig. 3 Equivalent circuit of the sigma-Z-source inverter (a) shoot-through state, (b) non-shoot-through state.

During the non-shoot-through state, the diode is forward bias. The dc source charges the capacitors in parallel and is connected to the VSI in series with W_{11} and W_{21}. From Fig. 3(b), the following circuit equations can be written by

$$\left.\begin{aligned} &-V_{Ci} - v_{Wi2(non)} + v_{Wi1(non)} + v_{pn} = 0 \\ &-V_{dc} + v_{W12(non)} + V_{C1} + v_{W21(non)} = 0 \\ &-V_{dc} + v_{W11(non)} + V_{C2} + v_{W22(non)} = 0 \\ &i_{Ci(non)} = i_{dc(non)} - i_{Wi1(non)} = i_{Wi2(non)} \\ &i_{pn(non)} = i_l \quad i_{Wi1(non)} = -i_{Wi2(non)} / n_{\Gamma i} + I_{mi} \end{aligned}\right\} \text{for } i = 1,2 \tag{2}$$

where the subscript '*non*' represents non-shoot-through state.

Taking the average voltage for each transformer winding to be zero for (1) and (2), the following shoot-through and non-shoot-through winding voltages and capacitor voltages can be found by

$$\left.\begin{aligned} v_{Wi1(sh)} &= \frac{n_{\Gamma i}(1-D_0)/(n_{\Gamma i}-1)}{1-\left(2+\frac{1}{n_{\Gamma 1}-1}+\frac{1}{n_{\Gamma 2}-1}\right)D_0} V_{dc} \\ v_{Wi2(sh)} &= \frac{(1-D_0)/(n_{\Gamma i}-1)}{1-\left(2+\frac{1}{n_{\Gamma 1}-1}+\frac{1}{n_{\Gamma 2}-1}\right)D_0} V_{dc} \\ v_{Wi1(non)} &= \frac{-D_0 n_{\Gamma i}/(n_{\Gamma i}-1)}{1-\left(2+\frac{1}{n_{\Gamma 1}-1}+\frac{1}{n_{\Gamma 2}-1}\right)D_0} V_{dc} \\ v_{Wi2(non)} &= \frac{-D_0/(n_{\Gamma i}-1)}{1-\left(2+\frac{1}{n_{\Gamma 1}-1}+\frac{1}{n_{\Gamma 2}-1}\right)D_0} V_{dc} \end{aligned}\right\} \text{for } i = 1,2 \tag{3}$$

$$V_{C1} = V_{C2} = V_C = \frac{(1-D_0)}{1-\left(2+\frac{1}{n_{\Gamma 1}-1}+\frac{1}{n_{\Gamma 2}-1}\right)D_0} V_{dc} \tag{4}$$

By substituting (4) into (2), the peak dc-link voltage during the non-shoot-through state can be determined by

$$\hat{v}_{pn} = \frac{1}{1-\left(2+\frac{1}{n_{\Gamma 1}-1}+\frac{1}{n_{\Gamma 2}-1}\right)D_0} V_{dc} = BV_{dc} \tag{5}$$

where the notation B represents the boost factor of the ΣZSI. Since the operation of the proposed ΣZSI does not affect the output volt-second balance, the output peak ac phase voltage can be written by $\hat{v}_{ac} = MBV_{dc}/2$ where M is the modulation index of the VSI.

From (5), it can be observed that the ΣZSI has the following characteristics: *1)* the theoretical boost factor B becomes infinite if $\left(\frac{1}{n_{\Gamma 1}-1}+\frac{1}{n_{\Gamma 2}-1}\right)=(1-2D_0)/D_0$; *2)* the boost factor is increased by reducing the turn ratio of the transformers. This is different from other transformer based ZSIs [15-18]; *3)* the desirable turn ratio is kept to $1 < n_{\Gamma i} \le 2$ for i = 1 or 2 to reduce the number of windings of the transformers.

To reveal the relationship of the boost factor with respect to the shoot-through duty cycle and the transformer's turn ratio, we let the turn ratio of the two transformers to be equal by taking $(n_{\Gamma 1} = n_{\Gamma 2})$. Using (5), the boost ability of the proposed ΣZSI is illustrated in Fig. 4(a) by varying the turn ratio and duty cycle in steps of 0.01. From Fig. 4(a), it is observed that the voltage gain increases when the shoot-through duty cycle is increased or when the turn ratio is decreased. When the turn ratio is 1.4 and D_0 = 0.1, the boost factor is 3.33. When D_0 is increased to 0.12, the boost factor becomes 6.25, demonstrating the high boosting capability despite a small change in the shoot-through duty cycle.

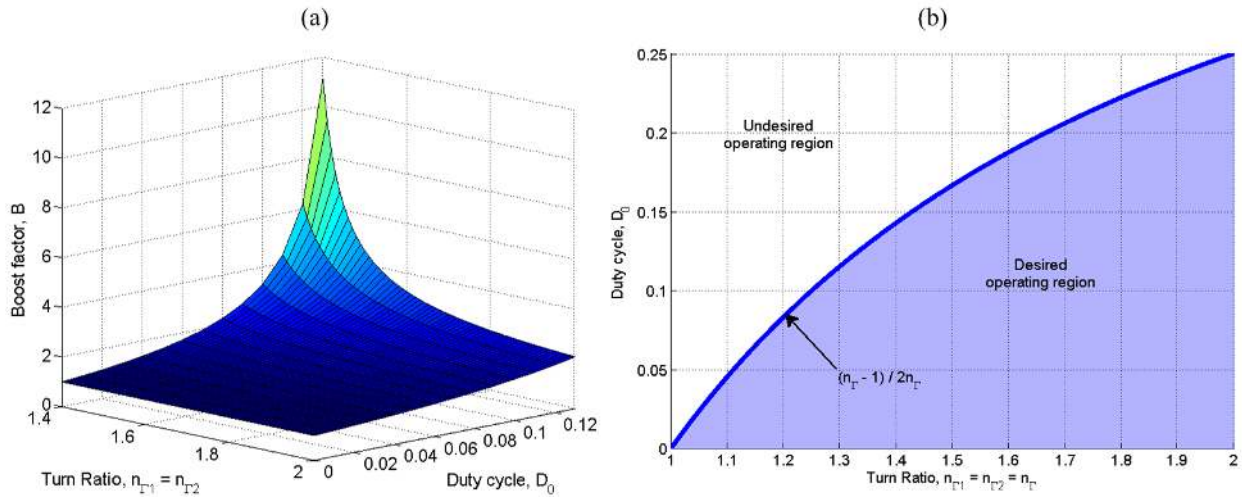

Fig. 4 (a) Boost ability and (b) desirable operating range of the proposed sigma-Z-source inverter with various turn ratio and duty cycle when $n_{\Gamma 1} = n_{\Gamma 2} = n_{\Gamma}$.

It is worthy to note that the proposed ΣZSI may exhibit negative gains for certain duty cycle and turn ratio. To protect the VSI from such cases, it is desirable to limit the duty cycle to be $0 < D_0 < 1\Big/\left(2+\frac{1}{n_{\Gamma 1}-1}+\frac{1}{n_{\Gamma 2}-1}\right)$ as shown in Fig. 4(b). From Fig. 4(b), it is observed that when the turn ratio decreases, the desired operating duty cycle range reduces. At low turn ratio, the ΣZSI becomes sensitive to the duty cycle that may cause it to operate at the undesired region.

Since the proposed ΣZSI uses the shoot-through states to achieve the boost capability, pulse width modulation (PWM) techniques that are suitable for the traditional ZSI can also be used [10, 22]. For this study, the shoot-through duty cycle is set as $D_0 = (1-M)$ to have a high modulation index M to improve the output power quality [12, 15]. Thus, the ratio of the input to output voltage gain $G=MB$ of the ΣZSI in (5) over the traditional ZSI can be derived by

$$\frac{G_{\Sigma ZSI}}{G_{ZSI}} = \frac{MB_{\Sigma ZSI}}{MB_{ZSI}} = \frac{1-2(1-M)}{1-\left(2+\frac{1}{n_{\Gamma 1}-1}+\frac{1}{n_{\Gamma 2}-1}\right)(1-M)} \tag{6}$$

where the subscripts 'ZSI' and 'ΣZSI' represent the traditional ZSI and ΣZSI respectively. From (6), it can be determined that the dc-ac output voltage gain of the ΣZSI achieves a higher dc-ac voltage gain over the traditional ZSI when $1 < n_{\Gamma i} < \infty$ for i = 1 and 2.

With a higher boost capability, the voltage stress across the switching devices can be reduced. The cost that the ZSI has to pay to achieve the voltage boost can be measured by the ratio of the voltage stress to the equivalent dc voltage GV_{dc} [10]. Using (5), the voltage stress to equivalent dc voltage ratio of the proposed ΣZSI can be expressed by

$$\frac{V_S}{GV_{dc}} = \frac{BV_{dc}}{GV_{dc}} = \frac{1}{1+\frac{1}{n_{\Gamma 1}-1}+\frac{1}{n_{\Gamma 2}-1}}\left(2+\frac{1}{n_{\Gamma 1}-1}+\frac{1}{n_{\Gamma 2}-1}-\frac{1}{G}\right) \tag{7}$$

From (7), the voltage stress of the proposed ΣZSI with the voltage gain G varied from 1 to 10 is illustrated in Fig. 5. It is observed that the voltage stress is lower for the proposed ΣZSI as compared to the traditional ZSI for the same voltage gain.

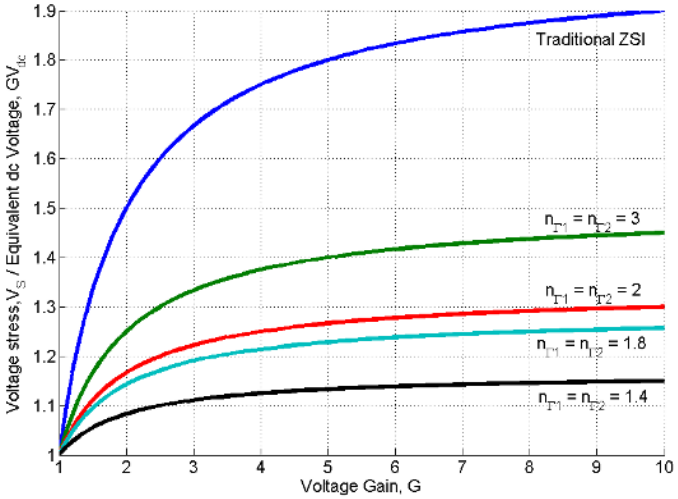

Fig. 5 Voltage stress of proposed sigma-Z-source inverter with various turn ratios.

III. SIGMA-Z-SOURCE INVERTER VERSUS TZ-SOURCE INVERTER

A summary of the dc-ac voltage gain, component voltage and peak current stress of transformer based ZSIs reported in the literature are presented in Table I. Among the methods, the TZSI and the proposed ΣZSI use two transformers.

Table I Summary of dc-ac voltage gain, peak voltage and current stress requirements for different topologies

	Proposed Sigma-ZSI	TZSI [13]	Trans-ZSI [15]	Traditional ZSI [1]
V_{C1}	$\frac{(1-D_0)V_{dc}}{1-\left(2+\frac{1}{n_{\Gamma1}-1}+\frac{1}{n_{\Gamma2}-1}\right)D_0}$	$\frac{(1-D_0)V_{dc}}{1-(2+N_1+N_2)D_0}$	$\frac{nD_0V_{dc}}{1-(1+n)D_0}$	$\frac{(1-D_0)V_{dc}}{1-2D_0}$
V_{C2}	$\frac{(1-D_0)V_{dc}}{1-\left(2+\frac{1}{n_{\Gamma1}-1}+\frac{1}{n_{\Gamma2}-1}\right)D_0}$	$\frac{(1-D_0)V_{dc}}{1-(2+N_1+N_2)D_0}$	N.A.	$\frac{(1-D_0)V_{dc}}{1-2D_0}$
$\hat{v}_{ac}$	$\frac{MV_{dc}/2}{1-\left(2+\frac{1}{n_{\Gamma1}-1}+\frac{1}{n_{\Gamma2}-1}\right)D_0}$	$\frac{MV_{dc}/2}{1-(2+N_1+N_2)D_0}$	$\frac{MV_{dc}/2}{1-(1+n)D_0}$	$\frac{MV_{dc}/2}{1-2D_0}$
$\hat{v}_D$	$\frac{-(n_{\Gamma1}n_{\Gamma2}-1)V_{dc}/(n_{\Gamma1}-1)(n_{\Gamma2}-1)}{1-\left(2+\frac{1}{n_{\Gamma1}-1}+\frac{1}{n_{\Gamma2}-1}\right)D_0}$	$\frac{-(1+N_1+N_2)V_{dc}}{1-(2+N_1+N_2)D_0}$	$\frac{-nV_{dc}}{1-(1+n)D_0}$	$\frac{-V_{dc}}{1-2D_0}$
I_{dc}	P_o/V_{dc}	P_o/V_{dc}	P_o/V_{dc}	P_o/V_{dc}
I_m	$I_{mi}=I_{dc}$	$I_{mi}=(1+N_i)I_{dc}$	$(1+n)I_{dc}$	N.A
$\lvert\hat{I}_L\rvert$	$\hat{I}_{W1i}=\frac{n_{\Gamma1}}{n_{\Gamma1}-1}I_{dc}$ $\hat{I}_{W2i}=\frac{n_{\Gamma2}}{n_{\Gamma2}-1}I_{dc}$	$\hat{I}_{Wi1}=(1+N_i)I_{dc}$ $\hat{I}_{Wi2}=\frac{I_{dc}}{(1-D_0)}$	$\hat{I}_{W1}=(1+n)I_{dc}$ $\hat{I}_{W2}=\frac{I_m-i_l}{n}$	$I_{L1}=I_{L2}=I_{dc}$
$\hat{I}_{sh}$	$\left(\frac{n_{\Gamma1}}{n_{\Gamma1}-1}+\frac{n_{\Gamma2}}{n_{\Gamma2}-1}\right)I_{dc}$	$(2+N_1+N_2)I_{dc}$	$(1+n)I_{dc}$	$2I_{dc}$

$\hat{v}_{ac}$ is the peak ac phase output voltage, $\hat{v}_D$ is the peak diode voltage, I_m is the average magnetizing current, $\hat{I}_L$ is the average peak winding or inductor currents, $\hat{I}_{sh}$ is the average peak shoot-through current, I_{dc} is the average dc current, P_o is the output power of the inverter, n is the turn ratio for trans-ZSI and N_i is the turn ratio for TZSI for $i=1,2$.

The source network of the TZSI [15] consists of two transformers and two capacitors connected in an X-shaped configuration as shown in Fig. 6(a). On the other hand, the proposed Σ-source network is realized by having the secondary windings of the TZ-source network to be in series with capacitors C_1 and C_2 as illustrated in Fig. 6(b).

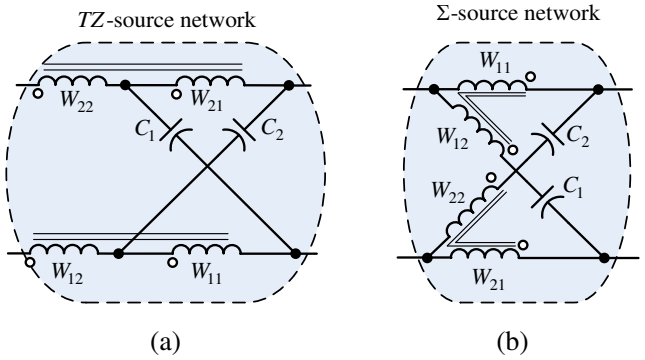

Fig. 6 Source network of (a) TZ-source inverter [15] and (b) proposed sigma-Z-source inverter.

From Fig. 6, it is observed that the TZ-source network uses the same components as the proposed Σ-source network. Therefore, it is used for the comparative study.

A. Effect of turn ratio on dc-ac voltage gain

For a fair comparison between TZSI and the proposed ΣZSI, the shoot-through duty cycle and modulation index are set to be the same. Mathematically, they can be written by

$$\begin{aligned} M_{TZSI} &= M_{\Sigma ZSI} = M \\ D_{0,TZSI} &= D_{0,\Sigma ZSI} = D_0 \end{aligned} \tag{8}$$

where the subscripts are added to distinguish TZSI from ΣZSI. By substituting (8) into the dc-ac voltage gains of ΣZSI and TZSI in Table I and equating them to be the same, the turn ratio of ΣZSI $n_{\Gamma i}$ in terms of the turn ratio of TZSI N_i is given by

$$\begin{aligned} \left.\frac{\hat{v}_{ac}}{V_{dc}}\right|_{\Sigma ZSI} &= \left.\frac{\hat{v}_{ac}}{V_{dc}}\right|_{TZSI} \\ \frac{1}{n_{\Gamma i}-1} = N_i \Rightarrow n_{\Gamma i} &= \frac{N_i+1}{N_i} \quad \text{for } i = 1,2 \end{aligned} \tag{9}$$

The turn ratio versus dc-ac voltage gain for TZSI and ΣZSI are illustrated in Fig. 7. The study is conducted for different shoot-through duty cycles with the dc-ac voltage gain varied from 0 to 5. The solid line and dotted line represent the turn ratios of the TZSI and ΣZSI respectively.

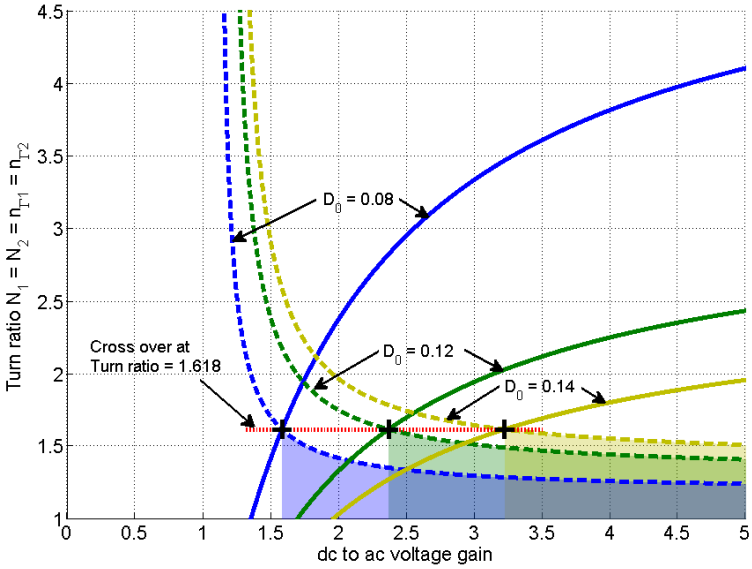

Fig. 7 Turn ratio versus dc-ac voltage gain comparison of TZ-source inverter (solid line) and sigma-Z-source inverter (dotted line) for different shoot-through duty cycles and $M = (1\text{-}D_0)$.

From Fig. 7, it is observed that when the shoot-through duty cycle is increased, the dc-ac voltage gains of both TZSI and ΣZSI are increased. To increase the dc-ac voltage gain at a given duty cycle, the turn ratio for the TZSI has to be increased while the ΣZSI is decreased. By solving (9) with $n_{\Gamma i} = N_i$ yields 1.618 which is the turn ratio of the cross over points in Fig. 7 indicated by the '+' markers. By substituting the turn ratio of 1.618 to the voltage gain of the ΣZSI, the dc-ac voltage gain at the cross over points is calculated by $M/(1-5.236D_0)$. Thus, to achieve a smaller transformer design than the TZSI, the transformer turn ratio must be less than 1.618 and the operating voltage gain must be greater than $M/(1-5.236D_0)$ which is indicated by the shaded areas in Fig. 7.

B. Transformer window area with equal dc-ac voltage gain

The transformer's core window area is proportional to the core geometry that is important in sizing the transformer. If the transformer window area is minimized, the transformer size can be reduced given that the power capability requirement is met. The amount of reduction varies differently depending on the core type. For a transformer core, its window area is fully utilized when [23]

$$K_u W_a = W_{pri}\left(1+\frac{W_{sec}}{W_{pri}}\right)A_w \tag{10}$$

where K_u is the utilization factor, W_a is the window area of the core calculated using the manufacturer's specification, W_{pri}, W_{sec} are the primary and secondary transformer's windings. A_w is the conductor area used for the windings assuming the conductor for the primary and secondary windings are the same. Ideally, the utilization factor should be one. Due to factors such as conductor insulation, method used to lay the conductor and workmanship, the usable window area is reduced. From [23], a good approximation of K_u is 0.4.

For comparison, the TZSI and ΣZSI transformers' turn ratios, their shoot-through duty cycle, modulation index, dc-ac voltage gain and number of primary windings are taken to be equal given by

$$\left.\begin{aligned} &M_{TZSI} = M_{\Sigma ZSI} = M \\ &D_{0,TZSI} = D_{0,\Sigma ZSI} = D_0 \\ &n_{\Gamma 1} = n_{\Gamma 2}, N_1 = N_2 \\ &W_{pri}\big|_{TZSI} = W_{pri}\big|_{TZSI} = W_{pri} \end{aligned}\right\} \text{for } \frac{\hat{v}_{ac}}{V_{dc}}\bigg|_{\Sigma ZSI=TZSI} \tag{11}$$

By substituting (11) and the dc-ac voltage gain of the ΣZSI and TZSI from Table I into (10), the window area required for the turn ratio of the ΣZSI and TZSI can be obtained by

$$\begin{aligned} W_a\big|_{TZSI} &= \frac{A_w W_{pri}}{K_u}\left(\frac{G-M}{2GD_0}\right) \\ W_a\big|_{\Sigma ZSI} &= \frac{A_w W_{pri}}{K_u}\left(\frac{2GD_0}{G-M-2GD_0}+2\right) \end{aligned} \tag{12}$$

The amount of window area saving that ΣZSI can achieve over TZSI due to reduction in turn ratio is obtained by taking the difference of equations in (12). The amount of window area saving for several shoot-through duty cycles with the dc-ac voltage gain varied from 2 to 5 is shown in Fig. 8.

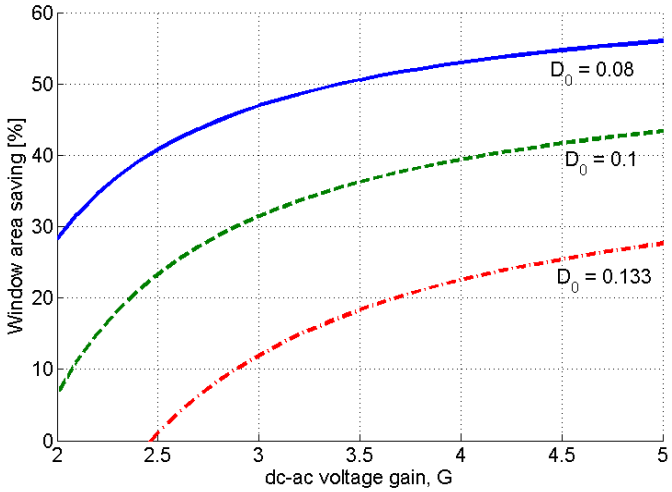

Fig. 8 Transformer core window area savings that the sigma-Z-source inverter can achieve over TZ-source inverter for different shoot-through duty cycle.

From Fig. 8, it is observed that the window area saving is greater if the dc-ac voltage gain is increased and when the shoot-through duty cycle is reduced. For example, the reduction of window area is about 30 % for a shoot-through duty cycle of 0.1 at a dc-ac voltage gain of 3.

C. Passive components and semiconductor stress

The voltage and current stress for components used in the TZSI and ΣZSI can be compared by substituting (8) into the equations of ΣZSI in Table I. Based on the resultant expressions, the capacitors voltage stress, diode voltage stress, peak average primary winding currents and shoot-through current are identical. The differences in component stress are the magnetizing current and secondary winding currents given by

$$\begin{cases} I_{m,\Sigma ZSI} = I_{dc} \\ I_{m,TZSI} = (1+N_i) I_{dc} \\ \hat{I}_{Wi2,\Sigma ZSI} = \hat{I}_{Wi2,\Sigma ZSI(sh)} = (1+N_i) I_{dc} \\ \hat{I}_{Wi2,TZSI} = \hat{I}_{Wi2,TZSI(non)} = \dfrac{I_{dc}}{(1-D_0)} \end{cases} \tag{13}$$

From (13), the magnetizing current for ΣZSI is smaller than TZSI by a factor of $(1+N_i)$. A lower magnetizing current prevents saturation of the transformer that may cause overcurrent in the system [24]. In addition, the average peak current of the secondary windings for the ΣZSI are greater than the TZSI. For the TZSI, the current at the secondary windings are zero during the shoot-through state and the peak current occurs at the non-shoot-through state resulting in lower current stress. For the ΣZSI, its secondary windings are in series with the network capacitors that are subjected to similar peak current as the primary windings during the shoot-through state. This results in zero dc current through the primary windings which prevent the shifting of hysteresis cycle towards the saturation region.

IV. Simulation and Experimental Results

The theoretic analysis of the ΣZSI is first validated using PowerSim. To reduce the voltage stress of the capacitors and achieve good grounding between the input dc source and the VSI, the discontinuous current quasi-ΣZSI (qΣZSI) that is derived from Fig. 2 with the dc voltage source placed at V_{dc2} is used. The simulation and experimental parameters are shown in Table II. These parameters are not optimized design but are components that are available in the laboratory.

Table II
Simulation and experimental parameters

Parameters	Value / Part number
DC source, V_{dc}	50 V
Fundamental AC frequency, f	50 Hz
Switching frequency, f_S	10 kHz
Capacitors C_1 and C_2	1000 μF from Vishay
Transformer cores	T102/66/15-3C90 from Ferroxcube
Voltage source inverter	PS21A7A from Powerex
Input diode, Dz	DSEI60 from IXYS
Output ac LC filter	4 mH, 15 μF
Output Y-connect load, R_L	100 Ω/phase

The choice of 50 V input dc voltage is to simulate the operation of the ΣZSI in low voltage renewable source applications. An intelligent power module (IPM) PS21A7A is used as the VSI. The short circuit current protection for the IPM is set to 127 A so that shoot-through states can be introduced without triggering the short circuit protection. Four transformers have been constructed using Litz wire and hand winded onto a T102/66/15-3C90 core from Ferroxcube. The measured primary leakage inductances are 8.43 µH and 4.83 µH for the transformers with a turn ratio of 2 and 1.5 respectively. They are shown in Table III. From Table III, the transformer with a turn ratio of 1.5 has a lower leakage inductance due to lesser number of windings [25-27]. This reduces the voltage drop. The experimental circuit is shown in Fig. 9. The modulation technique in [22] with a 10 kHz switching frequency is implemented using a dSpace DS1104 board.

Table III
Transformer parameters in simulation and experiment

Turn Ratio	Primary Magnetic Inductance	Leakage inductance referred to primary side
80:40	10.67 mH	8.43µH
60:40	7.54 mH	4.83µH

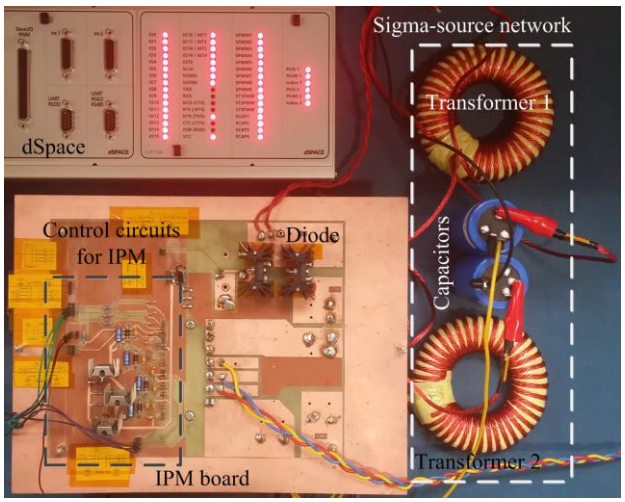

Fig. 9 Experimental circuit of the proposed sigma-Z-source inverter.

In this study, three simulation and experimental scenarios have been conducted as shown in Table IV. For case 1, a turn ratio of 2 is used for both transformers with M = 0.843 and D_0 = 0.157. In case 2, the transformers are replaced with turn ratio of 1.5 and the modulation index is increased to 0.9 while the shoot-through duty cycle is reduced to 0.1. With a smaller turn ratio and shoot-through duty cycle, the same dc-ac voltage gain in case 1 is achieved. In case 3, one transformer with a turn ratio of 2 and the other with a turn ratio of 1.5 is demonstrated. By maintaining the dc-ac voltage gain to be similar as in cases 1 and 2, the winding currents of both transformers are studied to observe the current stress due to the change in turn ratio.

Table IV
Simulation and experimental cases

	n_{T1}	n_{T2}	M	D_0
Case 1	2.0	2.0	0.843	0.157
Case 2	1.5	1.5	0.900	0.100
Case 3	2.0	1.5	0.877	0.123

Fig. 10 presents the simulation and experimental results for case 1. It is observed that the simulated and experimental windings and diode currents are similar. The capacitor and dc-link voltages are boosted to 60 V and 130 V in simulation while the experimental results are 51 V and 122 V respectively. Moreover, the output peak to peak line voltage is 191 V in simulation while the experimental measured value is 185 V. Using 100 Ω/phase resistors connected in ywe configuration, the simulated peak to peak line current is 1.1 A and is close to the experimental value of 1 A.

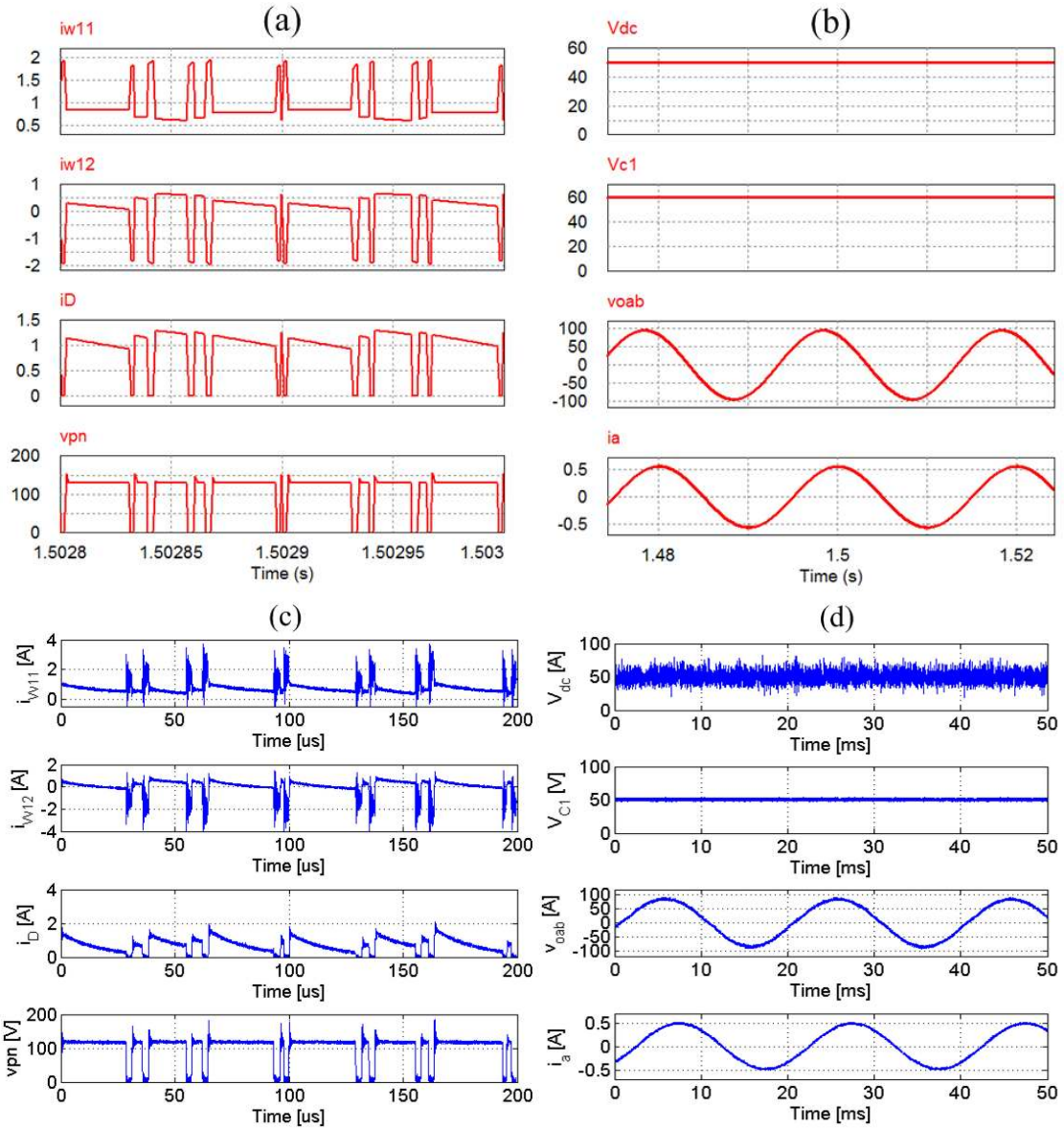

Fig. 10 Waveforms of the proposed sigma-Z-source inverter in case 1 when $M = 0.843$, $D_0 = 0.157$, $n_{T1} = n_{T2} = 2$. From top to bottom (a) simulated winding currents i_{W11} and i_{W12}, diode current i_D, and dc-link voltage v_{pn}, (b) simulated input dc source voltage Vdc, capacitor voltage V_{C1}, output line voltage v_{oab} and current i_a, (c) experimental winding currents i_{W11} and i_{W12}, diode current i_D, and dc-link voltage v_{pn}, (d) experimental input dc source voltage Vdc, capacitor voltage V_{C1}, output line voltage v_{oab} and current i_a.

Next, the characteristic of using a lower turn ratio transformer yet achieving the same voltage gain in case 1 is demonstrated using case 2. Fig. 11 shows the simulated and experimental waveforms for case 2. The windings and diode currents of the experimental waveforms are similar to the simulated results and are not shown for brevity. In Fig. 11(a), the simulated capacitor voltage is boost to 56.25 V and the dc-link voltage is 117.47 V. The corresponding experimental values can be obtained from Fig. 11(b) and they are 52 V and 114 V respectively. From the simulated output line voltage, the gain is 2.35 achieving an output peak to peak voltage of 185.33 V. The experimental output line voltage is similar to the simulated result with a boost gain of 2.28 and output peak to peak voltage of 176 V. This results in similar simulated and experimental peak to peak line current of about 1 A. With the advantage of using a lower turn ratio to achieve higher voltage gain, the improved boost capability also introduces voltage and current spikes as observed in Fig. 11(b).

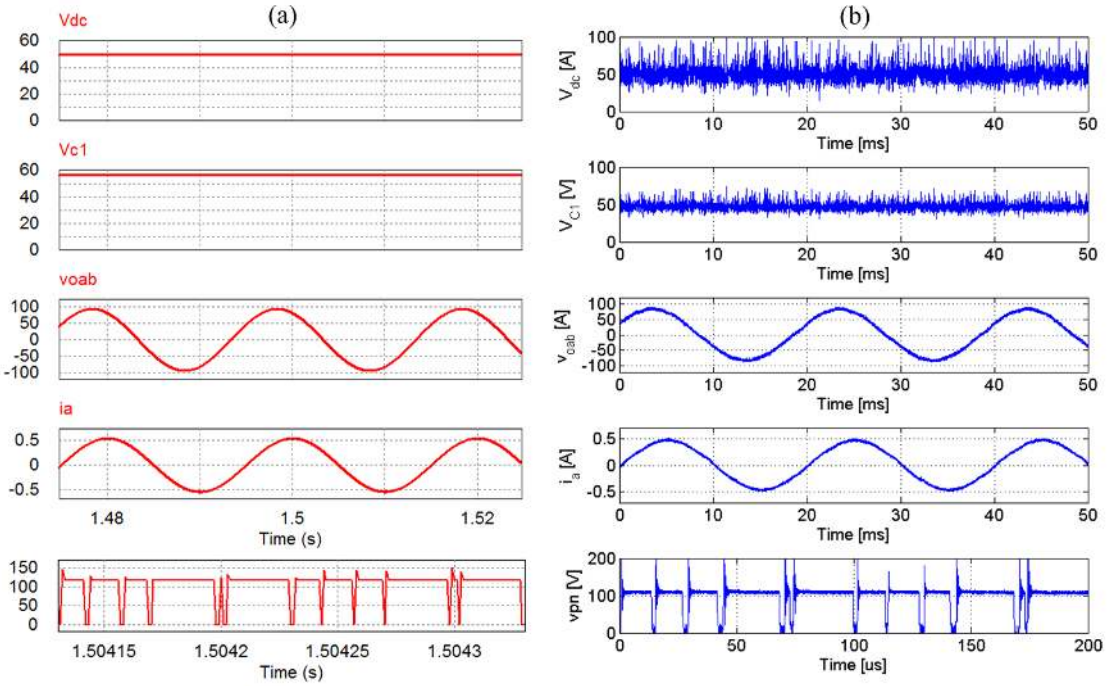

Fig. 11 (a) Simulated and (b) experimental waveforms of the proposed sigma-Z-source inverter in case 2 when M = 0.9, D_0 = 0.1, $n_{T1} = n_{T2}$ = 1.5. From top to bottom, input dc source voltage V_{dc}, capacitor voltage V_{C1}, output line voltage v_{oab}, output line current i_a and dc-link voltage v_{pn}.

Table V
Summary of simulated and experimental results for case 1 and 2.

	n_{T1}	n_{T2}	Leakage inductance refer to primary side	M	D_0	Simulated			Experimental		
						V_{C1}	v_{pn}	i_a	V_{C1}	v_{pn}	i_a
Case 1	2.0	2.0	8.43 µH	0.843	0.157	60.00 V	130.00 V	1.10 A	51.00 V	122.00 V	1.00 A
Case 2	1.5	1.5	4.83 µH	0.900	0.100	56.25 V	117.47 V	1.07 A	52.00 V	114.00 V	1.00 A

For a better discussion of the results, a summary of cases 1 and 2 is shown in Table V. For case 1, the turn ratios for both transformers are 2.0 and a modulation index of 0.843 with a shoot-through duty cycle of 0.157 is used. The experimental dc-link voltage is 122.00 V with an output line current of 1.0 A. By reducing the turn ratio and shoot-through duty cycle to 1.5 and 0.10 respectively, the proposed ΣZSI is able to maintain the same output line current as in case 1. Moreover, the voltage stress of the semiconductor devices for case 2 is about 6 % lower as compared to case 1 due to the use of a higher modulation index.

Due to the use of a higher turn ratio for case 1, the leakage inductance in the transformer is also higher as compared to case 2 resulting in a higher voltage drop. From Table V, the simulated and experimental dc-link voltages are 130.00 V and 122.00 V respectively. The difference is 8.00 V. For case 2, the leakage inductance is reduced to 4.83 µH due to a lower turn ratio of 1.5 used. The difference between the simulated and experimental dc-link voltage becomes 3.47 V. In summary, the comparison of cases 1 and 2 has shown that the proposed ΣZSI is able to obtain the same voltage gain by reducing the turn ratio and shoot-through duty cycle. By doing so, a higher modulation index and a lower leakage inductance can be realized. This results in lower voltage stress across the semiconductor devices and smaller voltage drop.

For case 3, the objective is to demonstrate the difference in current stress due to different turn ratio. Fig. 12 shows the experimental waveforms using the proposed ΣZSI in case 3 where n_{T1} = 2 and n_{T2} = 1.5. From top to bottom, Fig. 12(a) shows the winding currents i_{W11}, i_{W12} and the dc-link voltage respectively. Similarly, Fig. 12(b) shows the winding currents i_{W21} and i_{W22} measured at the same dc-link voltage as in Fig. 12(a). From the results, it is observed that the winding current stress for transformer with n_{T1} = 2 is about 1.5 times lower than the transformer with n_{T2} = 1.5. This result matches the theoretical studies in Table I. Moreover, the measured winding currents i_{w12} and i_{w22} have zero average dc value. This prevents the shifting of the hysteresis cycle of the transformer core towards the saturation region.

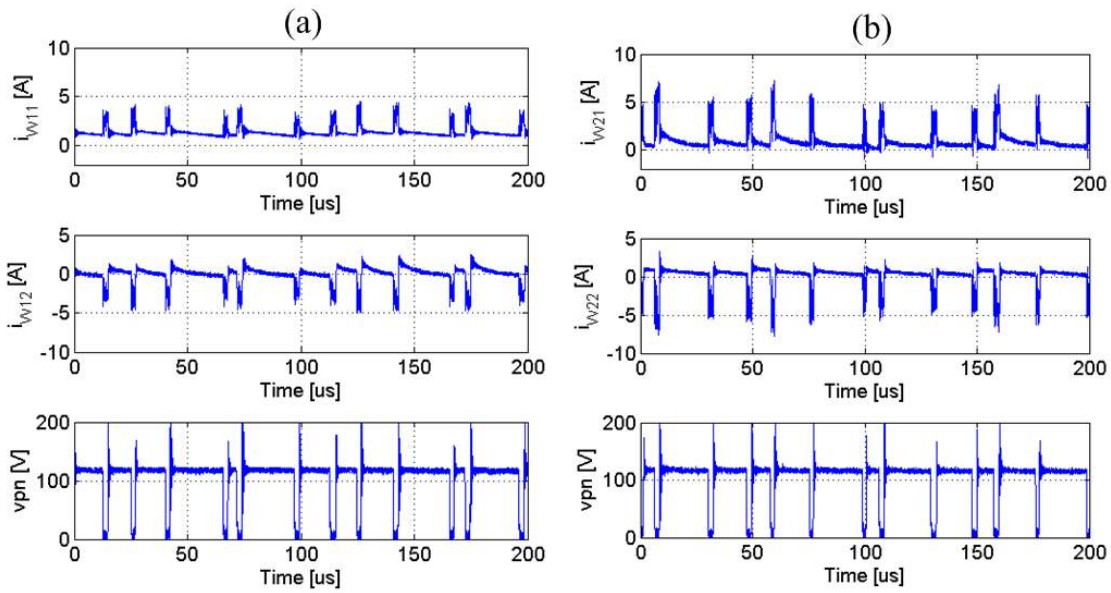

Fig. 12 Experimental waveforms of the proposed sigma-Z-source inverter in case 3 when M = 0.877, D_0 = 0.123, n_{T1} = 2 and n_{T2} = 1.5. (a) top to bottom winding currents i_{W11} and i_{W12}, dc-link voltage v_{pn}, (b) top to bottom winding currents i_{W21} and i_{W22}, dc-link voltage v_{pn}.

V. Conclusion

In this paper, a novel single stage sigma-Z-source inverter (ΣZSI) has been presented. It consists of two mirrored Γ-source networks to form a sigma-source network. Similar to the TZ-source inverter (TZSI), the proposed ΣZSI uses the same components configured in an X-shaped network. However, the dc-ac voltage gain of the ΣZSI is increased by reducing the turn ratio. A comparative study between ΣZSI and TZSI shows that the ΣZSI requires smaller turn ratio transformers when the turn ratio is smaller than 1.618 for any given duty cycle as long as the voltage gain is greater than $M/(1-5.236D_0)$. Simulation and experimental results have validated the operation of the proposed inverter. The results demonstrate that the proposed ΣZSI is able to achieve the same voltage gain when the turn ratio and shoot-through duty cycle are reduced. This results in a compact transformer to be used and the modulation index can be increased to reduce the voltage stress of the semiconductor devices. Furthermore, a transformer with lesser windings has lower leakage inductance that reduces voltage drop.

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