

Significant Reduction of Power/Ground Inductive Impedance and Simultaneous Switching Noise by Using Embedded Film Capacitor

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ABSTRACT –Significant reduction of power/ground inductive impedance and SSN suppression was successfully demonstrated by using embedded capacitor film in high performance package and PCB up to 3GHz frequency range. The reduction of the inductance impedance and SSN are acquired by the help of reduced via inductance in the embedded film capacitor.

I. Introduction

Nowadays, advances in CMOS technology require high-speed, high-current and stable power distribution network for reliable operation of device, package, and system. Major obstacle to obtain the stable power distribution which should be firstly secured is simultaneous switching noise (SSN) and it can be overcome by reducing power/ground network impedance in frequency ranges which are up to 10 times higher than the primary clock frequency of the system. Until now, discrete decoupling capacitors are commonly used to meet these requirements because of its cost effectiveness. [1][4] However, as the clock frequency and its harmonics are increased over GHz frequency range, the discrete decoupling capacitor is no longer effective for this purpose, because the decoupling function of the discrete decoupling capacitor is limited to a few hundred MHz due to self-resonance frequency. In general, high frequency region of the power/ground impedance over 100 MHz is dominated by its inductive behavior of the power/ground network. These inductive parasitic elements include large self-inductance of the decoupling capacitor as well as the inductance of mount pad, power/ground trace and via, and plane cavity resonances. [2]

As an alternative solution to provide the low noise digital power/ground network, embedded capacitor film is strongly emerging, to exhibit better noise performance (lower impedance and consequently smaller SSN) at high frequency range over GHz. These effects are expected by the help of low inductive power/ground current path to remove the excessive inductance of the decoupling capacitor, long through via, mount pad, and trace. Furthermore, the discrete decoupling capacitors can be removed from the surface of package and PCB, yielding better routability.

In this paper, we have experimentally demonstrated the effectiveness of the embedded film capacitor in terms of frequency and time domain measurement of power/ground impedance and Simultaneous Switching Noise (SSN). For the accurate measurement of the impedance, we have developed a microprobe station suitable for measuring the power/ground network impedance of large size multi-port package and PCB. The embedded capacitor has exhibited lower inductive impedance in a wide frequency range from 100 MHz up to 3GHz than the discrete decoupling capacitor has. Furthermore, it is confirmed that thinner embedded capacitor film and center oriented via distribution yield further reduction of the power/ground inductive impedance and the SSN.

II. Fabrication of Test Vehicles and Measurement Setup

To experimentally demonstrate the effectiveness of the embedded capacitor, two pairs of thin film layers (copper clad laminate, 12 μ m, 25 μ m, and 50 μ m of thickness, and 4.6 of dielectric constant, 5cm by 5cm) were inserted to conventional 4-layer PCB whose size was 6cm by 9cm as shown in the Figure 1-(a). The SEM photograph of the fabricated test vehicle with the embedded capacitor layers are shown in Figure 1-(c), (d), and (e). For the accurate measurement of the power/ground impedance (frequency domain), we have developed a microprobe station suitable

for large size and multi-port PCB (up to 40cm by 30cm) and is shown in Figure 2-(a). Agilent 8753D vector network analyzer with Cascade FPC series G-S probe was used for the setup. Also, SSN was measured using Agilent 54616B digital oscilloscope (500MHz bandwidth) with high impedance probe. (Figure 2-(c)). ALTERA was mounted on test vehicle and was programmed as eight clock drivers with frequency of 50MHz to generate SSN on the power/ground network.

III. Measured Power/Ground Impedance and Simultaneous Switching Noise

The significant reduction of the power/ground inductive impedance over GHz using embedded capacitor was measured as shown in Figure 3. The discrete decoupling capacitor could lower the power/ground impedance (dashed line) in the frequency range from its self resonance frequency to the frequency below GHz. That is, the low frequency limit of the decoupling capacitor is determined by its capacitance. On the other hand, the high frequency limit of it is determined by its ESL that is, inductive property of the impedance. Due to its large inductance introduced by its mount pad, trace and via, discrete decoupling capacitor cannot give any reduction over GHz as shown in the graph. Unlike the discrete decoupling capacitor, the embedded film capacitor exhibited the significant reduction of the power/ground inductive impedance over GHz because of its low inductance given by removal of mount pad and trace and shortened via. Of course, the embedded capacitor has smaller capacitance than the discrete capacitor; so its benefit just appears from 60MHz. In the view of SSN, the significant suppression of the power noise spectrum over 100MHz by using the embedded capacitor film was observed as shown in the Figure 4-(b). The noise spectrum was calculated using FFT from the measured SSN as denoted in the Figure 4-(a). Little suppression around 50MHz with the embedded capacitor film was also confirmed from the measurement. To see if both benefits at low and high frequency could be achieved together using both discrete and embedded capacitor, both capacitors were applied to the test vehicle. As can be seen in the Figure 5, Figure 6, the resonance peak introduced by the parallel combination of the ESL of the discrete capacitor and the capacitance of the embedded capacitor was observed around 100MHz. As a result, increased SSN was generated around this frequency in spite of the improvement at low frequency range.

IV. Conclusions

By the help of its low inductance, embedded capacitance has exhibited significant improvement of the power/ground impedance and consequent suppression of SSN over GHz. In this paper, the improvement has been successfully demonstrated by the accurate measurement of the fabricated test vehicles. Also, we have confirmed experimentally the limitation of the discrete decoupling capacitor on the power/ground performance. We also successfully verified the potential problem when we are using both discrete and embedded capacitor together. Using thinner dielectric material, the better power/ground performance up to higher frequency has been obtained. Also, the device (center)-oriented distribution of the power/ground via has shown better performance than uniformly distributed power/ground via case. In near future, due to its low inductive property, the embedded capacitor is expected to be adopted in most of high performance package and PCB inevitably.

Reference

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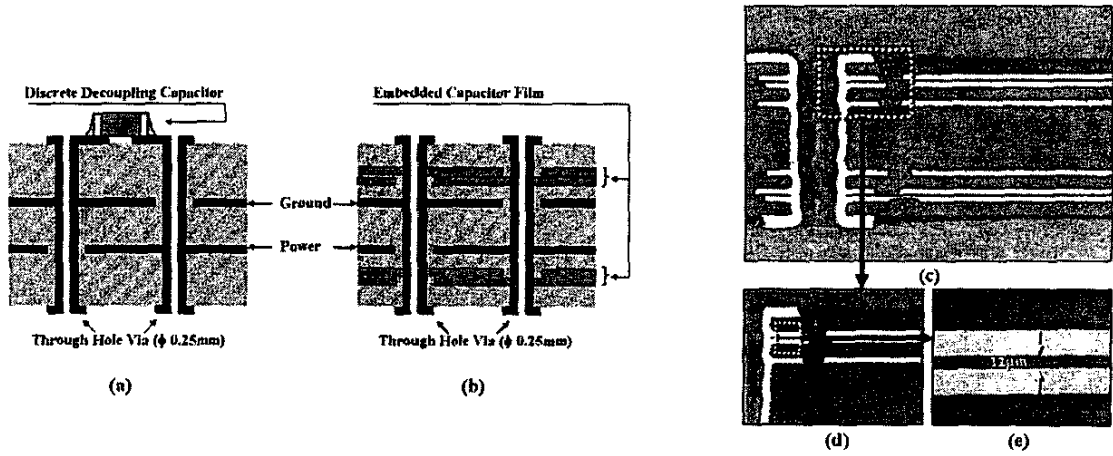


Figure 1 Vertical structures of Test PCB's with (a) discrete chip-type decoupling capacitor and (b) embedded capacitor film. SEM picture of test PCB's with the embedded capacitor film. (c) x50, (d) x100, and (e) x500 magnified.

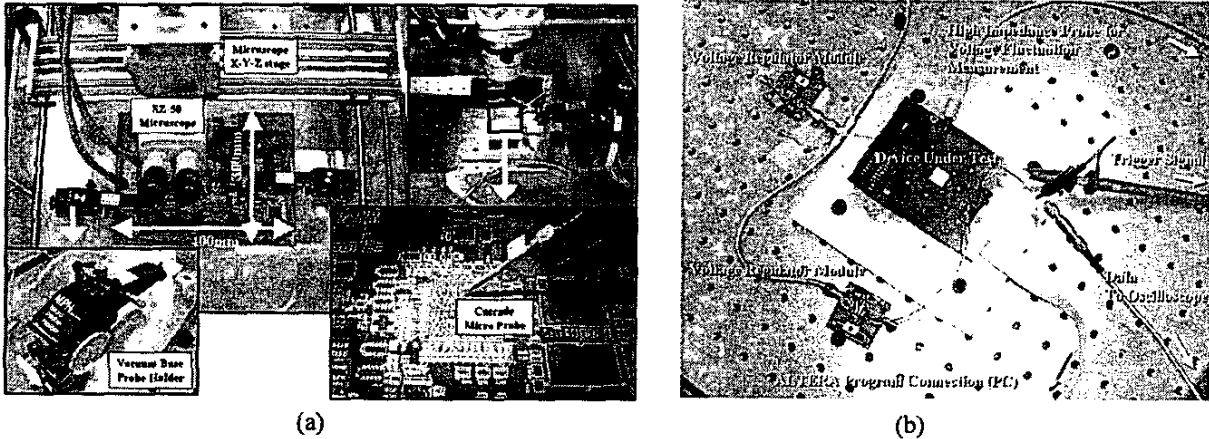


Figure 2 Photograph of (a) microprobe station for the accurate measurement of the power/ground network impedance and (b) the test setup for time-domain power/ground noise (SSN) measurement.

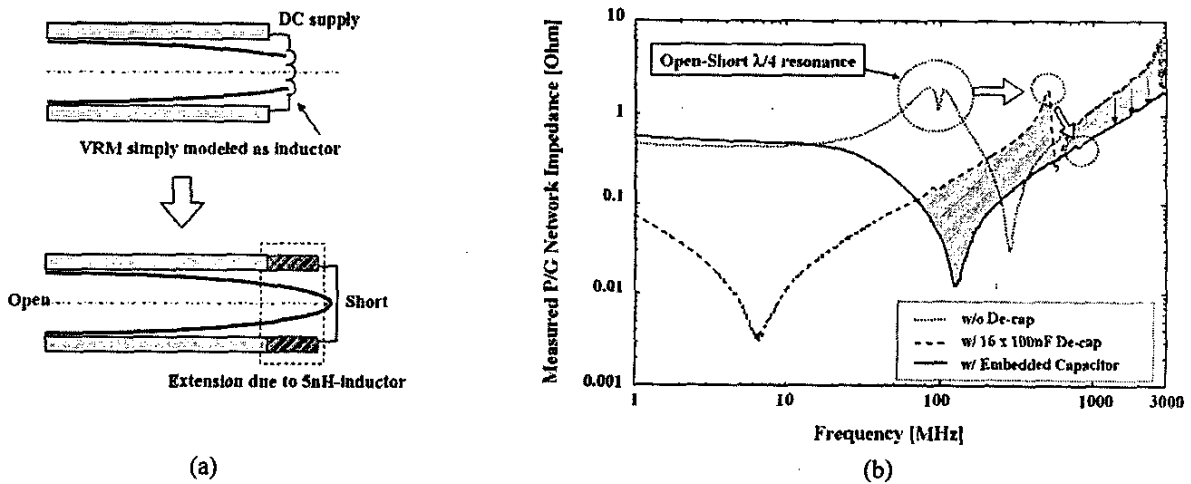


Figure 3 Mechanism of the open-short $\lambda/4$ resonance. (b) Measured Power/Ground Network Impedance curves without any decoupling capacitor (dotted line), with the sixteen discrete decoupling capacitors (dashed line), and with the embedded capacitor film (solid line). Significant reduction of the P/G inductive impedance is confirmed by using the embedded capacitor film on PCB up to 3 GHz frequency range.

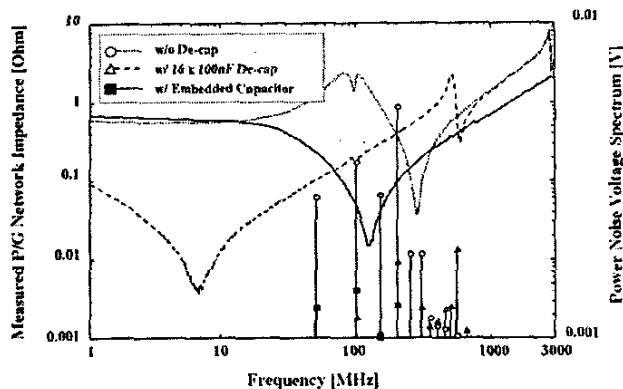
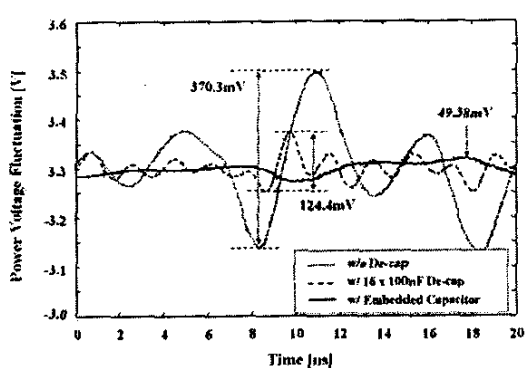


Figure 4 Measured (a) time-domain P/G SSN. (b) Frequency spectrum of the P/G SSN, the P/G impedance without any decoupling capacitor (dotted line), with 16 discrete decoupling capacitors (dashed line), and with the embedded capacitor film (solid line). Significant noise suppression is demonstrated with the embedded capacitor film on PCB.

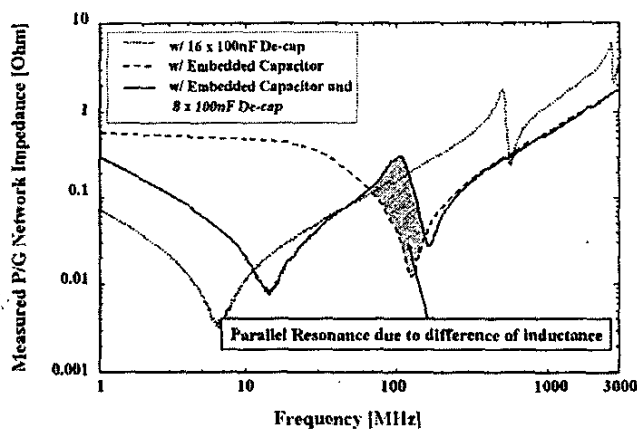
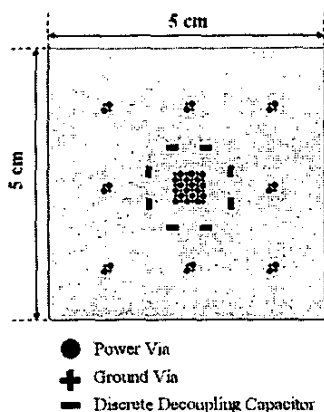


Figure 5 (a) Distribution of the discrete decoupling capacitors and the vias. (b) Measured Power/Ground Network Impedance curves with the sixteen discrete decoupling capacitors (dotted line), with the embedded capacitor (dashed line), and with both of them (solid line). Unwanted parallel resonance peak is generated at about 100MHz.

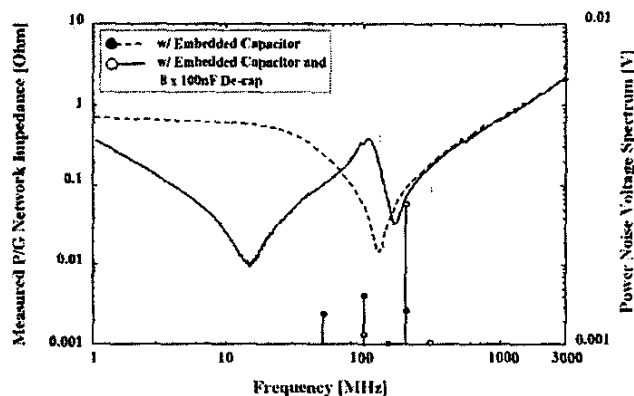
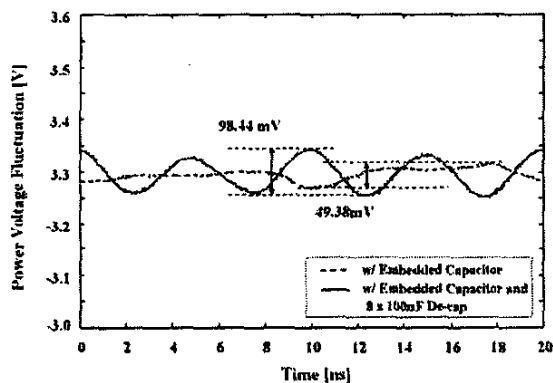


Figure 6 Measured (a) time-domain P/G SSN and (b) SSN noise spectrum calculated, and P/G impedance with the sixteen discrete decoupling capacitors (dotted line), with the embedded capacitor film (dashed line) and with both of them (solid line). Noise spectrum was amplified around an unwanted resonance peak frequency.