Silicon-Based Plasmonics for On-Chip Photonics

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Abstract—Silicon-based photonic devices dissipate substantially less power and provide a significantly greater information bandwidth than electronic components. Unfortunately, large-scale integration of photonic devices has been limited by their large, wavelength-scale size and the weak optical response of Si. Surface plasmons may overcome these two limitations. Combining the high localization of electronic waves with the propagation properties of optical waves, plasmons can achieve extremely small mode wavelengths and large local electromagnetic field intensities. Si-based plasmonics has the potential to not only reduce the size of photonic components to deeply subwavelength scales, but also to enhance the emission, detection, and manipulation of optical signals in Si. In this paper, we discuss recent advances in Si-based plasmonics, including subwavelength interconnects, modulators, and emission sources. From scales spanning slab waveguides to single nanocrystals, we show that Si-based plasmonics can enable optical functionality competitive in size and speed with contemporary electronic components.

Index Terms—Enhanced spontaneous emission, nanophotonics, optical modulation, plasmon waveguides, surface plasmon.

I. INTRODUCTION

CRYSTALLINE silicon paves the modern digital information superhighway [69]. That silicon would become the material of choice for microelectronics is not a historical happenstance. Although the first transistors and integrated circuits were fabricated with germanium, silicon would offer improved thermal stability, a larger bandgap, and the ability to sustain a protective oxide layer. Historical efforts to perfect methods of silicon purification, doping, and oxidation have resulted in a \$400-billion dollar industry forming the core of modern computation.

To date, computational networks have scaled in integration density and switching speed to keep pace with Moore's law. Microprocessors presently contain over 800 million transistors clocked at 3 GHz, with transistor gate lengths as small as 35 nm [12], [38]. By 2022, the International Technology Roadmap for

Semiconductors (ITRS) projects chip capacities will increase beyond 1 Tbit, with transistor gate lengths as small as 4.5 nm. Unfortunately, as gate lengths approach the single-nanometer scale, complementary metal–oxide–silicon (CMOS) scaling is accompanied by increased circuit delay and higher electronic power dissipation—a substantial hurdle to Moore's law often referred to as the "interconnect bottleneck." As noted in the 2008 ITRS, "by the end of the next decade it will be necessary to augment the capabilities of the CMOS process with new devices."

Optical technologies promise to circumvent the electrical and thermal parasitics associated with CMOS scaling. Compared with electronic components, optical devices can offer a substantially higher bandwidth, lower latency, and significantly reduced power dissipation [53], [61], [79]. Optical interconnects, for example, can transmit digital data with capacities over 1000 times larger than Cu wires [61] at twice the speed (30–60 Gb/s) and a fraction of the power consumption. Ideally, optical components including sources, interconnects, modulators, and detectors would comprise the same dimensions, materials, and functionality as electronic CMOS networks. Such design constraints would allow for ready integration into the well-established electronic processing infrastructure.

Unfortunately, Si-based photonics is hindered by two major challenges, namely, the size and sensitivity of Si-based optical devices. Optical components are limited by diffraction, which sets a lower bound on the dimensions with which light can be confined. Relative to CMOS electronic devices, optical devices are extremely bulky, comprising dimensions on the order of the signal wavelength. Large-scale electrooptic integration on a single chip is therefore hampered by the size mismatch between photonic and electronic components. Moreover, unstrained silicon exhibits an indirect bandgap and no linear electrooptic effect—two characteristics that generally yield a weak or slow continuous-wave optical response [71], [72].

Pat Gelsinger, Intel Senior Vice President and Chief Technology Officer, has stated that future computational networks will require a technology that can "collapse the gap between electrons and photons, bringing those together onto a single piece of Si" [1]. Surface plasmons may offer a unique electromagnetic platform for addressing this challenge. Plasmons are hybrid electron–photon oscillations that occur at the interface between a conductor and a dielectric [68]. As longitudinal charge density oscillations, plasmons resemble light waves confined to the surface of a metal. However, surface plasmons are also nonradiative in nature, characterized by evanescent electric fields in both the metal and dielectric. Relative to free-space photons, surface plasmons achieve very high local field intensities and short wavelengths, with even X-ray wavelengths accessible at

optical frequencies. Plasmons thus combine the high localization of electronic currents with the propagation properties of optical waves.

While the optical properties of metallic nanostructures have been studied for centuries, surface plasmons have only recently been considered for optoelectronic applications. In this paper, we describe various proposed and implemented plasmonic architectures for integrated photonics. Particular attention is given to metal–dielectric(insulator)–metal (MIM) geometries, where optical effects are dramatically enhanced by high field confinement in the dielectric slot. We show how MIM geometries can be implemented as CMOS compatible subwavelength interconnects, field-effect modulators, and optical cavities for enhanced spontaneous emission. Techniques for coupling single emitters (i.e., nanocrystals) to plasmonic geometries are discussed, and applications ranging from on-chip single photon sources to ultrasensitive photodetectors are proposed.

II. Si-Based Plasmonic Waveguides: Subwavelength Photonic Interconnects

The electronic interconnects that power devices from cellular phones to supercomputers rely on highly conductive metallic wires to transmit electrical signals. That this same metallic circuitry could be used to transmit optical signals is a fortuitous consequence of electrodynamics. While metals at microwave wavelengths are near-perfect conductors, metals are characterized by a finite field skin depth at visible and near-infrared wavelengths. Along a planar metal–dielectric interface, this skin depth is just large enough ($\sim$20 nm) to permit coupling between the free surface electrons and incident photons in the form of surface plasmon polaritons.

In planar geometries, surface plasmons represent plane-wave solutions to Maxwell's equations [33], [68]. Akin to conventional optical interconnects, the plasmon wave vector k_x can be used to uniquely determine the complex mode index as a function of frequency, ω. Naturally, the wavelength λ_{SP} and index n of surface plasmons are related to the magnitude of the real component of k_x via

$$\lambda_{SP} = \frac{2\pi}{|\text{Re}\{k_x\}|} \tag{1a}$$

$$n = \frac{c \cdot \text{Re}\{k_x\}}{\omega}. \tag{1b}$$

Likewise, the losses can be extracted from the magnitude of the imaginary component of k_x, with mode propagation lengths L_{SP} given by

$$L_{SP} = \frac{1}{2\text{Im}\{k_x\}}. \tag{2}$$

Solving Maxwell's equations subject to continuity of the tangential electric fields E_x and normal displacement fields D_z yields the plasmon dispersion relations $k_x(\omega)$ [29]–[31]. Since continuity of E_y forbids charge accumulation at the interface, transverse-electric surface plasmon waves do not generally exist in planar metallodielectric structures.

Along thin metallic films and wires, surface plasmons can propagate over tens of centimeters at infrared wavelengths [7]–[9], [29]. Supporting the so-called "long-range surface plasmon-polariton" (or LR-SPP), this geometry has formed the basis for many passive plasmonic waveguide elements, including low-loss bends, waveguide couplers, splitters, interferometers, and grating filters [18]. However, this long-range plasmon propagation is achieved at the expense of confinement: field penetration increases exponentially with wavelength from the metal/dielectric interface, extending over several microns into the surrounding dielectric [7]–[9], [20], [29]. In terms of designing highly integrated photonic and plasmonic networks, a more favorable balance between localization and loss is required.

In recent years, attention has shifted to high-index contrast (HIC) structures for dense optical integration and strong field confinement. In the context of fiber interconnects, HIC geometries are generally composed of a low index dielectric core surrounded by a higher index cladding [4]. While these fibers are characterized by low loss and high-mode confinement, their dimensions are limited by diffraction. An alternate geometry replaces the high-index dielectric cladding with a metallic layer [74]. These MIM, or plasmon slot waveguides, are characterized by higher losses than their all-dielectric counterparts, but can substantially reduce the mode wavelength [28], [30], [33], [86]. MIM waveguides thus allow optical mode volumes to be reduced to deeply subwavelength scales, with negligible field decay out of the waveguide physical cross section.

Fig. 1 illustrates the transverse-magnetic dispersion relations for a slab MIM waveguide composed of an Si core and Ag cladding layers. Similar results are achievable with various CMOS-compatible dielectric cores (i.e., SiO_2, Si_3N_4) and metallic cladding layers (i.e., Cu or even highly doped Si) [27], [30], [47]. As shown in the inset, wave propagation is assumed to be along the x-direction, with each material interface perpendicular to z; the waveguide is infinite in y. Similar to conventional optical interconnects, the core dimensions determine the allowed propagating modes. If the core thickness t exceeds approximately one half the optical wavelength, these MIM waveguides will be predominantly characterized by "photonic" modes, which resemble the modes of a parallel-plate microwave waveguide [40]. As seen in Fig. 1(a), these photonic modes lie to the left of the Si light-line, $\omega = ck_0/n_d$, where n_d is the refractive index of the Si core and $k_0 = 2\pi/\lambda_0$. For these larger core MIM waveguides, a surface plasmon mode to the right of the light line is also present, corresponding to polaritons propagating along each Ag/Si interface.

As the core thickness is reduced, the cutoff energy of each photonic mode increases until only coupled plasmonic modes remain. These plasmonic modes are characterized by electric field distributions E_x that are either antisymmetric (TM_0) or symmetric (TM_1) across the waveguide core, with field maxima at each metal–dielectric interface. As shown in Fig. 1(b), wave vectors of the fundamental TM_0 mode approximate the Si light line for longer wavelengths and approach a maxima at the surface plasmon resonance. Compared with the plasmon dispersion relation for a single metal–dielectric interface (plotted in gray), this TM_0 mode is characterized by larger wave vectors
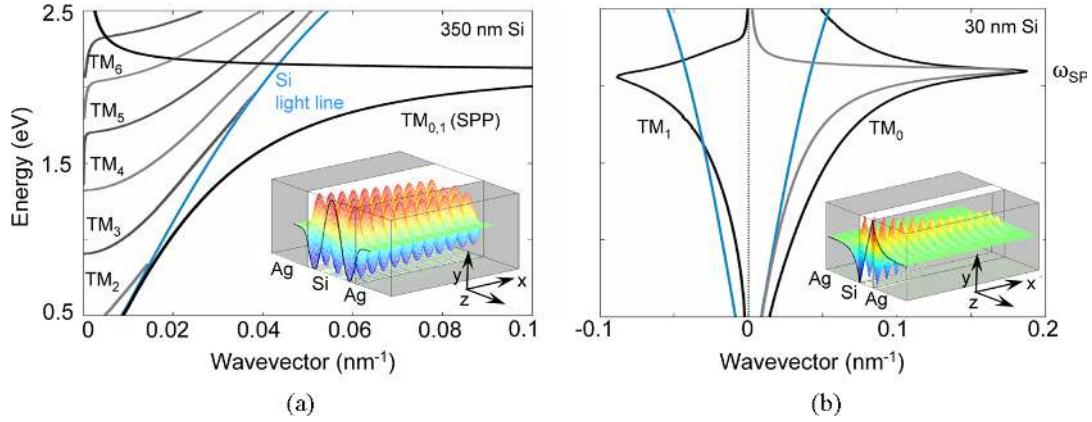
Fig. 1. Calculated transverse-magnetic mode dispersion relations for slab metal–insulator–metal waveguides composed of an Si core and Ag cladding. (a) Dispersion curves for a Ag/Si/Ag waveguide with a dielectric core thickness $t = 350$ nm. This thick-core waveguide supports a number of transverse-magnetic photonic modes (gray lines), lying to the left of the Si light line, and also a plasmonic mode (black line). As the core thickness is reduced to 30 nm (b), the photonic modes are cutoff and only plasmonic modes are allowed to propagate. The insets show characteristic E_x field profiles for the (a) TM_3 photonic mode and the (b) TM_0 plasmonic mode.

and hence smaller surface plasmon wavelengths. Interestingly, this mode does not exhibit cutoff, regardless of the transverse core dimensions. In fact, plasmon wave vectors as small as 50 nm have been observed in MIM geometries composed of a 3 nm SiO_2 core and an Au cladding, excited with a free-space wavelength of 650 nm [55].

MIM waveguides with subwavelength-thickness cores can also support modes with negative wave vectors [31], [70]. These TM_1 modes are characterized by antiparallel energy and phase velocities, and hence, a negative index. As seen in Fig. 1(b), at lower energies (≤ 1.5 eV), the group and phase velocities of this mode exceed those of a photon in bulk Si. For these energies, we will see that this mode is characterized by extremely high losses. However, between the bulk and surface plasmon resonance, this mode can actually propagate much farther than the TM_0 mode, offering a unique opportunity for on-chip negative index materials.

Variation of waveguide composition or core dimensions allows for ready tuning of the complex plasmon mode wave vector and index. Fig. 2 plots the achievable plasmon mode indices and figures of merit (FOM) for Ag/Si-based MIM waveguides with core thicknesses ranging from 5 to 50 nm. Here, the FOM is defined as the ratio of $Real\{k_x\}$ to $Imag\{k_x\}$, or equivalently, $Real\{n\}$ to $Imag\{n\}$. Heuristically, the FOM indicates the number of plasmon cycles supported by the structure before the wave decays. Note that each vertical slice through the figure corresponds to one dispersion diagram, with the index and FOM plotted on the color scale. Mode index maps are provided for both the TM_0 and TM_1 modes. As seen, both modes achieve refractive index magnitudes spanning from ~ 0 to $|n| > 60$ as the Si core thickness is reduced. FOM for the TM_0 mode obey step-function-like behavior across the surface plasmon resonance, where the high FOM observed below the resonance quickly decay to zero above resonance. Correspondingly, the FOM for the TM_1 or negative index mode are nearly zero for frequencies below the surface plasmon resonance, but approach 15 for thinner waveguides excited above resonance. Interestingly, these
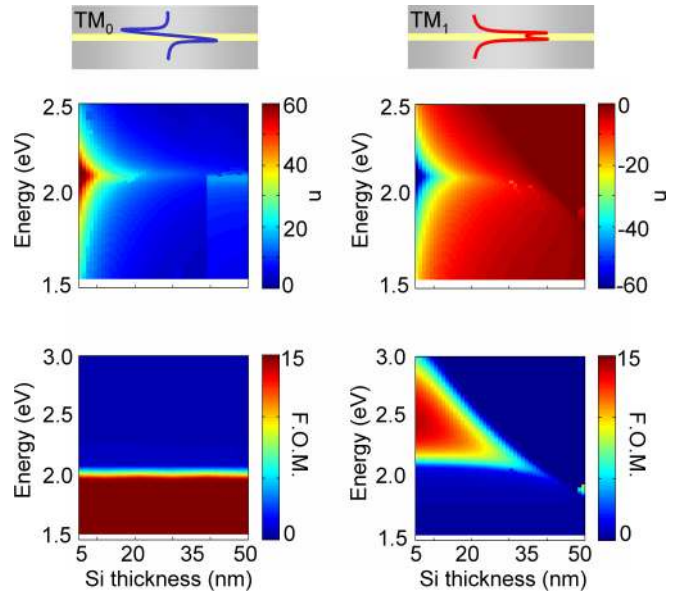

Fig. 2. Calculated mode indices and FOM = $Re(k_x)/Im(k_x)$ for Ag/Si/Ag slab waveguides, plotted as a function of photon energy and waveguide core thickness. Results are included for both the E_x-field-antisymmetric, TM_0 mode and the E_x-field-symmetric, TM_1 mode.

negative-index FOM can be orders of magnitude higher than the FOM for positive index modes above resonance. For example, at a wavelength of ~ 550 nm (2.42 eV), negative indices of $n = -25$ can be achieved with FOM equal to 14, using a 5-nm-thick Si core. In contrast, the FOM for the positive index mode at the same wavelength is <0.5.

Fig. 3 plots the propagation lengths for various MIM waveguides. Attention is given to the fundamental TM_0 mode, which can propagate many microns throughout visible and near-infrared wavelengths. Not surprisingly, propagation lengths decrease with decreasing core thickness, shown here for Ag/Si/Ag waveguides with t spanning 35–175 nm.
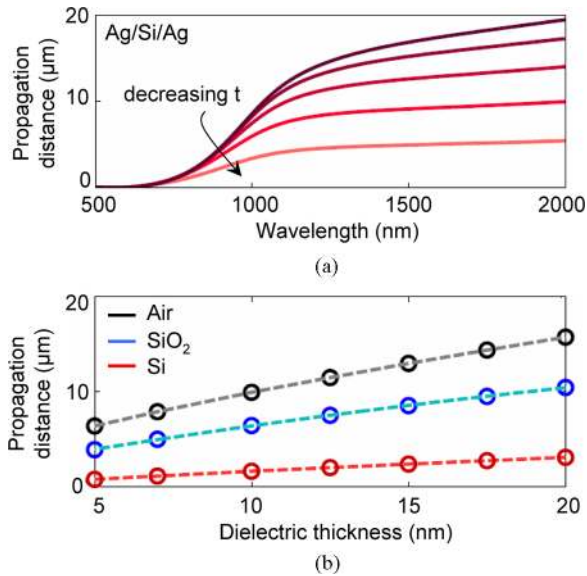
Fig. 3. Plasmon propagation lengths for the TM_0 mode of MIM wavguides. (a) Propagation lengths of Ag/Si/Ag slab waveguides, plotted as a function of free-space wavelength for Si core thicknesses of $t = 35$ nm, 75 nm, 115 nm, 150 nm, and 175 nm. (b) Plasmon propagation lengths at $\lambda = 1.55$ μm for Ag-clad MIM waveguides of varying core dielectric thickness and composition.

However, propagation lengths actually increase with increasing wavelength—a result of the lower metal losses for longer wavelengths. For waveguide cores thinner than 100 nm, propagation lengths can approach 10 μm at near-infrared wavelengths.

Variation of propagation length with core thickness is shown in Fig. 3(b). Here, the MIM waveguide is composed of Ag cladding layers with either an Si, SiO_2, or air core. The wavelength has been set to 1550 nm, corresponding to the C-band for fiber-optic communications, and the waveguide core thickness is varied from 5 to 20 nm. As seen, propagation lengths decrease with decreasing core thickness and increasing core index. Still, a 15-nm-thick SiO_2 core waveguide can sustain plasmon propagation over 8 μm. In other words, a waveguide with a core thickness 100 times smaller than the optical wavelength supports plasmon propagation over distances of five times the wavelength.

Experimental results have confirmed these propagation trends, and have also shown that conversion from a slab geometry to a rectangular (tubular) waveguide does not substantially impact the mode profile or propagation length [28], [77]. Notably, the significant concentration of light in MIM geometries can be leveraged to create devices with a volumetric size of only a few cubic wavelengths [27], while being suitable for planar integration [17] and having an intrinsic top and bottom contact available for electrooptic operation. Alternatively, these MIM geometries can be adapted for plasmon propagation in slits and grooves. For example, MIM-related modes can be identified at the tip of V-shaped grooves in a metal surface [59], [66], [67]. These so-called channel plasmon polaritons (CPPs) have enabled the design of low-loss, compact plasmonic waveguides, bends, and splitters, as well as ring-resonator-based components such as add–drop filters [15], [16], [80].

Despite the characteristic losses of metals, the previous results suggest plasmon waveguides as potential interconnects for highly integrated photonic circuits—particularly in applications where dense integration is favored over long-range propagation. While fiber-optic technology has been challenging to implement over the "last mile," CMOS-compatible plasmoic waveguides may facilitate implementation throughout the "last micron."

III. ACTIVE PLASMONICS: DISPERSION HAS A SILVER LINING

Dispersion is among the most undesirable features in photonic networks. In optical fibers, for example, this variation of phase velocity with wavelength limits both the signal integrity and the rate of data transfer over long distances. However, as we saw in the last section, dispersion is an inescapable characteristic of plasmonic architectures. Since the electric permittivity of metals is a strong function of wavelength, so too is the surface plasmon wave vector.

While dispersion limits the utility of plasmonic interconnects for long-range communications, dispersion engineering can yield novel active devices. Over micron-scale distances, plasmonic dispersion enables ready tuning of the plasmonic index and propagation constant simply by tailoring the waveguide composition and dimensions. Alternatively, small induced shifts in the waveguide index or dimensions can profoundly impact plasmon propagation.

In recent years, considerable effort has been devoted to dispersion-engineering surface plasmons for active devices. In 2004, for example, Nikolajsen *et al.* reported thermooptic interferometric modulation of the LR-SPP mode in metal stripe waveguides [57]. This modulator offered strong performance in terms of insertion loss, intrinsic loss and mode extinction ratio, but the 20-mm-long device did not offer subwavelength confinement. Concurrently, Krasavin and Zheludev proposed a technology for active control of plasmon waves based on nanoscale structural transformations [43]. In simulations using the properties of a solid-liquid phase change in Ga, all-optical switching was described in a waveguide only 2.5 μm by 2.5 μm, requiring 10 pJ of energy, and exhibiting submicrosecond speed.

Since these pioneering results, electrooptic surface plasmon modulators have been demonstrated in a number of other material systems including liquid crystals [34] and ferroelectric thin films [25], [50]. In the realm of all-optical plasmonic devices, the strong localization of light has been leveraged to achieve low power optical switching in waveguides less than 10 μm long, featuring sub-100 nanometer thin film active regions consisting of CdSe quantum dots [62] or photochromic molecules [63]. Very recently, ultrafast SPP modulation has been achieved by direct femtosecond pulse optical excitation of a metal waveguide [85]. These varied approaches are indicative of a wide range of active plasmonic applications, with a correspondingly large range of target performance characteristics.

An alternative plasmonic device, designed with on-chip integration in mind, relies upon field-effect modulation of
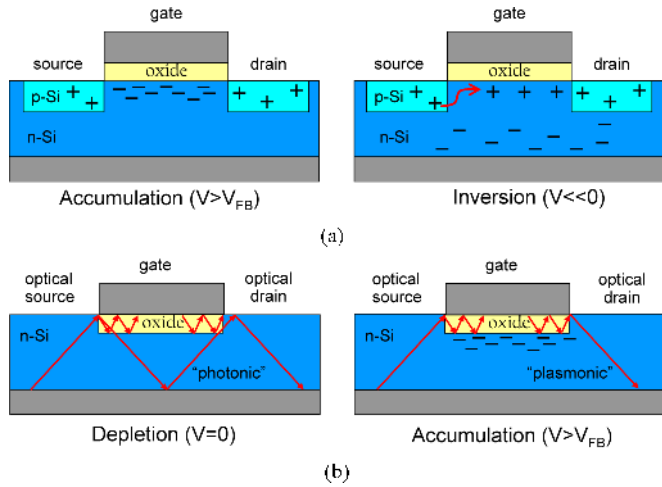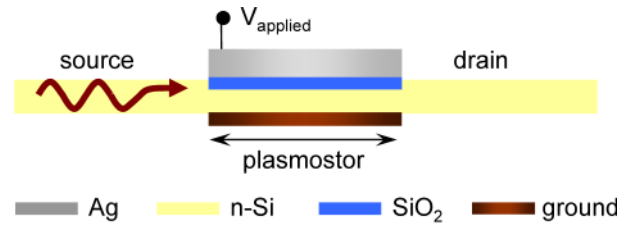
Fig. 4. Schematic operation of a conventional MOSFET compared with the plasMOStor. (a) In a conventional electronic MOSFET, current is modulated between a p-type source and drain via an applied electric field at the gate. (Left) In accumulation, electrons in the n-type Si of a MOSFET form a 2-D electron gas that prohibits the flow of holes from the source to the drain. (Right) For negative applied biases, an inversion layer of minority carriers forms just below the oxide, creating a channel for holes to flow. (a) Schematic of a plasMOStor for modulation of optical signals. (Left) In the absence of an applied gate voltage, the plasMOStor is fully depleted, and light can be guided through both the Si and SiO$_2$ layers. (Right) For applied voltages greater than the flat band voltage, an accumulation layer forms that inhibits photonic mode propagation through the Si.

Fig. 5. Geometry and tabulated modes of the plasmostor. (Top) The plasmostor is composed of a Ag gate contacting a 10-nm-thick SiO$_2$ layer on 173 nm of n-type Si; the ground is also Ag. Here, the optical source and drain consist of an Si waveguide with transverse dimensions equal to the plasmostor dimensions. (Bottom) Tabulated mode profiles, refractive indices and losses for the plasmostor in both depletion (voltage-OFF) and accumulation (voltage-ON) states at $\lambda = 1550$ nm.

plasmon modes in a metal–oxide–silicon (MOS) geometry—a close cousin of the MIM geometry. This "plasMOStor" extends the design of conventional electronic MOSFETs to modulate optical signals, by transforming the channel oxide into a plasmon slot waveguide [27]. Fig. 4 highlights the distinctions between a conventional MOSFET and the plasmostor. As seen in Fig. 4(a), a MOSFET modulates current between a p-type source and drain via an applied electric field at the gate. For gate voltages above the flat-band voltage, the device is in accumulation and electrons in the n-type Si form a 2-D electron gas that prohibits the flow of holes from the source to the drain. In contrast, for negative gate biases, electrons in the substrate are repelled and an inversion layer of minority carriers forms just below the oxide. This layer creates a channel between the source and drain for holes to flow, switching the device to its "ON" state.

The plasmostor is essentially a MOSFET designed to operate in accumulation. A schematic is shown in Fig. 4(b). As seen, the electronic source and drain are replaced with an optical source and drain for light to enter and exit the device. In the absence of an applied field at the gate, the plasmostor is fully depleted and light can be guided through both the Si and SiO$_2$ layers. Depending on the waveguide length, these two modes will interfere either constructively or destructively at the optical drain. However, for voltages greater than the flat band voltage, an accumulation layer forms that inhibits wave propagation through the Si. In accumulation, light will be almost exclusively guided through the thin channel oxide, and will exit the drain without interference from the Si-guided mode.

The accumulation-based operation of the plasmostor relies on cutoff of a photonic mode in the Si core. By designing the plasmostor with a 170-nm-thick Si core and 10-nm SiO$_2$ channel, a small gate voltage can cutoff the TM$_2$ photonic mode for wavelengths spanning $\lambda = 1.48$–1.58 μm [27]. Plasmostor operation at $\lambda = 1.55$ μm is illustrated in Fig. 5. Here, the plasmostor is modeled as a four-layer waveguide consisting of semi-infinite Ag cladding layers surrounding the Si core and SiO$_2$ channel. In the off state ($V = 0$), the unbiased plasmostor supports two modes: the TM$_2$ photonic mode lying to the left of the Si and SiO$_2$ light lines, and a plasmonic mode lying to the right of the Si light line. As seen in the table of Fig. 5, the photonic mode (red) is characterized by an electric field localized predominantly in the Si core and a mode index of $n = 0.375$. In contrast, the plasmonic mode (blue) exhibits maximal field intensities within the SiO$_2$ channel and a mode index of $n = 3.641$. Losses of the plasmonic and photonic modes are 0.207 and 2.37 dB/μm, respectively. For both modes, fields in the metal cladding decay within approximately 20 nm of the Ag–Si and Ag–SiO$_2$ interfaces.

Modifying the Si index through free-carrier absorption can push the TM$_2$ mode into cutoff, such that this modal dispersion curve intercepts the energy axis just above $\lambda = 1.55$ μm. The remaining plasmonic mode will then propagate through the plasmostor without interference from the photonic mode. In the plasmostor, such changes in the Si index are induced by applying a positive bias to the gate. For drive voltages above the flat-band voltage, electrons in the n-type Si form an accumulation layer characterized by a peak carrier concentration at the Si/SiO$_2$ interface and a spatial extent given by the Debye length. Fig. 5 tabulates the theoretical change of mode index and propagation
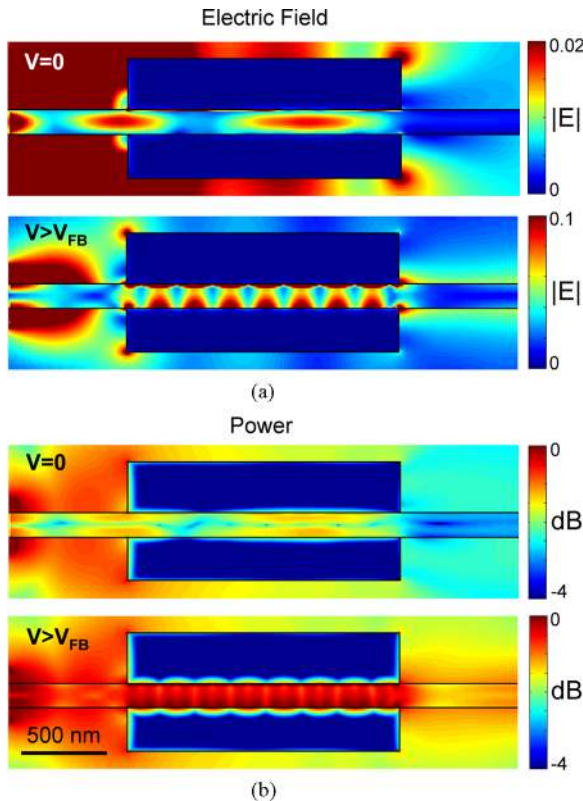
Fig. 6. Finite-difference time-domain simulations of the plasmostor, showing the (a) total electric field and the (b) transmitted power for a 1.6-μm-long optical source–drain separation. Plasmostor mode and power profiles at $\lambda = 1.55$ μm are shown in both the voltage-OFF (depletion) and voltage-ON (accumulation) states.

length with the onset of accumulation. Here, the accumulation layer is modeled as a multilayer Drude electron gas with an average carrier concentration of approximately 5×10^{18} cm^{-3} and a Debye decay length of 14 nm. As expected, the effective index and losses of the plasmonic mode exhibit very little change between the voltage-OFF (depletion) and voltage-ON (accumulation) states. In particular, the plasmonic mode index varies from the off state by $\delta n = 0.008$, and losses are only slightly increased to 0.228 dB/μm. However, the photonic mode is pushed into cutoff, as indicated by the near-zero mode index and substantially increased losses (i.e., the photonic mode becomes evanescent). Therefore, in the accumulation state, the plasmostor will guide near-infrared light almost exclusively through the 10-nm-thick SiO$_2$ channel [45], solely via the plasmonic mode.

Finite-difference time-domain simulations [2] of plasmostor operation are illustrated in Fig. 6. In these simulations, the plasmostor is excited at $\lambda = 1.55$ μm via an Si waveguide. The plasmostor length has been set to 1.6 μm, and the transverse source and drain dimensions are equal to the plasmostor core thickness. This Si waveguide source supports a fundamental TM photonic mode that couples into the plasmostor with coupling efficiencies of $\sim$30% [73]. Note, however, that more efficient coupling schemes, exhibiting $\geq$90% coupling efficiencies, are possible [78].

As seen in the upper panel of Fig. 6(a), in the absence of an applied gate voltage, plasmostor fields are distributed throughout the Si core with sparse regions of high electric field in the oxide slot. However, with the onset of accumulation, the field transmitted within the Si core is notably decreased. As seen in the lower panel of Fig. 6(a), plasmostor fields are localized predominantly within the 10-nm-thick oxide layer and along the Si/Ag interface. In one sense, the oxide layer serves as an optical channel between the optical source and optical drain. Within the plasmostor, pronounced maxima and minima within the resonator can be observed with a wavelength of $\sim$250 nm.

By choosing the source–drain separation to correspond to a condition of destructive interference between the photonic and plasmonic mode, plasmostor transmission can be substantially increased by inducing accumulation. Fig. 6(b) plots the total power transmitted through the plasmostor at $\lambda = 1.55$ μm, with a source–drain separation $d = 1.6$ μm. Comparing intensities at the optical drain between the voltage-OFF and voltage-ON states, modulation ratios of approximately +4 dB can be observed.

Plasmostor operation has been experimentally demonstrated for wavelengths spanning $\lambda = 1.48$ μm to 1.58 μm and also at 685 nm [27]. By varying the source–drain separation in nanometer-scale increments, amplitude modulation depths ranging from -3.15 to 4.56 dB were observed at $\lambda = 1.55$ μm with gate biases as small as 0.75 V. Moreover, simulations indicate the potential for modulation ratios as high as 11 dB in device volumes as small as one-fifth of a cubic wavelength. The low switching voltages and experimentally determined plasmostor capacitance yield a required switching energy $E = CV^2/2$ of 3.5 fJ, commensurate with existing CMOS and optical logic gates [49]. Combined with its gigahertz switching speeds, the plasmostor offers a unique opportunity for compact, Si-based plasmonic modulation using scaled electronic MOSFET technology.

IV. ON-CHIP Si-COMPATIBLE LIGHT SOURCES: PLASMON-ENHANCED SPONTANEOUS EMISSION

The library of photonic waveguides and modulators compatible with CMOS processing is expanding on a Moore's-law-like trajectory. This initial success of Si-photonics is in part due to the advantages offered by Si. As noted earlier, Si is characterized by a high refractive index and a low intrinsic absorption at near-infrared wavelengths—two features that make it ideal for photon guiding and detection. Unfortunately, Si is also characterized by an indirect bandgap—a feature that reduces the probability of photon absorption or emission, since electronic transitions from the valence to conduction band require simultaneous absorption or emission of a phonon.

In recent years, considerable effort has been devoted to enhancing the optical properties of Si and other CMOS-compatible materials. This intense effort is motivated by the necessity to develop on-chip Si-compatible light sources, including LEDs and lasers. Among various approaches to enhance Si light emission, rare-earth-doped and quantum confined structures have received particular attention [41]. On the one hand, quantum confinement effects in nanostructured materials can significantly change the
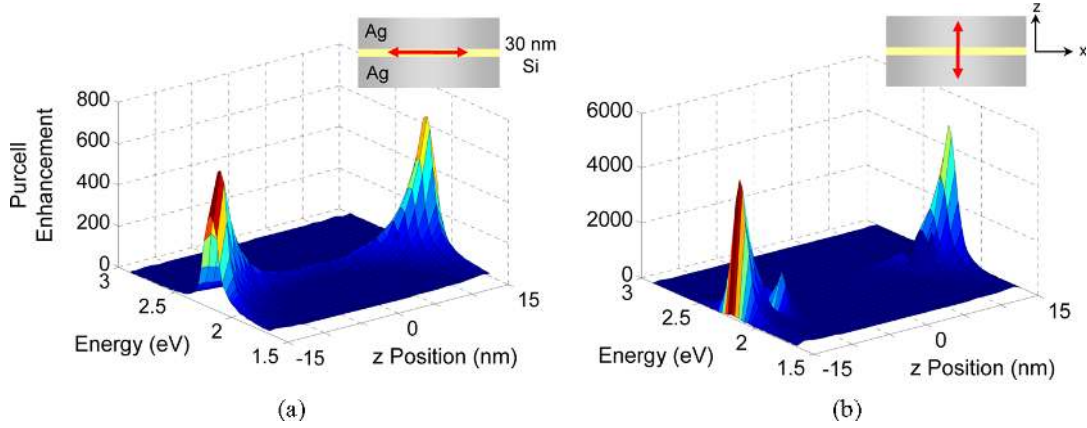
Fig. 7.   Simulated Purcell enhancement for MIM waveguide cavities composed of a 30-nm-thick Si core and Ag cladding layers. Purcell enhancements are plotted for dipoles oriented both parallel and perpendicular to the metal interface, as a function of dipole position and emission energy. The waveguide core is centered at $z = 0$, and waveguide dimensions are assumed infinite in x and y.

material's band structure, modifying both the ground-state energy and the density of electronic states [19], [82]. In Si, quantum confinement has led to high external quantum efficiency bulk LEDs [76], novel nanocrystal-based field-effect LEDs [81], and even the possibility of fast optical gain in closely packed nanocrystals [24], [65]. On the other hand, rare-earth doping has led to efficient room-temperature Si-Er electroluminescence [37] and the possibility for Si-based optical amplification. Despite these advances, however, the radiative rates for absorption and emission of light in Si remain well below those of direct gap semiconductors.

Plasmonic effects present an alternate approach to enhancing light emission from Si and Si-compatible materials. The high local electromagnetic fields produced by surface plasmons can modify the absorption cross-section, radiative decay rate, and quantum efficiency of an emitter [10], [11]. In addition, the reduced surface plasmon wavelength can enable high quality factor microcavities [54] that confine light well below the diffraction limit. Combined, these plasmonic effects have enabled novel devices for on-chip nonlinear optics [44], [64], quantum optics [21], and lasing [35].

In terms of developing a Si-compatible plasmonic light source, it would be highly desirable to directly integrate light-emitters with planar plasmon waveguides. This design would enable near-zero coupling loss of sources to other on-chip devices [41] and ensure compatibility with standard CMOS processing techniques. Moreover, the waveguide itself could be designed to enhance (or suppress) light emission via control of the local density of optical states (LDOS). In this section, we investigate coupled emitter–plasmon interactions in a planar waveguide geometry. Exploiting the MIM waveguides discussed earlier, we show that enormous LDOS enhancements can be achieved, even far from the surface plasmon resonance.

The local density of states (LDOS) describes the total number of eigenmodes available to a source at a specific spatial location [36]. Analytically, the LDOS can be determined from the imaginary component of the Green's function tensor, which describes the frequency-dependent field response at $\mathbf{r}'$ to an oscillating dipole at $\mathbf{r}$ [51]

$$\left[\nabla \times \nabla \times \frac{\omega^2}{c^2} \varepsilon(\mathbf{r}) \right] G(\mathbf{r}, \mathbf{r}'; \omega) = \frac{\omega^2}{c^2} \mathbf{I} \delta(\mathbf{r} - \mathbf{r}'). \quad (3)$$

Here, $\mathbf{I}$ is the unit dyadic and $\varepsilon(\mathbf{r})$ is the spatially dependent permittivity. The Green's function tensor yields both the spontaneous emission rate Γ and the Purcell factor F_P via [32], [51]

$$\Gamma(r) = \frac{2d \cdot \text{Im}[G(\mathbf{r}, \mathbf{r}; \omega)] \cdot d}{\hbar \varepsilon_0} \quad (4a)$$

$$F_P = \frac{\text{Im}[G(\mathbf{r}, \mathbf{r}; \omega)]}{\text{Im}[G_{\text{hom}}(\omega)]} \quad (4b)$$

where d is the optical dipole moment of the emitter and G_{hom} is the Green's function tensor for a homogeneous medium. Of course, the imaginary component of G_{hom} is given by the well-known analytic expression, $\text{Im}[G_{\text{hom}}] = \omega^3 \sqrt{\varepsilon}/6\pi c^3$.

In plasmonic geometries, strong Purcell enhancements have been demonstrated along single metallic films [5], [60] and near nanoparticles [52] and nanowires [3]. Spontaneous emission enhancements have also been investigated in plasmon gap geometries supporting only the TM_0 mode [39]. Fig. 7 shows the calculated Purcell enhancement for a MIM waveguide as a function of dipole frequency (energy) and position. Here, the waveguide is composed of 30 nm of Si clad by Ag. However, similar results can be achieved with various CMOS-compatible cores and cladding layers. The waveguide core is centered at $z = 0$ and all waveguide layers are assumed to be semiinfinite in x and y. As illustrated in Fig. 2, this geometry supports both the fundamental, field-antisymmetric TM_0 mode and the symmetric TM_1 mode. Accordingly, each mode will contribute a channel for spontaneous emission decay, with strengths dependent on the dipole position and orientation as well as the emitted frequency.

To ensure proper accounting for all decay channels— including surface plasmon coupling and quenching—the Green's function tensor was calculated using full-field, 3-D finite-difference time-domain simulations. This method has
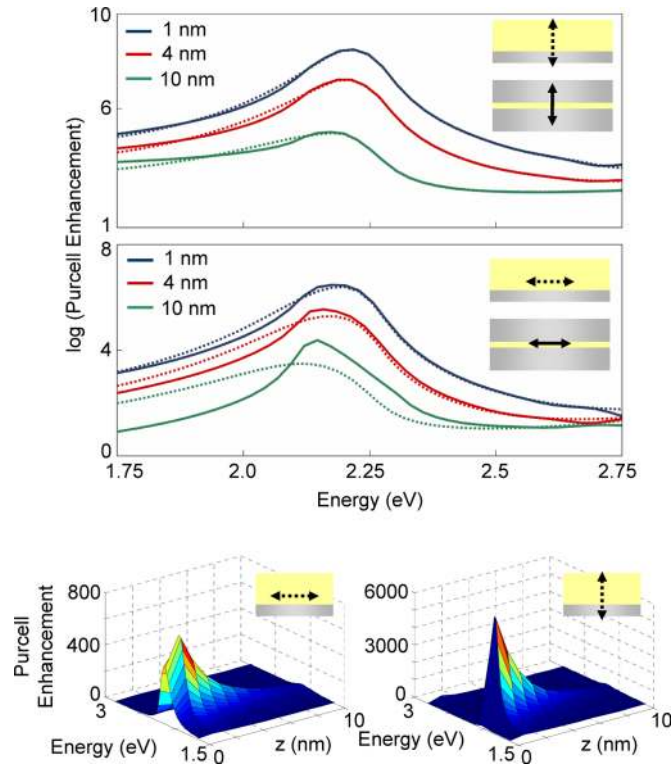
Fig. 8. Simulated Purcell enhancement for Ag/Si/Ag cavities as a function of dipole–metal separation and frequency. Both z- and x-oriented dipoles are considered, and the dipole–metal separation is varied between 1, 4, and 10 nm. For reference, the simulated Purcell enhancements of single Ag/Si interface geometries are also included (dotted lines and bottom graphs). In the upper panels, note that the natural log of the Purcell enhancement has been plotted to highlight the distinctions between MIM and single-interface waveguide cavities.

been used to accurately calculate the LDOS of arbitrary complex dielectric media and photonic crystal nanocavities [51], [83]. Fig. 7(a) shows the Purcell enhancement for a dipole oriented parallel to each metal–dielectric interface; Fig. 7(b) shows the enhancement for a perpendicularly oriented dipole. As expected, for each orientation, the enhancement is highest for frequencies near the surface plasmon resonance. Moreover, the enhancement is highest within a few nanometers (≤ 2 nm) of the metal surface. While Purcell factors for an x-oriented dipole are higher than 600, enhancements of a z-oriented dipole approach 5000. Additionally, large Purcell enhancements (exceeding 100) can be observed a few hundred millielectronvolts from the plasmon resonance.

Fig. 8 highlights this frequency-dependent spontaneous emission enhancement. Both z- and x-oriented dipoles are considered, and the dipole–metal separation is varied between 1, 4, and 10 nm. For comparison, the figure also includes Purcell enhancement factors for a dipole near a single Ag/Si interface. Unlike MIM waveguides, this single metal–dielectric interface will support propagation of only one surface plasmon mode (see Fig. 1).

As expected, spontaneous emission enhancement decays exponentially with distance from a single metal–dielectric interface—behavior consistent with the near-field of a metal-

lic surface. For small dipole–metal separations, very little distinction can be made between the Purcell factor of a single metal–dielectric interface and MIM structures. However, each geometry shows notably different enhancements for larger dipole–metal separations. In particular, an x-oriented dipole spaced $\sim$10 nm from the metal surface of a MIM waveguide shows a twofold enhancement in spontaneous emission at resonance over the single-interface geometry ($F_P^{\mathrm{MIM,10\,nm}} = 78.4$ while $F_P^{\mathrm{IM,10\,nm}} = 30.9$). Interestingly, for wavelengths near the plasmon resonance, the dipole position can be used to selectively discriminate between the TM_1 and TM_0 modes. For example, larger enhancements for the MIM geometry are seen at higher frequencies and larger dipole–metal separations. At these higher frequencies, the MIM TM_1 mode exhibits relatively low loss compared with the TM_0 mode. In other words, larger dipole–metal separations allow selective coupling to the negative-index TM_1 mode. Moreover, while both MIM and single-interface geometries are characterized by broadband enhancements, the MIM enhancement bandwidth is considerably sharper. This spectral response could be desirable for design of on-chip plasmon and photon sources, including lasers and spasers [6].

Experimentally, the ability to engineer on-chip Purcell enhancements requires precise control of emitter properties and position. Colloidal semiconductor nanocrystals may provide a unique platform for such control. Colloidal nanocrystals exhibit vast tunability of emission and absorption wavelengths, a high degree of quantum confinement, and a low defect density. Using colloidal-based techniques, a variety of monodisperse nanocrystal assemblies can be synthesized, spanning the II–VI and III–V semiconductor families with morphologies ranging from dots and rods to tetrapods. Furthermore, colloidal nanocrystals can be synthesized with sizes ranging from tens of nanometers down to 1 nm and emission wavelengths ranging from the ultraviolet to the infrared.

In recent years, techniques have been developed that allow the precise positioning of colloidal nanocystals on-chip, using standard lithography [23] and macroscopic self-assembly [48]. This approach combines top-down CMOS-compatible fabrication with bottom-up, solution-based synthesis. Most significantly, the technique allows single nanocrystals to be systematically placed in well-defined, nanometer-scale junctions, as shown in Fig. 9. Such coupled contact-nanocrystal devices have already been shown to act as single electron transistors [42], [75], and provide a unique opportunity for coupling single electron states with single photon and/or plasmon absorption and emission on a Si chip.

V. Si Plasmonics: Challenges and Projections

As highlighted in this review, plasmonic components are rapidly evolving from discrete, passive structures toward integrated active devices. In part, this progress has been facilitated by opportunities to dispersion engineer metallodielectric systems. Surface plasmons provide access to an enormous phase space of refractive indices and propagation constants that can be readily tuned through variation of material, dimension,
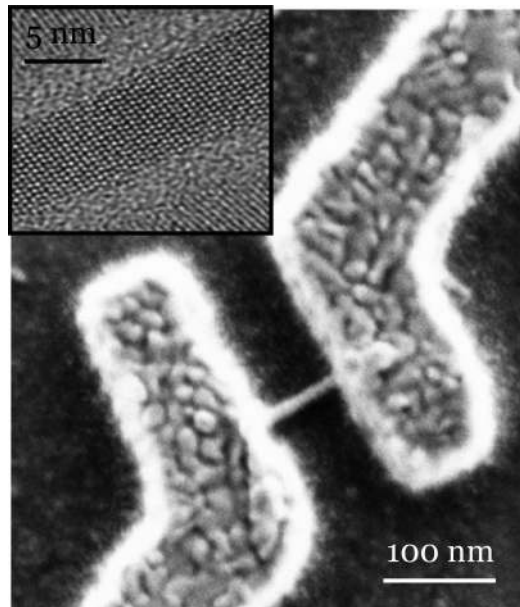
Fig. 9. Two-terminal device consisting of Pd metallic contacts to a single colloidally synthesized nanorod on an Si chip. The inset shows a high resolution transmission electron micrograph of a colloidally synthesized CdSe nanorod.

Fig. 10. Future integrated plasmonic circuit, including: (0) incoupling structures; (1) color demultiplexing in a "Z" add/drop filter; (2) bends and tapers in LR-SPP waveguides; (3) all-optical preprocessing logic; (4) integrated photodetection; (5) optical clock incoupled from free space; (6) nano-optical subcircuit (on-chip integrated light source, electrooptic plasmostor, single quantum dot devices, integrated photodetection); (7) collection of light via "photon sorting"; (8) integrated plasmonic color filtering; and (9) beam shaping of emitted light.

or geometry. Via dispersion engineering, plasmonics has enabled a suite of passive and active subwavelength optical components, including interconnects, negative index metamaterials, optoelectronic modulators, and plasmon-enhanced sources. Plasmonic geometries are also being explored for quantum optics, nonlinear optics, transformation optics, optical antennas, and nano-optical circuits.

The ultrasmall mode size and high local fields of plasmonic architectures can combine the functionality of photonics and electronics on-chip. Still, a number of challenges should be addressed *en-route* to integrated plasmonics. These include: (i) investigating low-loss plasmonic materials, with lower intrinsic absorption than Ag; (ii) developing a surface-plasmon laser that is both frequency-tunable and subwavelength in size; (iii) exciting and detecting surface plasmons on-chip via electrical means; and (iv) demonstrating integrated plasmonic logic.

Despite these challenges, Si-based plasmonic networks may be envisioned for the foreseeable future. Fig. 10 depicts an artistic rendering of a hybrid optoelectronic circuit, synthesizing a number of plasmonic device concepts from the recent literature. On the far left, light arrives from a dielectric waveguide which can be matched with low insertion loss to an LR-SPP waveguide [58]. Wavelength demultiplexing is performed using "Z" drop filters [13], while low-loss tapers and bends direct the LR-SPPs into the densely integrated section of the circuit [22]. A compact, low power all-optical plasmonic switch [62] provides a dynamically configurable interconnect system. Ultimately, the incident LR-SPPs are detected by waveguide-integrated photodetectors [14].

Separately, an optical clock signal arrives as a free space beam, which is captured by a grating and distributed throughout the electronic processor by a branching plasmonic network. Utilizing a planar-comp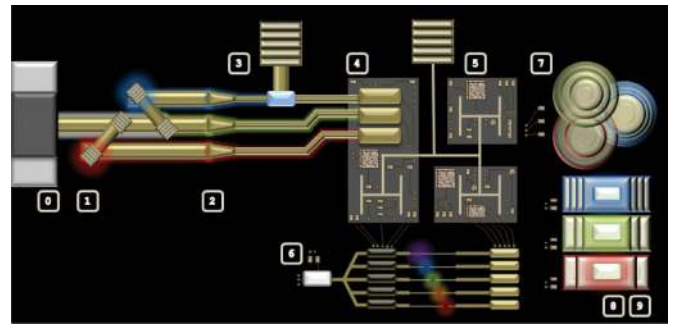act MIM waveguide, this signal could be carried to buried layers as well as across the top surface [17]. The electronic circuit is coupled to a nano-optical subsystem, which employs an on-chip optical train consisting of an integrated plasmonic light source [35], electrooptic plasmon modulators [27], and detectors. Here, the region of interest is represented as nanoguides, which address individual light emitting quantum dots [3]. Other exciting nano-optical systems on chip might include highly integrated chemical or biological analysis arrays that address multiple individual molecules.

Finally, the module contains functionality for receiving and transmitting data by free space optical communication. For detection, a small array of photodetectors is employed, which take advantage of plasmonic collection of light. These concentric rings increase the effective area of the detector, as well as integrating color selectivity [46]. On the output side, in conjunction with an integrated broadband source, the wavelength of emitted light is controlled dynamically by a tunable plasmonic color filter [26]. Whether the output beams emanate from such a plasmonic color display or an alternative light source such as an array of vertically emitting lasers, the output beams are conditioned to have small divergence, using an integrated plasmonic antenna collimator [84].

As noted by Gordon Moore in his seminal 1965 manuscript, *Cramming more components onto integrated circuits* [56], "the future of integrated electronics is the future of electronics itself." Perhaps the same can be said of plasmonics. The promise of plasmonics for Si photonics lies in the ability to combine optical sources, interconnects, modulators, and detectors on the same chip, within subdiffraction-limited dimensions. Such an integrated photonic technology could revolutionize the bandwidth, speed, size, cost, and power requirements of modern computational networks, enabling more efficient solutions to increasingly complex problems.

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