REVIEW

# Silicon carbide and diamond for high temperature device applications

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The physical and chemical properties of wide bandgap semiconductors silicon carbide and diamond make these materials an ideal choice for device fabrication for applications in many different areas, e.g. light emitters, high temperature and high power electronics, high power microwave devices, micro-electromechanical system (MEMS) technology, and substrates. These semiconductors have been recognized for several decades as being suitable for these applications, but until recently the low material quality has not allowed the fabrication of high quality devices. Silicon carbide and diamond based electronics are at different stages of their development. An overview of the status of silicon carbide's and diamond's application for high temperature electronics is presented.

Silicon carbide electronics is advancing from the research stage to commercial production. The most suitable and established SiC polytype for high temperature power electronics is the hexagonal 4H polytype. The main advantages related to material properties are: its wide bandgap, high electric field strength and high thermal conductivity. Almost all different types of electronic devices have been successfully fabricated and characterized. The most promising devices for high temperature applications are pn-diodes, junction field effect transistors and thyristors. MOSFET is another important candidate, but is still under development due to some hidden problems causing low channel mobility. For microwave applications, 4H-SiC is competing with Si and GaAs for frequency below 10 GHz and for systems requiring cooling like power amplifiers. The unavailability of high quality defect and dislocation free SiC substrates has been slowing down the pace of transition from research and development to production of SiC devices, but recently new method for growth of ultrahigh quality SiC, which could promote the development of high power devices, was reported.

Diamond is the superior material for high power and high temperature electronics. Fabrication of diamond electronic devices has reached important results, but high temperature data are still scarce. PN-junctions have been formed and investigated up to 400 °C. Schottky diodes operating up to 1000 °C have been fabricated. BJTs have been fabricated functioning in the dc mode up to 200 °C. The largest advance, concerning development of devices for RF application, has been done in fabrication of different types of FETs. For FETs with gate length 0.2 $\mu$m frequencies $f_T = 24.6$ GHz, $f_{max(MAG)} = 63$ GHz and $f_{max(U)} = 80$ GHz were reported. Further, capacitors and switches, working up to 450 °C and 650 °C, respectively, have also been fabricated. Low resistant thermostable resistors have been investigated up to 800 °C. Temperature dependence of field emission from diamond films has been measured up to 950 °C. However, the diamond based electronics is still regarded to be in its infancy. The prerequisite for a successful application of diamond for

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the fabrication of electronic devices is availability of wafer diamond, i.e. large area, high quality, inexpensive, diamond single crystal substrates. A step forward in this direction has been made recently. Diamond films grown on multilayer substrate Ir/YSZ/Si(001) having qualities close those of homoepitaxial diamond have been reported recently.
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## 1. Introduction

The electronic revolution of the 20th century is mainly based on silicon which can be regarded as the first generation semiconductor. Around the turn to the 21st century gallium arsenide and indium phosphide have evolved as second generation semiconductors constituting the base for the wireless and information revolution. Now at the start of the 21st century, the wide bandgap semiconductors silicon carbide and gallium nitride are on the rise and maybe regarded as third generation semiconductors used in the electronic and optoelectronic industries. Moreover given diamond's superior properties and the recent surge of research on diamond preparation and fabrication of diamond based electronic devices, one might speculate that diamond may be the future generation semiconductor.

The effects of temperature on materials and devices have been of great interest throughout the history of semiconductor research. The aim has been to investigate the high temperature limits of materials and to enhance high temperature semiconductor device performance. The development of semiconductor devices for reliable operation for an extended period at high temperatures is a complex process in which a number of physical effects connected with increasing temperature [1, 2] have to be considered. The term high temperature is not defined in a unique way in the literature and has a different meaning depending on the semiconductor under consideration and the area of application of semiconductor devices. The definition of high temperature often cited in the literature is temperatures above 125 °C [2, 3], since 125 °C is frequently specified as the upper limit at which standard commercial silicon devices function properly, although tests on standard commercial components indicate that even 150 °C maybe be applicable to selected silicon components [3].

Silicon is still the dominant semiconductor and silicon devices are still being developed. The most common and cost effective integrated circuit technology is now silicon CMOS which is able to operate up to 200 °C. The SOI (Silicon On Insulator) technology extended the operational temperature of CMOS circuits to 300 °C [4–8]. In addition, devices based on gallium arsenide and related alloys devices which are commercialized to a lesser degree than silicon, are also candidates for high temperature operation beyond 300 °C. The short term operation of GaAs devices at temperatures as high as 500 °C has been reported [9, 10].

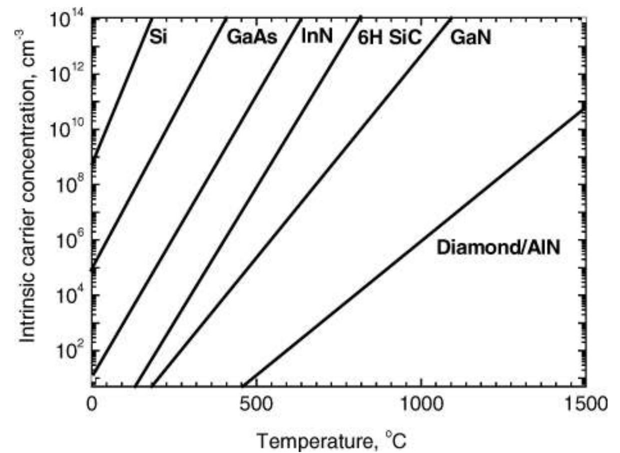


*Figure 1* Intrinsic carrier concentration as function of temperature of several semiconductors (ref. [9]).

A survey of the literature indicates that 300 °C can be regarded as a dividing point from several standpoints, e.g. packaging, wiring, connecting, etc. [1, 2, 4]. This temperature is approximately the maximum temperature at which low-power silicon or conventional gallium arsenide devices can function reliably. The intrinsic carrier concentration for several semiconductors as function of temperature is shown in Fig. 1. The control of the free carrier concentration is vital for the performance of all semiconductor devices. The intrinsic carrier concentration ($n_i$) is exponentially dependent on the temperature:

$$n_i = \sqrt{N_C N_V} e^{-E_G/2kT} \quad (1)$$

where $E_G$ is the bandgap, $k$ is the Boltzmann constant and $T$ is the temperature in Kelvin. Evidently, at temperatures above 300 °C, SiC, GaN and diamond and AlN have much lower intrinsic carrier concentrations than Si and GaAs. This implies that devices designed for higher temperatures should be fabricated from wide bandgap semiconductors, to avoid the deteriorating effects of thermally generated carriers.

The wide bandgap third generation semiconductors, SiC and GaN (including the III-nitrite systems e.g. AlGaN), have been recognized for over three decades as materials which are well suited for high temperature electronics and for light emitters, but until recently, the low material quality has not allowed the production of

high quality devices. The availability of single crystal SiC wafers at the start of the nineties initiated a great deal of activity towards the development of SiC based devices, and their commercialization started with the release of blue light emitting diode (LED). The availability of commercial high quality substrates meant that more research has been carried out on SiC than on GaN and III-nitrite systems. The SiC devices have the advantages of a more mature semiconductor material growth and device fabrication technology. Furthermore, GaN and III-nitrite crystals have mostly been grown by heteroepitaxy on e.g. sapphire and SiC, since a viable GaN substrate technology does not exist. Unfortunately, GaN crystals always contain more defects than SiC and the current aim is to reduce the surface defect densities in GaN from current densities of the order $10^8$ $cm^{-2}$ to $10^5$ $cm^{-2}$. The unavailability of low defect density substrates and defect free material limits the ability to fabricate high quality GaN devices. The discussion of wide bandgap semiconductors must mention AlN since it has one of the largest bandgaps (wurtzite: 6.23 eV and zincblende: 6.0 eV [11]). The growth of defect free AlH crystal (as with the GaN) is an outstanding issue. The reduction of the defect density and the effects of specific defects of third generation semiconductors are the most urgent current problems that must be solved. Diamond is a future generation semiconductor which is at a different stage of research than the third generation semiconductors, particularly SiC, which is far more developed then diamond.

The research in wide bandgap semiconductors has been driven by the need for light emitters, high temperature and high power industrial applications, and microwave power applications. A variety of applications e.g. in aircraft and space systems, automotive electronics, deep well drilling, energy production centers etc., would benefit by power devices that function at high temperatures [12–16]. When the ambient temperature is too high, the performance enhancing electronics presently used to beneficially monitor and control crucial hot sections must reside in cooler areas, this is achieved by their remote location or actively by cooling with air or liquid. These thermal management approaches introduce additional overhead that can have a negative impact relative to the desired benefits when considering the overall system performance. The additional overhead, in the form of longer wires, more connectors and plumbing for the cooling system, can add undesired size and weight to the system, and an increased complexity corresponding to an increased potential for failure. The economic benefits of high temperature electronics for various systems are likely to be orders of magnitude greater than the total market for actual high temperature electronics. The world market for high temperature electronics between 2003 and 2008 is predicted to increase from 400 to 900 millions US-dollars, which is substantially lower than the world's total semiconductor electronic market [1]. The situation can be dramatically described as follows, a mere handful of high temperature electronic chips that may cost a few hundred dollars, can optimise the performance of a very large number of systems thus saving many millions of dollars, e.g. deep-well drilling [5].

A survey of the potential industrial users of high temperature electronics revealed that the majority of applications for high temperature electronics operate in the range 150–300 °C [1, 2, 4]. The recent development of silicon and gallium arsenide electronics and their cost (silicon technology is much cheaper than SiC), indicates that wide bandgap semiconductor devices are unlikely in the near future to be used in low power electronics applications for temperatures up to 300 °C. These devices maybe used for application which cannot be satisfied by available technologies such as SOI, and for temperatures above 300 °C. However, in order to realize viable low power SiC devices for the temperature range 300–600 °C, the long term reliability of electronic circuits must be achieved [1].

The performances of silicon power devices have almost reached their theoretical limits [17]. The practical operation of Si power devices at ambient temperatures higher than 200 °C appears problematic, as self-heating due to current flow at higher power levels results in high internal junction temperatures and leakage. The overall goal for high temperature power electronic circuits is to reduce power losses, volume, weight, and at least the costs of the system. The continuous progress in high temperature electronics creates a demand for unique material properties, novel processing technologies and electronic devices. The physical and chemical properties required for meeting the demands of the high-temperature and high-power applications can only be found in wide bandgap semiconductors which offer a number of advantages over corresponding devices fabricated from silicon. These include higher temperature stability, higher chemical stability, higher thermal conductivity, and higher breakdown field. Various device implementations not only use these standard semiconductor parameters, but also the special peculiarities these materials exhibit, e.g. aluminium nitride and gallium nitride, unlike diamond and silicon carbide, have a direct bandgap and have complete miscibility with each other and with indium nitride. This is important for the implementation of optoelectronic device since it allows the bandgap to be controlled, and thus the wavelength of the spectral characteristic maximum [4]. The wide badgap silicon carbide and diamond are next discussed in this review.

The properties of silicon carbides make it an excellent material for high power devices operating at temperatures up to 600 °C and above, and at frequencies around 20 GHz. Within power electronics, SiC has the potential to replace Si based diodes and IGBTs (Insulated Gate Bipolar Transistor), and Si-GTO thyristors

(Gate Turn-Off), which are part of the mass market of discrete power devices in general and in converter systems in particular. The power losses in SiC switches are two orders of magnitude lower compared with Si devices, thus SiC devices have a large potential for applications in e.g. uninterrupted power systems (UPS), motor controls, etc. The maximum operating temperature of a Schottky diode in SiC may be limited by an increasing leakage currents, but active power devices for operation at high temperature has been presented. UMOSFET (U-shaped trench Metal Oxide Semiconductor Field Effect Transistor) made from SiC that operate up to 450 °C and thyristors (6 A, 700 V) that operate at 350 °C have been presented. Furthermore, SiC MOSFETs have been reported to operated even at 650 °C, and devices based on NMOS (n-type channel MOS) (which is an integrated operational amplifier) have been reported to work at 300 °C [18–22]. The properties and preparation of SiC are elucidated in the next section.

Among the wide bandgap semiconductors, diamond has the most superior physical, chemical and electrical properties [23], unmatchable by any other material. The properties of interest relevant to high temperature high frequency power electronics are the large bandgap energy (5.5 eV), the breakdown electric field (10 MV/cm), the carrier mobilities (~2200 and ~1600 $cm^2$/Vs for electrons and holes resp.), the thermal conductivity (10–20 W/cmK), the low dielectric constant (5.5), and the excellent resistance to radiation. Diamond can be found naturally or must be sythesized. In nature diamond occurs as single crystals only, whereas the synthetic diamond can be prepared as single crystals, or as a polycrystalline or as a nanocrystalline material.

The discovery that diamond can be grown by CVD technique has opened up some of the expected applications of diamond. However, the utilization of diamond's many unique properties in electronics has so far been limited among others by the unavailability of large area high quality diamond and that only p-type (acceptor type impurity) diamond with high hole densities are available today. The n-type (donor type impurity) diamond with high electron densities would find many applications, apart from the fundamental interest to realize pn-junctions and other electronic devices in diamond. The n-type diamond is expected to be a better electron emitter for field emission, photo emission, and ion or electron impact induced emission, and may also serve as a better inert electrode for electrochemical applications.

Nevertheless, many studies have been reported with natural, high-pressure high-temperature (HPHT) synthesized and polycrystalline CVD diamonds [24, 25]. The pn-junctions were formed from boron and phosphorus doped diamond films, and from boron and nitrogen doped diamond films, respectively. The diamond films with high crystalline perfection were grown epitaxially on diamond single crystals. The I–V (current–voltage) characteristic of the boron/nitrogen pn-junction diode was studied up to 400 °C. The combination of two boron/nitrogen pn-junctions, a BJT (bipolar junction transistor) which can operate in DC mode up to 200 °C was fabricated. The fabrication of many types of FETs (Field Effect Transistors) for both DC and RF modes has crossed many important milestones. The cut-off frequency of 1.7 GHz and a maximum drain current of 360 mA/mm were measured for a MESFET with a gate length 0.2 $\mu$m. Recently, a FET functioning up to 81 GHz was reported by a collaboration between Nippon Telegraph and Telephone Corp. and the University of Ulm in Germany. The research groups fabricated T-shaped gates on a diamond layer with a carrier mobility of 130 $cm^2$/Vs [26]. In addition, Schottky diodes that function up to 1000 °C were fabricated from either single crystal or polycrystalline diamond. The low resistant thermostable resistors deposited on ceramic substrates have been investigated for temperatures up to 800 °C. The temperature dependence of the field emission of nitrogen doped diamond films has been investigated for temperatures up to 950 °C.

There has been much progress in the fabrication of diamond based electronic devices and several types of devices have reached an important stage in their development. However, despite these developments diamond based electronics is still in its infancy.

## 2. Material properties and preparation

### 2.1. Silicon carbide

The properties of silicon carbide's makes it an excellent material for devices operating at high temperatures (600 °C and higher), high power (4H-SiC transistor: presently RF output power on the order of 5 W/mm), and high frequency (RF through X band (5.2–10.9 GHz) potentially to *K* band (20–40 GHz)). The large bandgap of silicon carbides (2.2, 3.26 and 3.0 eV for 3C-SiC, 4H-SiC and 6H-SiC respectively) compared to the bandgap of silicon (1.1 eV) enables devices to function at temperatures beyond 600 °C. The very high breakdown electric field of these materials (~1.8, 3.5 and 3.8 MV/cm for 3C-SiC, 4H-SiC and 6H-SiC respectively) which are approximately 10 times higher than of Si (0.3 MV/cm, allows a reduction of the thickness of the conduction regions (for constant doping) which results in very low specific conduction resistance. The 4H-SiC junctions exhibits a negative temperature coefficient, with a breakdown voltage that decreases by about 8% within the temperature range from room temperature to 623 °C [27]. The high thermal conductivity (~4–4.5 W/cmK) permits a power density increase which fascilitates a more compact or much higher power per area. The high saturation velocity of all three types of silicon carbide is high $\sim 2 \cdot 10^7$ cm/s compared to the value for silicon ($1 \cdot 10^7$ cm/s). The low carrier mobilities of silicon carbide is a disadvantage which limits RF performance at frequencies above the X band. The electron mobilities

TABLE I Approximative values of physical properties for some semiconductors

| Name | Bandgap $E_g$ (eV) | Maximum electricfield V/cm | Dielectric constant $\varepsilon_s$ | Thermal conductivity W/cmK | Carrier mobility cm$^2$/Vs |
|---|---|---|---|---|---|
| Si | 1.1 | $3 \times 10^5$ | 11.8 | 1.5 | 1350 |
| | | | | | 480 |
| GaAs | 1.4 | $3.5 \times 10^5$ | 10.9 | 0.8 | 8600 |
| | | | | | 250 |
| SiC | 3.3 | $2.5 \times 10^6$ | 9.8 | 4.9 | 980 |
| | | | | | 200 |
| GaN | 3.4 | $2 \times 10^6$ | 7.8 | 1.4 | 2000 |
| Diamond | 5.5 | $1 \times 10^7$ | 5.5 | 10–20 | 1800 |
| | | | | | 1600 |

are of the order 900, 500 and 200 cm$^2$/Vs for 3C-SiC, 4H-SiC and 6H-SiC respectively. The hole mobilities are of the order of 50 cm$^2$/Vs for all three types of SiC (for Si: ~1350 and ~500 cm$^2$/Vs for electrons and holes respectively). The carrier mobilities of SiC are adequate however, for high power devices in the X band. The properties of silicon carbide and diamond relevant for electronics are given in Table I.

Noteworthy, is that silicon carbide has a close lattice match with III-nitrides, which makes it a preferred substrate material for nitride-based electronic and optoelectronic devices. The commercial production of large size substrates which have improved electronic and optoelectronic properties constitutes a milestone in their application. These materials have been used (among others) for a large production of green, blue and ultraviolet light emitting diodes. Unfortunately, unavailability of high quality defect free SiC substrates is slowing down the pace of transition from research and development to production of SiC devices, which may include high-power solid-state switches or diodes for electrical power control, and high power density microwave transistors.

Silicon carbide occurs in a large number of polytype structures. The number of polytypes in the literature varies between 150 and 250. These polytypes are differentiated by the stacking sequence of the biatomic closed packed layers. A detailed study of silicon carbide's polytypism was done in [28]. The most famous polytypes are the hexagonal 4H and 6H, cubic 3C, and rhombohedral 15R structures. Not all types are easy to grow, only 4H and 6H polytypes are available as substrate materials. In a single bilayer of SiC each C atom is tetrahedrally bonded to four Si atoms–to three ones within the layer and to one in the next layer. Looking at a bilayer from the top in the direction of the c-axis [0001], the C atoms form a hexagonal structure as shown in Fig. 2(a) and (d). These are labeled as A. The C atoms of the next biatomic layer have the option to be positioned at the lattice sites 'B' or 'C' as shown in Fig. 2(b) and (c), respectively. This is the stacking sequence defining a polytype. Fig. 2(d) shows schematically the first bilayer with six C atoms forming the hexagonal structure and the option positions for the three C atoms in the next layer beyond the first layer. Fig. 2(e)–(h) shows the stacking sequence for the most

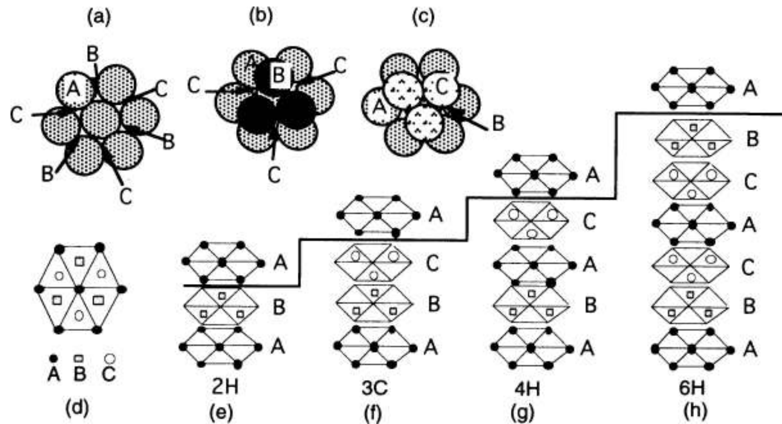


*Figure 2* The stacking sequence of double layers of the four most common SiC polytypes, (a) locations of C atoms, labeled as A, in the first biatomic layer in {0001} plane; (b), (c) optional positions of C atoms, labeled as B and C resp., in the next biatomic layer above the first layer; (d) first biatomic layer with six C atoms and the optional positions of the three C atoms in the next biatomic layer, (e)–(h) stacking sequence of the most common SiC polytypes. The solid line indicates the completion of the unit cell in [0001] direction.

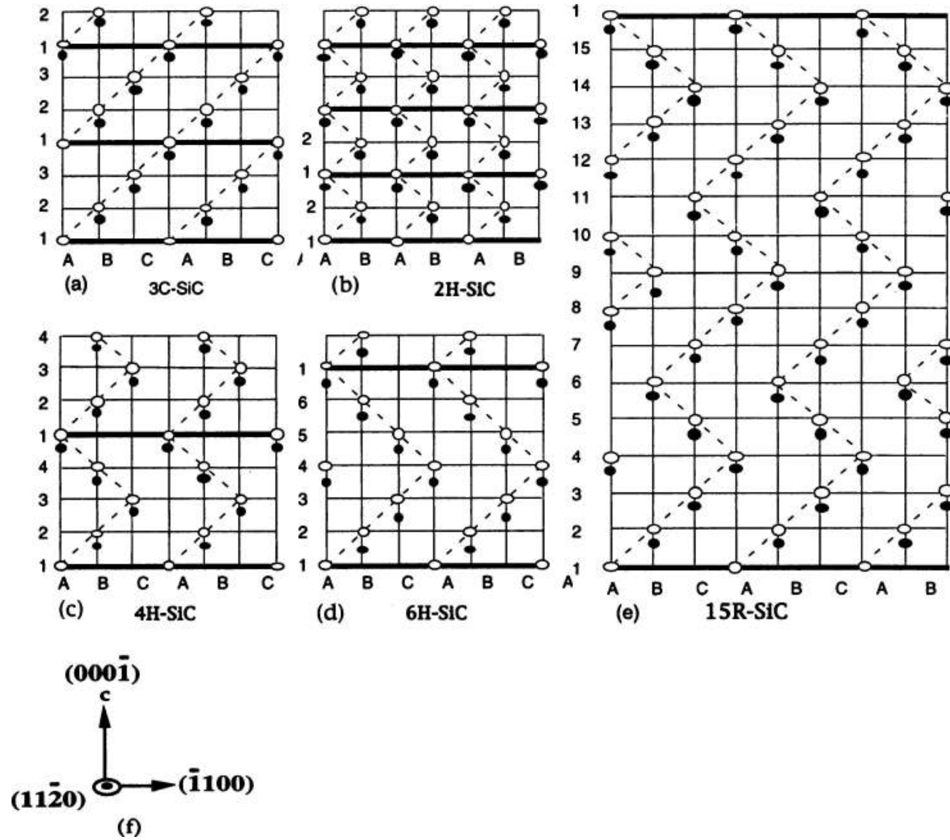


*Figure 3* Schematic representation of the structure of the most common SiC polytypes viewing in the {11$\bar{2}$0} plane. The black dots represent C atoms and the open circles represent Si atoms. The bold line indicate the completion of the unit cell in [0001] direction.

common SiC polytypes. The change in sequence has an impact on the properties of the material, for example the bandgap changes from 3.4 eV for 2H polytype to 2.4 eV for 3C polytype. Fig. 3(a)–(e) shows the structure of the most common SiC polytypes viewing in the {11$\bar{2}$0} plane, i.e. in the [0001] direction.

The leading manufacturer of substrates is Cree Inc., though new manufacturers have recently appeared. The crystalline quality in terms of a low defect density, and a specially low micropipe density the substrates of Cree Inc. are still ahead. The preperation of silicon carbide is complicated by the fact that it does not melt, it sublimates at temperature above 2000 °C, thus standard growth techniques, e.g. the Czochralski process by which large single-crystal ingots are produced by pulling a seed crystal from the melt, cannot be used. Silicon carbide crystals are grown by a sublimation method first developed by Lely in 1955 [29], and later extended to a seed sublimation technique by Tairov and Tsvetkov in 1978 [30]. This method is also termed physical vapour transport (PVD) growth. The crystals are grown by SiC deposition derived from Si and C molecular species provided by a subliming source of SiC placed in close proximity to the seed wafer.

A new high temperature CVD (HTCVD) technique was developed in 1999 [31] where the growth rate can be tuned in such a way that a high quality thick epitaxial layer with precisely controlled doping levels can be grown in a few hours, which is fast compared to conventional CVD which takes days to grow a similar structure. As an alternative to CVD, sublimation epitaxy has also been demonstrated for the growth of thick epitaxial layers. The growth rate in sublimation epitaxy is also very high, of the order of few hundred micrometers an hour. In devices where the control of the doping level is an important issue, sublimation epitaxy has been shown to work successfully.

The commercial availability of SiC substrates with increasing diameter and quality has been a prerequisite for the advances in SiC device technology. The SiC substrates are available in two different polytypes, namely 6H- and 4H-SiC. The latter is relevant for electronic application due to its higher carrier mobility and wider bandgap than 6H-SiC. SiC substrates have been in the market for over a decade, but the absence of defect free growth is slowing down the pace of transition from research and development to the production of power devices such as high-power solid-state switches or diodes for electrical power control and high power density microwave transistors. Three-inch 4H-SiC substrates have been commercially available since 2001, but it was only recently that their defect concentration have been reduced to levels that allows for the fabrication of commercially viable high power switches.

During 2003 Infineon and Cree Inc. released 10 A devices, which is clear evidence that substrates have reached an acceptable level of quality.

The important defects of SiC are different types of dislocations. The open core screw dislocations called micropipes are of particular concern for SiC due to their detrimental effects on power devices. The micropipes cause diodes to fail for voltages which are much smaller than the voltage at which avalanche breakdown occurs [32]. Progress in the development of the PVT technique during the last four years, has resulted in a significant reduction of the micropipe density in 3 inch 4H-SiC wafers, from a previously typical value above 100 $cm^{-2}$ to a value as low as 0.22 $cm^{-2}$ in R&D samples. The micropipe densities in commercially available substrates are $<30$ $cm^{-2}$ and $<80$ $cm^{-2}$ for n-type and semi-insulating materials, respectively. The 100-mm 4H-SiC wafers are now under development. The micropipe densities for such wafers are $\sim$22 $cm^{-2}$ and $\sim$55 $cm^{-2}$ for n-type and semiinsulating crystals, respectively [33, 34].

Low angle grain boundaries also known as domain walls, is an other class of defect which has to be reduced, since it is associated with leakage currents and failure in devices, and may cause wafers to crack during epitaxial processing. This type of defect can be observed through whole wafer X-ray topography, though it is difficult to obtain quantifiable numbers on the wafer quality by such measurements. This defect seems to be intimately related to the growth method used [35]. A class of defects known as threading screw dislocations are suggested to have an impact on the leakage behavior of Schottky diodes. The evidence suggests that these defects are introduced at the seed/growth interface by seed subsurface damage. The application of seed treatment reduces the density of dislocations in a 3 inch 4H-SiC wafer from a value of the order $3 \cdot 10^4$ $cm^{-2}$ to $3 \cdot 10^3$ $cm^{-2}$ [34]. The so-called basal plane dislocation is another important and significant defect. It has been shown that PiN device structures are susceptible to severe degradation of the forward voltage characteristics due to the presence of these defects in the active layer of the device [36]. The presence of these dislocations increases the resistance of the active layer of the device. It is critical to reduce the density of these dislocations in epitaxial layers for stable device production. A level of basal plane dislocations in the substrate which may be acceptable in order to allow reasonable yields of PiN diods, is on the order of 100 $cm^{-2}$. The average density of the basal plane dislocations in 3-inch 4H-SiC wafers is $1.5 \cdot 10^3$ $cm^{-2}$ [34]. Recently it was reported that this type and even other types of dislocations and defects can be reduced by growing the material along a-face direction [37]. The single crystals of SiC are usually grown by the method termed c-face growth where crystals are grown along the [0001] c-axis direction using a seed of {0001} substrate. The new method known as a repeated a-face growth process, single crystals are grown along the a-axis $[11\bar{2}0]$ or $[1\bar{1}00]$ (both axis are called a-axis in the report) direction in several steps. The a-face growth process is shown in Fig. 4.

The electrical properties of SiC substrates are related to the purity of the as-grown crystals. The substrate purity is dominated by the presence of residual nitrogen and boron impurities. The level of these impurities is critical for the production of undoped high purity semi-insulating substrates with uniform and stable semi-insulating properties. High purity 3-inch and 100 mm 4H-SiC substrates with low micropipe densities and uniform semi-insulating properties ($>10^9$ $\Omega$cm) over the full wafer diameter have been produced. These wafers had typical residual level contamination densities $5 \cdot 10^{15}$ $cm^{-3}$ and $3 \cdot 10^{15}$ $cm^{-3}$ for nitrogen and boron respectively [38].

Although most doping of SiC is obtained by an in situ method during epitaxial growth, additional selected area doping is often required during fabrication of devices such as MOSFETs and lateral bipolar transistor. Due to the extremely low diffusion coefficient of dopant atoms in SiC even at very high temperatures ($\sim$2000 °C), ion implantation is the only viable doping technique during device fabrication. The critical parameters of the ion implantation of dopants in SiC are the temperature of SiC during implantation (from room temperature up to 900 °C), as well as the subsequent annealing required to activate the dopant performed at around 1700 °C. Nitrogen is typically used as the n-type dopant, while Al is often the p-type dopant widely used during epitaxy. The element boron is a lighter element than Al and subsequently causes less lattice damage during implantation, and may eventually replace Al. However, a small amount of B also diffuses into the lightly doped drift layer side during the annealing process thereby degrading the junction.

The high bond strength of SiC means that a room temperature wet etches for this material does not exist, and so RIE (Reactive Ion Etching) is the standard method used. Frequently fluorine-based chemistries are used in which the silicon forms a volatile $SiF_4$ molecule and C is removed either as $CO_2$ or $CF_4$. However, RIE is not regarded as a limitation since as feature sizes decrease, dry etching processes are actually preferred to wet etching.

A unique advantage of SiC compared to other wide bandgap semiconductors, is its ability to oxidize and form $SiO_2$ exactly as in Si technology. The oxidation rates are much lower for SiC than for Si, and are very dependent on if a silicon- or carbon-terminated face is exposed to the growing $SiO_2$. The fabrication of high quality thermal oxides with low interface state and oxide trap densities has proven to be a great challenge. Finally, the reliability of oxides is a major issue for SiC devices since at high electric fields and high temperatures oxides have poor longevity. This issue needs further research

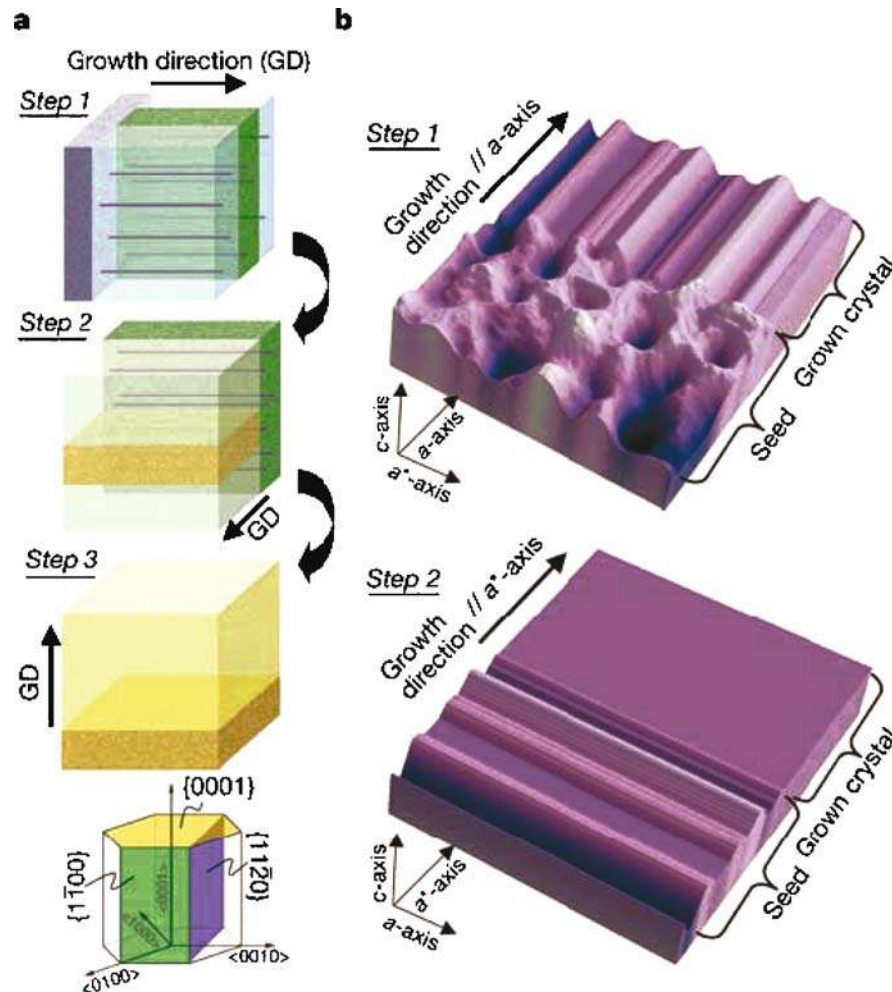


*Figure 4* Schematic picture of the a-face growth of SiC (ref. [37]).

to reduce the leakage current in the devices that operate at elevated temperatures.

An important issue in high temperature electronics is the type of metallizations used where examples include ohmic, Schottky, heat-sinking and capping. It is necessary to have reasonable thermal expansion matching and a good adhesion of the metal and SiC. The wide bandgap of silicon carbide makes it difficult to control the electrical properties at the metal-semiconductor interface of devices. In addition, stable non-corrosive contacts are also key issues in high temperature electronics. The main parameter of concern for SiC high-frequency devices is a stable Schottky barrier for good rectification and a low reverse leakage current while operating at elevated temperatures. Several groups have tried different combinations of transition metals that form good Schottky contact on n- and p-type SiC with barrier heights in the range of 0.9–1.7 eV [20, 39–41]. The rectifying properties either change to ohmic or degrade severely while operating at temperatures above 600 °C. Among the ohmic contact the most widely used material for n-type is $Ni_2Si$ which is generally formed by deposition of Ni film and silicidation is obtained by annealing at above 900 °C. The $Ni_2Si$ ohmic contact has been shown to be stable at very high temperatures [39, 42]. The formation of low-resistance ohmic contacts to p-type SiC is still difficult since metals with sufficiently large work functions are not available to offset the wide bandgap and electron affinity of SiC. Aluminum is typically used to form p-type ohmic contact. A major drawback of Al however is its relatively low melting point, which prohibits its use for high temperature applications. Several other combinations of different metals have also been reported in the literature these have poor contact resistivities compared to Al [43, 44]. A special effort is required to develop stable contacts for SiC devices operating at higher temperatures, and metals with a high melting temperature and their silicides and carbides should be studied in the future towards this goal.

The packaging of SiC devices for high-power and high-frequency applications and operation at elevated temperature is an issue which has been neglected compared to material growth and device processing technology. It is highly desirable to find suitable packaging for high temperature electronics which can endure high

thermal stress and high power without the extra effort of cooling.

## 2.2. Diamond

Among the wide bandgap semiconductors, diamond has the most superior properties, unmatchable by any other material [45–49]. Most electrical, thermal and optical properties of diamond are extrinsic, i.e. strongly dependent on the impurity content [23, 46]. The most common impurity being nitrogen. Diamond has large bandgap (5.5 eV), high breakdown electric field (10 MV/cm), low dielectric constant (5.66–5.70), high carrier mobilities ($\sim$1800 and $\sim$1600 cm$^2$/Vs for electrons and holes resp. [45]), high saturated carrier velocity ($2.7 \cdot 10^7$ cm/s and $1 \cdot 10^7$ cm/s for electrons and holes resp.), high thermal conductivity (10–20 W/cmK), high resistivity ($10^{13}$–$10^{16}$ $\Omega$cm), low thermal expansion coefficient (1.1 ppm/K at R.T.), highest sound velocity ($1.833 \cdot 10^6$ cm/s), exceptional hardness (10000 kg/mm$^2$) and wear resistance, low friction coefficient (0.05 (dry)), broad optical transparency (from 225 nm to far IR), excellent resistance to radiation, chemical and thermal stability. A unique feature of diamond is that some of its surfaces can exhibit a very low or negative electron affinity. Obviously diamond is the material of choice for many applications, including electronics. The properties of diamonds make it the most suitable semiconductor for power electronics at high frequencies (RF radio frequency) and high temperatures [50–53]. Since diamond like silicon is a single element semiconductor it is less susceptible to have a high density of structural defects that are usually present in compound semiconductors. However to date, diamond is regarded as one of the most difficult semiconductors to synthesize for the fabrication of electronic devices.

Diamond is cubic semiconductor with lattice constant $a = 3.566$ Å. The covalent bonding of the carbon atoms (sp$^3$ bonds) is extremely strong and short, which gives diamond its unique physical, chemical and mechanical properties [46–49]. Diamond is available naturally and can also be synthesized. The natural form of diamond occurs as single crystals, whereas the synthetic diamond can be prepared as single crystals, or as polycrystalline or nanocrystalline material. Usually natural diamond single crystals have a high nitrogen content and cannot be used for the fabrication of electronic components. There are several classifications according to different criteria of the natural diamond. The physical classification, used frequently in connection with the preparation of the diamond, is based on the optical absorption of nitrogen, boron and hydrogen related defects and paramagnetic absorption of single substitutional nitrogen. According to this classification there are two basic types of diamond, type I and type II. These two basic types are devided into several types, designated Ia, Ib, IIa, IIb, etc, depending on the type of the impurity and defects introduced by the impurities in diamond. Nitrogen is an important impurity in diamond because it deteriorates the exceptional properties of the diamond. So, diamond materials exhibiting optical and paramagnetic absorption dominated by different nitrogen defects are classified as the type I. Natural type I diamond contains normally several impurities in comparison with the type II diamond. The most evident difference between type I and II is obtained from IR absoption spectra considering it thus as the main criterion for the differentiation. About 74% of natural diamonds are classified as the type I. The type II classified diamonds exhibit no optical and paramagnetic absorption due to any nitrogen related defects. Only about 1% of the natural diamonds do not exhibit absorption due to the nitrogen related defects. The diamonds exhibiting no optical absorption due to boron and hydrogen impurities in the one phonon region, having nitrogen concentration less than $10^{18}$ cm$^{-3}$, are classified as type IIa. Diamonds of this type are the most transparent ones. A detailed description of the selection criteria for the classification of diamonds can be found e.g. in [46, 54].

Diamond melts at approximately 3827 °C [45]. It is stable at elevated temperatures, but the stability depends on the ambient. In hydrogen ambient diamond is stable up to 2200 °C [55], but it is graphitized in vacuum [56, 57] or in an inert gas [56]. Diamond does not have a native oxide, but it oxides in air at elevated temperatures. This is a critical point for the application of diamond for high temperature devices. The oxidation of natural and synthetic diamond has been studied since the beginning of the sixties. Despite this, discrepancies in the literature indicate that more research is needed for a complete understanding of the oxidation process. The activation energy for the oxidation of CVD grown films in air was 213 kJ/mol for temperatures between 600°C and 750 °C and the oxidation proceeded by etching pits into the CVD film thus creating a highly porous structure [58]. The results of several studies indicated that diamond oxidized preferentially. The oxidization of natural diamond and CVD grown diamond films in oxygen has been observed to be dependent on the crystallographic orientation, here the (111) plane oxidized more easily than the (100) and (220) planes, and also the CVD films were less resistant to oxidation than the natural diamond [56, 59]. Sun *et al.* [56] observed that the oxidation of synthetic diamond started in air at 477 °C when oxygen is able to impinge into the densely packed (111) planes and they suggested that the oxidation of diamond occurs by the same mechanism as the corrosion of metals whereby oxygen penetrates into the bulk by bonding and rebonding, leaving behind weakly interacting dipoles which are eroded away during processing. Lu *et al.* [60] reported that the oxidation in air of diamond films prepared by d.c. arc plasma jet started at 650 °C which was about hundred degrees lower than the temperature of oxidation of natural diamond. Furthermore,

it was reported that the oxidation rate of CVD diamond depended on the diamonds growth condition [61].

There are several etchents for diamond. The most commonly used method is oxidative etching. The effects of dry oxygen and a mixture of oxygen and water in the temperature range 700–900 °C has been studied and compared with the effect of molten potassium nitrate [62, 63].

Diamond-based electronic devices have now been fabricated from natural and synthesized single crystals, high purity single crystal films (homoepitaxial diamond), and from polycrystalline films (heteroepitaxial diamond). Single crystals can be synthesized artificially by the (HPHT) method (high-pressure high temperature), which mimics the process used by nature. The drawback of this method is that it produces single crystals limited in size. The largest crystals prepared by this method have a dimension of the order of millimeters, and the processing time to produce such crystal is very long [64]. These crystals have been used for the fabrication of discrete electronic devices and as substrates for homoepitaxial growth of diamond films by CVD technique. Diamond films have been epitaxially deposited on diamond single crystals substrates, this demonstrates that single crystal diamond deposition is possible by low pressure processing [65, 66].

The discovery that diamond can be grown homoepitaxially and heteroepitaxially by chemical vapor deposition (CVD) technique has opened up some of the expected applications of diamond. The history of this technique goes back to the late sixties. During the eighties researchers [67, 68] made a series of discoveries which enabled them to grow, at significant growth rates, diamond films of high quality on non-diamond substrates by using hot filament CVD and subsequently by microwave plasma chemical vapor deposition (MPCVD). This started a worldwide interest in diamond CVD for both research and technology. Since then a number of low pressure CVD techniques have been developed [69, 70] and the volume of research on the preparation of large area diamond films has been very intense.

It has been shown recently [71, 72] that homoepitaxial growth of diamond films on high quality HPHT diamonds can produce single crystal films of a purity that exceeds the purity of the purest diamonds found in nature. The measurements of the carrier mobilities in these films have revealed interesting results such as mobilities of 4500 and 3800 $cm^2/Vs$ for the electrons and holes respectively. These values are the highest ever reported for diamond and are approximately twice as high as those found in pure natural diamond. The carrier mobility measurements were performed on homoepitaxial diamond deposited by a microwave plasma assisted CVD technique and a HPHT diamond single crystal of dimensions 4 by 4 by 0.5 mm was used as the substrate. The homoepitaxial diamond film was found to be of exceptional purity and it was found to contain a low concentration of intrinsic and extrinsic defects. The total measured nitrogen concentration was less than $1 \cdot 10^{15}$ $cm^{-3}$ and the dislocation density was less than $10^6$ $cm^{-2}$. The exceptionally high values of the carrier mobilities were attributed to the low defect and dislocation densities.

The disadvantage of diamond homoepitaxy is that only small area single crystal can be fabricated, and substrates typically have a size of the order of millimeters. In order to exploit diamond's superior properties for the fabrication of electronic devices, thin diamond films are required, i.e. a method for the production of large area, inexpensive single crystal films with a low defect density.

Dispite the progress made, the available diamond homoepitaxy methods cannot solve the technological problem of producing large area diamond wafers for the fabrication of electronic devices. During the last ten years film preperation has focused on diamond heteroepitaxy. The aim has been to produce films of homoepitaxial diamond's quality by avoiding the formation of grain boundaries and other defects. The research has focused on finding suitable substrates, conditions for achieving high diamond nucleation densities on various substrates, and the optimization of textured growth procedures. To date many substrates have been investigated, e.g. Ni, Co, Pt, Si, BeO, SiO2, cubic BN, $\beta$-SiC, GaN, etc. [73–77]. However, there is a number of crucial criteria, e.g. long term chemical and physical stability at high temperatures, thermal expasion coefficient comparable to that of diamond, close lattice matching, adhesion, availability of a substrate as large area single crystals, etc., that any material must satisfy in order to be recognized as a candidate for the substrate. These stringent conditions have reduced the number of candidates to a few substrates for deposition of diamond films interesting for applications in electronics. Diamond thin films have been grown epitaxialy on high pressure synthesized cubic BN single crystals [77]. The cubic BN is the most suitable substrate, found up to now, due to its high surface energy, thermal expansion coefficient comparable to that of diamond and close lattice match with diamond, but unfortunately the preparation of single crystals of cubic BN met with the same difficulties as those affecting the growth of diamond single crystals. The growth of diamond on $\beta$-SiC has been studied intensely [75]. Despite the rather large lattice mismatch between $\beta$-SiC and diamond, about 20%, a very high degree of orientation of the diamond polycrystalline films was achieved on (100) oriented $\beta$-SiC. Diamond has been also grown on GaN [76] which implies possibility to integrate the diamond, for example as a heat sink, with GaN electronics.

Most of the CVD diamond films reported to date have been grown on Si, mainly due to the availability of large area single crystal wafers and the low cost of Si as well as the favorable properties of Si [78–84]. Despite the large

lattice parameter mismatch between Si and diamond, about 35%, substantial progresses towards high quality films have been done. Among the techniques developed for preparation of CVD diamond films on oriented Si, two main directions could be discerned—hot filament CVD method and bias enhanced nucleation MPCVD method. The first method is relatively cheap and easy to operate and is used to grow smooth polycrystalline or nanocrystalline randomly oriented films for coatings or to grow diamond crystals of micron size for industrial applications. By the second method heteroepitaxial highly oriented diamond (HOD) films can be deposited on large Si substrates, e.g. 2 in diameter wafers. These films are still polycrystalline but highly oriented with respect to the substrate. The key step of this method is bias enhanced nucleation (BEN), whereby a negative potential (100–200 V) is applied to the substrate in the first stage of the deposition process, in order to create directly diamond nuclei on Si [obs 45–48]. Further improvements of the bias enhanced nucleation with respect to density, uniform distribution and orientation of the nuclei have made the deposition of thick films with a low surface roughness (e.g. less than 100 nm for a film with 15 $\mu$m thickness) containing only low angle grain boundaries, possible. These films having properties approaching those of ideal diamond, as high hardness, high mechanical strenth, high Young's modulus and high thermal conductivity, have found application in many fields, e.g. electrochemical electrodes, field emitter arrays, radiation detectors, micro electromechanical systems (MEMS), etc. In the field of MEMS a large number of devices for various applications has already been built, demonstrating thus the excellent properties of these films [85–87]. Despite their high quality, these films are not suitable for the fabrication of electronic devices since their attractive properties are deteriorated by structural imperfections, particularly by grain boundaries. The performance of electronic devices fabricated using such low quality films is significantly reduced. Furthermore, due to their mosaic spread, these films cannot be used as substrates for the homoepitaxial growth of diamond.

A significant advance in the diamond heteroepitaxy was made by the application of substrates with a multilayer structure. It was discovered that iridium single crystal films grown as a buffer layer on MgO could serve as a substrate for the nucleation and growth of low-pressure microwave plasma-enhanced CVD diamond [88, 89]. Iridium has a high melting point, chemical and physical stability at high temperature in hydrogen environment and a lattice constant only 7% larger than diamond. The epitaxial diamond grains grown on iridium exhibit an up to now unsurpased degree of initial alignment and an extraordinary density. The key step for inducing the formation of diamond nuclei on the iridium films is the BEN method developed in connection with diamond growth on Si. By optimazing the biasing conditions, very high nucleation densities, of the order $10^{12}$ cm$^{-2}$, were reported [93]. The substrate MgO was later replaced by $SrTiO_3$ [90, 91] that decreased the mosaic spread of the epitaxial iridium and of the resulting heteroepitaxial diamond. $SrTiO_3$ has a smaller lattice constant and is readily available. The diamond films were grown by a two stage process. During the first stage, following BEN, thin polycrystalline diamond film grew. The subsequent textured growth transformed the polycrystalline film to a film with a quality comparable with that of natural type II diamond single crystals. The network of grain boundaries dissolved into short segments of defect bands of limited extension indicating thus that the films were not polycrystalline. The diamond layer had single crystal quality and was used for the fabrication of field effect transistors [92]. A further advance in the large-scale heteroepitaxial growth of diamond has been made recently when $SrTiO_3$ was replaced successfully by sapphire [93, 94]. The diamond produced in this way had the same high quality as the one prepared on $SrTiO_3$. However, since sapphire is a relatively inexpensive large area substrate, this development is a further step towards the wafer scale production of heteroepitaxial diamond.

When cooling from the growth temperature the diamond film experiences significant compressive stresses due to the difference in the thermal expansion coefficient of the materials present. These stresses can cause delamination which is a serious obstacle for the development of diamond wafers. Moreover, calculations have shown [95] that films grown on MgO, $SrTiO_3$ and $\alpha$-$Al_2O_3$ substrates are exposed to a significant amount of stress, −8.30, −6.44 and −4.05 GPa, respectively. These large stresses make the treatment of thick films difficult. From the thermal stress point of view, Si with a stress of −0.68 GPa is the most superior substrate so far.

Further step towards the fabrication of large area diamond single crystal films for electronic applications has been made recently [95] by introducing a new concept for the substrate multilayer. The multilayer was prepared in two steps, where yttrium stabilized zirconia (YSZ) was first deposited on Si, then an iridium thin film was deposited on YSZ. This process decreases the lattice misfit between consecutive layers and such a substrate multilayer is shown in Fig. 5. The diamond was then grown on the iridium film as before. The quality of the diamond was the same as of that grown on $SrTiO_3$. The advantage of this concept is in the type and the combination of the substrate materials which minimizes thermal stress thereby avoiding delamination.

An important parameter, concerning the large scale heteroepitaxy of diamond for electronics, is the growth rate of the diamond films. Normally the growth rate is about some $\mu$m/h. Addition of nitrogen induces the increase of the growth rate in CVD process. High growth rates of up to 50 $\mu$m/h have been achieved [167].

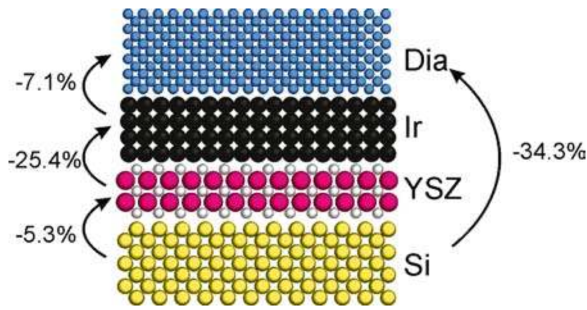


*Figure 5* Schematic representation of the layer system diamond/Ir/YSZ/Si(001). In the YSZ crystal the large spheres correspond to the oxygen ions. The numbers indicate the lattice mismatch between consecutive layers (ref. [95]) (*Figure provided by Matthias Schreck, University of Augsburg*).

In order to exploit diamond's superior properties for the fabrication of electronic devices, thin diamond films are required, i.e. a method for the production of large area, inexpensive single crystal films with low defect and dislocation densities is needed. Diamond device technology has similar problems to third generation semiconductor technology, namely, availability of inexpensive large area diamond crystal with a low defect concentration; this is the prerequisite for a successful application of diamond for the fabrication of electronic devices.

## 3. Electronic devices

### 3.1. Silicon carbide

The ability of silicon carbide to operate at high temperature, high power, and high frequencies enables considerable enhancement of the performance of devices used within a wide variety of applications. In particular, SiC power devices can outperform equivalent Si devices, but this would require a mature and viable SiC semiconductor technology. The fundamental physical limitations of Si operation are the strongest motivation for switching to a wide bandgap semiconductor such as SiC for high temperature applications. The replacement of Si by SiC for power switches [20] is extremely advantageous, since the avalanche breakdown voltage for SiC is about ten times higher than that of Si. Moreover, silicon carbide based power switches also have a faster response with a lower parasitic resistance, so that the physical size of SiC devices shall be much smaller than equivalent silicon devices. In addition, the faster switching speed enhances the efficiency of power system conversion, and allows the use of smaller transformers and capacitors which reduce significantly the overall size and weight of the system. The cooling requirements in power electronics, which are a considerable portion of the total size and cost of power conversion and distribution systems, can be significantly reduced by the high temperature capabilities of SiC.

Power switching devices based on SiC such as Schottky barrier diodes, PiN junction diodes, MOSFETs (Metal Oxide Semiconductor Field Effect Transistor), JFETs (Junction Field Effect Transistor), BJTs (Bipolar Junction Transistor) have already been demonstrated in the research stage. To date, the SiC Schottky barrier diodes used for high voltage applications have evolved from the research stage to limited commercial production [96]. Although Schottky barrier diodes offer rectification with fewer switching losses compared to PiN diodes (when switching from the conducting state to the blocking state) Si based Schottky barrier diodes are still not used for high voltage applications. The reason for this is comparatively smaller barrier height between ordinary metals and Si (typically less than 0.5 eV) which is further reduced in reverse biased mode. The electron injection current from metal to semiconductor increases exponentially as the barrier height reduces. As a result very large reverse currents are observed at relatively low voltages, in the case of Si. The high Schottky barrier height of about 1.5 eV for SiC reduces the leakage

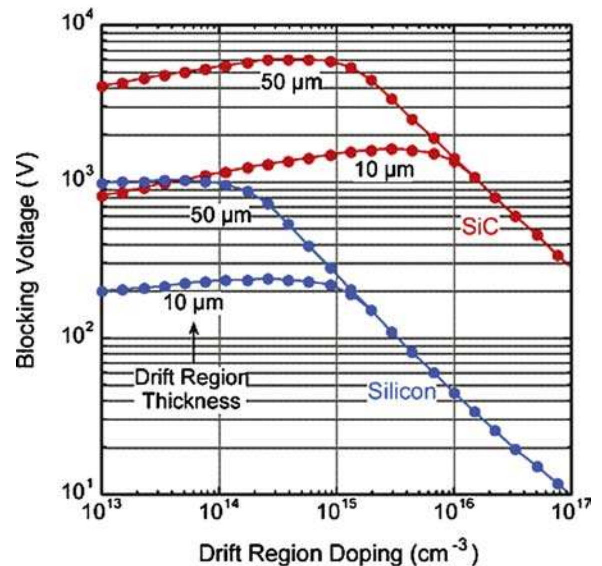


*Figure 6* Comparison of silicon carbide and silicon dielectric strength (ref. [203]).

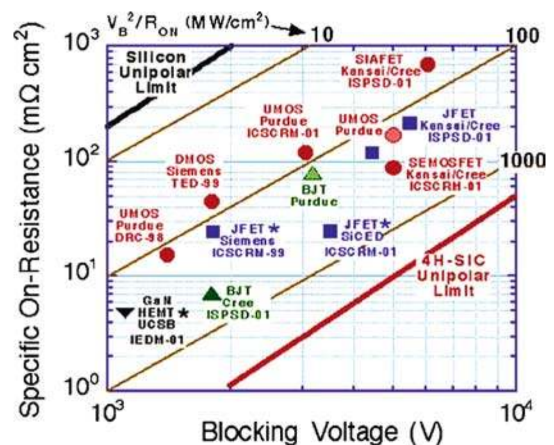


*Figure 7* Comparison of silicon and silicon carbide operating voltage and conduction resistance (ref. [20]).

current such that SiC Schottky diodes can operate at high voltages, and a blocking voltage up to 5 kV has been demonstrated [39].

### 3.1.1. Diodes, Schottky and PiN diodes

In contrast to Si diodes, SiC rectifiers exhibit ultimate low switching losses, no reverse current peak, and therefore an extreme soft recovery behaviour. In Schottky diodes, a reduced forward voltage drop and hence a reduced power loss would be desirable, and this can be achieved by lowering the Schottky barrier height. On the other hand even at high temperatures, the barrier must be high enough to ensure a certain blocking voltage with a reasonably low reverse leakage current. There is a strong dependency of the measured reverse current with the electric field for a Ti/SiC Schottky diode with the temperature as a parameter [97].

Schottky barrier diodes with Ta and TaC on p- and n-type SiC have been investigated by a group at Carnegie Mellon University [98]. The rectifying behavior of both Ta and TaC was observed on p-type 6H-SiC to 250 °C, while on n-type, TaC showed ohmic behavior above 200 °C [98]. The maximum operating temperature of SiC Schottky diodes is restricted because of the increasing leakage current and therefore, junction devices can approach and perform better at higher temperature.

The pn junction-diode characteristics at temperatures up to 400 °C has been reported both for epitaxially grown and ion-implanted SiC. The characteristics of the 6H-SiC pn-diode were obtained where nitrogen was implantated into p-type substrate. The rectifying ratio was measured to be $10^9$ at room temperature and $10^5$ at 400 °C. The PiN diodes of 4H-SiC has been successfully fabricated and this device has a blocking voltage of up to 19 kV [99]. The high temperature operation of a 8 kV diode indicates that the reverse leakage current density at 5 kV increases by only an order of magnitude between room temperature and 300 °C [100]. The reverse recovery of these diodes showed an extremely fast switching which only increased by a factor of two between room temperature and 275 °C. This is small compared to Si diodes which have an increase of four times between room temperature and 120 °C [100]. In the 5.5 kV blocking range of a PiN diode, a forward voltage drop of less than 5V was observed at 500 $Acm^{-2}$ between room temperature and 225 °C, in addition to a 50% increase in the peak reverse recovery current [101]. The reverse leakage current in a large area ($6 \times 6$ $mm^2$) diode which blocked 7.4 kV showed a small increase in the current up to 200 °C after packaging when measured up to 4.5 kV [102].

Another diode the so-called Junction Barrier Schottky (JBS) is also considered an attractive device for power switching applications. The JBS device was first demonstrated in Si [103, 104]. The device structure is a combination of a Schottky barrier and a pn-junction, which allows a reduction in the power loss of the pn-junction under forward conduction and the utilization of the Schottky barrier. In the reverse direction the Schottky region is pinched off by the pn-junction thus exhibiting a smaller leakage current. The spacing between the p+ regions should be designed so that pinch-off is reached before the electric field at the Schottky contact increases to the point where excessive leakage currents occur due to tunnelling, this complicates the device design and several attempts have been reported [105–107]. The major problem concerning SiC may be the poor ohmic contact with p-doped samples which requires a very high temperature annealing (above 850 °C) that causes severe damage to the Schottky contact, this then increases the excessive leakage current compared to an undamaged Schottky contact.

Though all these results on PiN diodes are very encouraging, there still remain problems in its practical operation. The most important perhaps, is the degradation of the current with time when operating at forward bias. One of the most attractive applications of SiC PiN diodes is in HVDC electrical transmission systems. The current degradation is presumed to be related to the generation and extension of stacking fault defects in the basal plane. These defects lie in the crystalline plane perpendicular to the current flow direction. Recently it has been claimed [108] that this problem may be solved by growing the material along another direction. In order to get a defect free crystalline structure, the material was grown on several a-face surfaces at least in 2–3 steps. The PiN diodes fabricated from this material were stressed and measured for 4 hours at constant voltage. The growth using a few steps might be not feasible and more research on the operation of these PiN diodes is needed.

### 3.1.2. High frequency MESFETs, SITs and BJTs

Concerning high frequency devices, several groups from the USA, Japan and Europe have demonstrated two types of SiC transistors, MESFETs (Metal Semiconductor Field Effect Transistor) and SITs (Static Induction Transistors). These transistors suffer from large gate leakages, so that the possible application may be restricted to less than 350 °C. The Static Induction Transistors (SITs) shows the best performance for high peak power applications up to 4 GHz. Under class C operation, the transistor produces over 350 Watts output power with 50% efficiency and a gain greater than 10 dB [109]. At UHF 900 W, pulsed power was obtained from a single chip packaged with a 51 cm gate periphery and at L-band, and the same power was obtained for a 54 cm periphery package [109]. No investigations of the thermal limit of the high temperature operation have been reported for such high power SIT. For MESFETs, power densities as high as 5.2 $W/mm^2$ with

63% power added efficiency (PAE) have been demonstrated at 3.5 GHz while single device with 48 mm of gate periphery yielded 80 Watt CW at 3.1 GHz with 38% PAE [110, 111]. Though these results are impressive, the transistor performance suffers severely from the self-heating due to current flow in the device. Thus the majority of published articles are related to small-gate-periphery since thermal problems are limited and the power densities are recorded to be very high. When the gate periphery increases, the power densities decrease very quickly, this is related to the self-heating effect. For a wide transistor, the temperature becomes very high and, therefore, the electron mobility decreases together with the drain current, and finally the RF power decreases. In a recent investigation, a channel temperature as high as 340 °C was observed for a 31.5-mm large transistor when only DC biases without any RF excitatio and the estimated dissipated power was 58.6 W in class AB [112]. In another investigation, the saturated DC drain current was reduced from 80 mA to 50 mA when the temperature was increased to 250 °C for a 6H-SiC MESFET [113].

Very little has been published so far on bipolar transistors and specially within microwave applications. Due to the wide bandgap, junctions of the transistors can control the reverse and forward current, and hence can be very attractive for high ambient temperature operations. But the transistor suffers from some severe materials properties such as low minority carrier lifetime, a very small hole mobility that restricts the cut-off ($f_T$), and a maximum frequency of oscillation ($f_{max}$). The transistors have been fabricated and exhibited typical emitter breakdown at 500 V while the $f_T$ was only at 1.5 GHz. The transistor with an emitter width of 2.5 $\mu$m and an an emitter periphery of 2.62 cm has demonstrated an output power of 50 Watt using 80 V power supply in common emitter, class AB mode. The pulse width was 100 $\mu$s and the duty cycle was 10% only. The collector efficiency was 51% with a power gain of 9.3 dB [114]. Since SiC junctions can withstand high junction temperatures, the transistor can function efficiently without any external cooling, resulting in significant system advantages.

### 3.1.3. JFETs

SiC based JFETs are very attractive for high-temperature electronics due to the reasons described for the case of BJTs. The JFETs are more attractive as it is a unipolar device and thus does not suffer from the low value of the hole mobility. However, JFETs are normally depletion-mode (normally on) devices, and the gate must be kept at a negative voltage to keep the transistor off. Most power control systems require enhancement-mode (normally-off) transistors so that the system can be switched off in a safe condition. One way to circumvent this problem is to connect a JFET in a cas-code configuration with an enhancement-mode control device such as Si or SiC MOSFET [115]. High temperature operation of SiC based JFETs has been reported in the literature since the early nineties along with the evolution of SiC as a semiconductor for microelectronics.

Transistor with high blocking voltage up to 5.5 kV has been successfully fabricated. This transistor showed a specific on-resistance of 69 m$\Omega$ cm$^2$ and the turn off time was 47 ns [116]. The material 4H-SiC is more attractive due to high carrier mobilities which results in some favourable properties. Specifically, in a vertical JFET with the drain on the backside of the wafer, a forward current density reached up to 249 A/cm$^2$ at a drain voltage of only 1.2 V at room temperature, while at 600 °C the current droped to 61 A/cm$^2$ with an increase of the specific on-resistance from 4.8 to 19.6 m$\Omega$ cm$^2$. In addtion, the breakdown voltage of the transistor was 1644 V at room temperature while it increased to 1928 V at 600 K [117]. In a thermal stress study of a 6H-SiC JFET, about a 40% decrease in the drain current was observed at 300 °C [118].

The high performance of SiC JFET has been reported by Siemens. The buried gate is permanently connected to the source, the device blocked 1800 V at a specific on-resistance of 24 m$\Omega$ cm$^2$. Recently, Kansai Electric and Cree Inc. reported the first enhancement mode SiC JFET [119]. The device structure consisted of two gates; the buried gate was connected to the top gate, providing a gating effect from both sides. The transistor with a 50-$\mu$m thick drift layer blocked 4.4 kV and the specific on-resistance was 121 m$\Omega$ cm$^2$.

### 3.1.4. MOSFETs

In contrast with Si MOSFETs, the 6H-SiC MOSFETs transconductance and channel mobility increases with rising temperature for up to 225 °C. The high interface state density [120] maybe the reason for these trends. MOSFETs fabricated from 6H-SiC have operated at temperatures around 400 °C with a very low drain leakage current in air [121]. In a recent report, a large area device (3.3 × 3.3 mm$^2$) blocked 1.6 kV with an on resistance of 27 m$\Omega$ cm$^2$. This device exhibited a peak channel mobility of 22 cm$^2$/Vs and a threshold voltage of 8.8 V which decreased to 5.5 V at around 200 °C [122].

The transistors were fabricated both in the lateral DMOSFET (Double Diffused MOSFET) and the vertical UMOSFET (U-shaped trench MOSFET) directions, these blocked several kilo volts. The Northrop Grumman group determined that both transistor types have similar channel mobilities and the same temperature effect due to the interface traps. In addition, they operated up to 300 °C where the current and transconductance increased with rising temperature [123]. A group at Purdue University demonstrated a novel DMOSFET which could block 2.6 kV, where the drain current at

155 °C was four time the value at room temperature [124]. Recently, Purdue and Auburn University fabricated a UMOSFET which could block more than 5 kV, with a specific on-resistance of only 105 mΩ $cm^2$, for a 100-$\mu$m thick low doped drift layer. This device has not been characterized at elevated temperatures [125]. The transistor maintained a low on-resistance to current densities above 100 A/$cm^2$, while the maximum reported current density has been 40 A/$cm^2$. Cree Research has already reported a record blocking of more than 6 kV.

Due to the problems caused by a high interface state density which results in a very low channel mobility, a new type of transistor the ACCUFET (Accumulation-mode MOSFET) with output characteristics that are similar to MOSFETs has been introduced and fabricated in both 6H- and 4H-SiC [126]. The 4H-SiC transistor exhibited a high specific on-resistance, 3.2 Ω$cm^2$ at a gate bias of 5V which reduced to 128 mΩ $cm^2$ at 450 K. The transistors were not designed for high blocking voltages thus the un-terminated breakdown voltage was only 450 V.

Recently, encouraging results from the continuing research 4H-SiC MOSFET has been reported [127, 128]. Growing the gate oxide in $N_2O$ ambient results in a significant enhancement of the inversion channel mobility in lateral n-channel Si face 4H-SiC MOSFETs. A mobility of 150 $cm^2$/Vs was obtained, whereas a value below 10 $cm^2$/Vs was obtained when growing the gate by the conventional process: in a wet or dry oxygen ambient.

#### *3.1.5. Thyristors, GTOs and IGBTs*

One of the most significant developments in device technology during the last 15–20 years is the IGBT (Insulated Gate Bipolar Transistor) that blocks high voltages but at the same time has a high conduction current. The basic advantage of the IGBTs is conductivity modulation due to carrier injection and a MOS-driven gate. The device operates between 600 and 6.5 kV where the current varies over 1–3500 A. The device has a big potential for further development in the areas of higher currents and voltages, and for higher frequencies and lower dissipated power.

A large amount of effort is being made on the development of SiC thyristors and IGBTs. The main advantage is the high electric breakdown field strength, which leads to very thin drift layers, and consequently much faster switching behaviour.

The thyristor is the most popular controllable device used in high power systems with controllable turn-on, and large area Si thyristors are produced today as a single device on a wafer with a 4-inch diameter. The current capability is more than 1000 A with a blocking voltage approaching 10000 V. These devices are used in HVDC (High Voltage DC) transmission systems, and so far no other device can match its performance. A 6H-SiC poly-type thyristor was first demonstrated in early 1993. Due to the high resistivity of the p-type substrate, a high specific on-resistance of 128 mΩ $cm^2$ has been obtained for a 100 forward blocking voltage device [129]. However, at a higher temperature of 633 K, the thyristor performance improved with a specific on-resistance reduced to only 11 mΩ $cm^2$. The opposite polarity thyristor has been realised on the same structure with an improvement in all the characteristic parameters, and a very low specific on-resistance of about 3.6 mΩ $cm^2$ that increased to 10 mΩ $cm^2$ at 623 K temperature. Furthermore, early 4H devices exhibited a blocking voltage of –375 V. The low on resistance of the 4H devices resulted in a lower voltage drop. Subsequently, the Northrop Gramman group has demonstrated a GTO (Gate Turn-Off) with 1 kV blocking, but the device was turned-off by an external MOSFET. The device has been operated successfully at 390 °C [130]. Recently a remarkable effort has been put into this area and a 4H-SiC based GTOs has been demonstrated with a 3.1 kV forward blocking capability with a 12 A conduction current [131].

### 3.2. Diamond

The many exceptional properties of diamond make it a very attractive material in several fields of electronics, optoelectronics and electromechanical micro devices. Since an exhaustive review on the application of diamond in electronics and optoelectronics would be beyond the scope of this relatively short review, here the survey is limited to the application of diamond for pn-junctions, BJTs, FETs, passive components, heat spreading elements, field emission, and resistors. For the application of diamond in other areas, e.g. sensors and detectors [132–137], microwave filters [138], acoustic wave filters [69, 139] and electro-mechanical micro devices [86, 140], the interested reader is directed to the above references.

#### *3.2.1. PN-junction*

In order to exploit the superior properties of diamond for high-power/high temperature electronic devices, high quality, inexpensive diamond must be available. The preparation of heteroepitaxial diamond is viable by bias-enhanced nucleation of iridium single crystal film on sapphire or $SrTiO_3$ followed by low-pressure plasma enhanced chemical vapor deposition. The crucial factor in the fabrication of electronic devices is the ability to prepare pn-junction, i.e. the ability to prepare in a reliable way p- and n-type materials with high carrier densities.

The p-type diamond has up to now been created by doping with boron. The boron is introduced from a gas or a solid [141–145] during diamond growth. The activation energy of electrical resistivity decreases with increasing boron concentration, being in the range 0–

0.43 eV [141]. The energy is 0.35 eV for boron concentration of $1 \cdot 10^{18}$ cm$^{-3}$ and it becomes zero for boron concentrations greater than $1.7 \cdot 10^{20}$ cm$^{-3}$ [141]. The p-type diamond can also be created by exposing the material to hydrogen plasma. The hydrogenation creates a layer with p-type conductivity with a fairly low resistivity $\sim 10^6$ Ωcm [146]. The discovery that both single crystal and polycrystalline diamond can be treated by the plasma has led to a successful use of these materials for the fabrication of electronic devices, e.g. fabrication of FETs.

The growth of n-type diamond is one of the most challenging issues in the diamond field. Many theoretical predictions as well as experimental attempts to obtain n-type diamond have recently been published. Unfortunately, all experimental attempts have up to now delivered n-type diamond with low electron densities, this restricts the use of n-type diamond for the fabrication of transistor. Nitrogen is often used to create n-type diamond, but nitrogen doped diamond is an electrical insulator at room temperature due to the deep level of 1.7 eV of the nitrogen impurity. Nitrogen is thus not a practical dopant atom to use. Phosphorus would be an obvious candidate but it has an impurity level of $\sim$0.59 eV which is still rather high. Several reports on phosphorus doping have been published reporting activation energy in the range 0.32–0.59 eV [141, 147–149]. Reproducible results on phosphorus doping have been reported recently [147, 148]. At room temperature a reasonably high electron mobility of 250 cm$^2$/V was measured in the P-doped films [147]. Attempts to use other elements for n-type doping has also been made, e.g. sulphur (0.32 eV [141, 149, 151]), lithium (0.16 eV [141, 150]). A survey of p-type doping of diamond has been given by Kalish [152].

In spite of the experimental difficulties in n-type doping several research groups have succeeded to create a well functional pn-junction. Koizumi *et al.* [147] created a pn-junction by epitaxial growth using a MPCVD technique to fabricate a phosphorus doped n-type diamond film on a boron doped p-type diamond film, on the [111] oriented surface of a diamond single crystal. The substrate contained over 100 ppm boron and exhibited high electrical conductivity. The electrical and optical properties of the junction have been investigated. The pn-junction exhibited clear diode characteristics, where the rectification ratio was over five orders in magnitude and the turn-on voltage was 4–5 V. The temperature dependence of the hole and electron concentrations in doped diamond films has been studied up to 1000 K. At room temperature the carrier mobilities of the boron and the phosphorus doped film were 300 and 60 cm$^2$/Vs respectively, and UV light emission has been observed at 235 nm.

A pn-junction has also been formed by using boron doped p-type and nitrogen doped n-type diamond films [153]. The active diamond films were grown by a MPCVD technique on heavily boron doped HTHP diamond single crystals. The forward and reverse I-V characteristics of the junction were studied as a function of temperature up to 400 °C. At room temperature the resistivity of the n-layer is extremely high, $\sim$10 GΩcm. The activation energy of the pn-junction diode saturation current obtained from these measurements was 3.8 eV. This value is in good agreement with theoretical predictions that assumes that the energy of the nitrogen level 1.7 eV. A pn-diod was also formed from thick litium doped layer grown on highly boron doped substrate [141]. At room temperature the rectification ratio was $\sim 10 \cdot {}^{10}$ for $\pm$10 V, but the serie resistance was very high $\sim$200 kΩ, whereas at higher temperatures the series resistance decreased to 30 kΩ but the rectification ration decreased to $\sim 10^6$.

A single crystal diamond pnp type BJT consisting of boron/nitrogen pn-junctions has been fabricated [145, 153]. The transistor characteristics for common-base and common-emitter configurations have been measured. The temperature activated leakage current limited the operation of the transistor up to 200 °C. The study showed that it was possible to fabricate a pnp type BJT, but the high resistance of the base $\sim$10 GΩm at 20 °C, limited the operation of the BJT:s to the dc mode, small currents (nA), and moderate temperatures. Diodes as electronic devices must have a high reverse voltage and a low resistance in forward direction. It has been shown that lightly boron doped ($\leq 10^{17}$ cm$^{-3}$) Schottky diodes on oxygen terminated surfaces exhibit good performance at high temperatures. Stable contacts at high temperatures have been developed to create diodes that may operate up to 1000 °C [154–156]. The diodes showed breakdown behaviour at reverse bias, but the reverse current was higher than theoretical values. The breakdown electric field for CVD diamond has been estimated to be 2.106 V cm$^{-1}$ [141], a value well below that of natural diamond.

### 3.2.2. FETs

While the development of the diamond bipolar junction transistor is hindered by the lack of n-type diamond with high electron densities, there has been some promising results towards the development of diamond field effect transistors, though studies at high temperatures are absent. Nevertheless, a short review of the present situation regarding diamond FETs is given here. There are presently two concepts for obtaining high performance devices: boron $\delta$-doped p-channel FET and hydrogen induced p-type surface channel FET. Since a shallow diamond dopant is absent, $\delta$-doping and 2D-conduction are essential parts of the diamond device concept.

Hydrogenated surfaces of natural diamond and films grown by plasma assisted chemical vapor deposition technique exhibit substantial conductivity. Hydrogenation is carried out by treating the diamond surface

with hydrogen plasma and cooling to room temperature in hydrogen ambient. The hydrogen terminated surfaces exhibits the following, a p-type conductivity (2D-conduction) of the order of $10^{-4}$–$10^{-5}$ $\Omega^{-1}$, a shallow acceptor level less which is less than 50 meV, a high carrier concentration $10^{13}$ cm$^{-2}$, and a hole mobility in the range 100–150 cm$^2$/Vs [146, 157–161]. The thickness of the conductive layer is estimated to be less than 10 nm. It has been suggested that the surface conductivity depends on the details of the hydrogen termination together with the coverage of physisorbed adsorbates [162–164]. The high conductivity of the layer can be destroyed by dehydrogenation of the surface, by exposing the surface to oxygen or by heating in air at a temperature above 200 °C [146, 165]. The latter consideration may complicate the fabrication of devices. In order to exploit the conducting layer for the fabrication of high temperature diamond devices, a way of protecting the layer has to be developed [165]. The opposite of hydrogenation is obtained by treating the diamond surface with oxygen plasma. The oxygen terminated surface becomes highly insulating due to the surface potential pinning at ~1.7 eV above the valence band [166]. This effect is exploited to isolate parts of a device when fabricating devices by the planar process. The hydrogen terminated areas are transformed into oxygen terminated ones. The hydrogen terminated surface has a low surface state density thus the barrier height between a metal and the surface is almost determined by the work function of the metal only. Usually Al and Au are used as ohmic contacts. Furthermore, when hydrogenation is used to create surface p-type conductivity, alternative cheaper types of diamond can be used [167].

The high hole conductivity allows for the fabrication of high performance FETs, e.g. [158, 168–172]. Two types of FETs have been investigated, the MISFET (Metal Insulater Semiconductor Field Effect Transistor) and the MESFET (Metal Semiconductor Field Effect Transistor). The high frequency performance and DC output characteristics of a MISFET with 0.7 $\mu$m gate length has been investigated at room temperature [172]. The measurements show that the cutoff frequency $f_T$ and the maximum frequency (MAG—maximum available gain) $f_{MAX}$ are 11 and 18 GHz respectively. In addition, a transconductance, $g_m$, of 100 mS/mm, has been obtained from dc measurements. The DC output characteristics of a circular FET with a gate length 3 $\mu$m has been investigated at room temperature [173]. The maximum current was 90 mA/mm at a gate bias −6 V, and the maximum transconductance was 25 mS/mm. Breakdown voltage at pinch-off was −200 V. The high frequency performance of MESFETs has also been also investigated at room temperature [174]. The cutoff frequency and the maximum frequency for a transistor with 2 $\mu$m gate length were 2.2 and 7.0 GHz, respectively. The highest frequencies at room temperature were obtained for a MESFET with a gate length 0.2 $\mu$m [170,

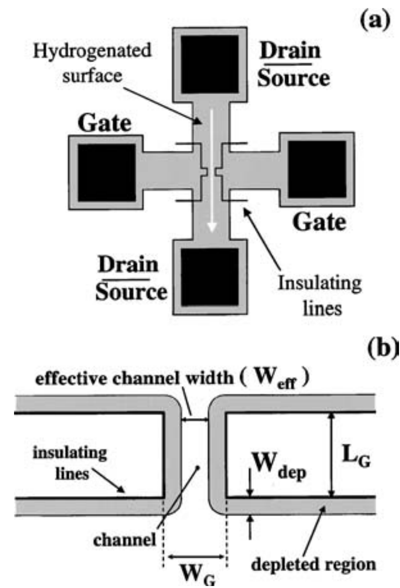


*Figure 8* (a) Schema of an in-plane transistor fabricated on a H-terminated diamond surface, using oxidized lines to define channel and gate, (b) channel region with oxidized lines and depletion regions along the lines. $L_G$ and $W_G$ are gate length and gate width, respectively (ref. [171]) (*Figure provided by J.A. Garrido, Munich University of Technology*).

175, 176], and the following values were reported: maximum drain current, $I_{\mathrm{Dmax}}$, 360 mA/mm, the transconductance, $g_m$, 150 mS/mm, the maximum drain voltage, $V_{\mathrm{DSmax}}$, 68 V, and the maximum estimated power capability, $P_{\mathrm{Rfmax}}$, 3.0 W/mm for class A. The cutoff and maximum frequencies were measured to be 11.7 GHz and 31.7 GHz respectively [175]. In a later investigation even higher frequencies were obtained, 21 GHz and 63 GHz, respectively [176]. These results indicate that a high gain can be obtained and that this transistor can operate at RF frequencies. Unfortunately, the instabilities of the hydrogen terminated surface prevented large signal measurements on the device. The structure of a FET fabricated using the hydrogen layer is shown in Fig. 8.

The hole concentration of homoepitaxially prepared diamond films was measured for temperatures up to 500 °C. By altering the manner in which the temperature is increased and decreased, it has been shown that adsorbates from the environment can change the hole concentration in the conducting layer. Furthermore, the influence of the crystalline and surface properties of diamond homoepitaxial layers on device properties of hydrogen terminated surface-channel FETs has been investigated [177].

The $\delta$-channel FET approach is based on boron $\delta$-doping, where the doping profile with peak concentration of $10^{20}$ cm$^{-3}$ must be confined to within a few nanometers [178, 179]. The DC output characteristics of $\delta$-doped MESFETs were investigated at room temperature and at 350 °C [180]. The maximum drain current $I_{\mathrm{Dmax}}$ at room temperature and 350 °C were 35 $\mu$A/mm

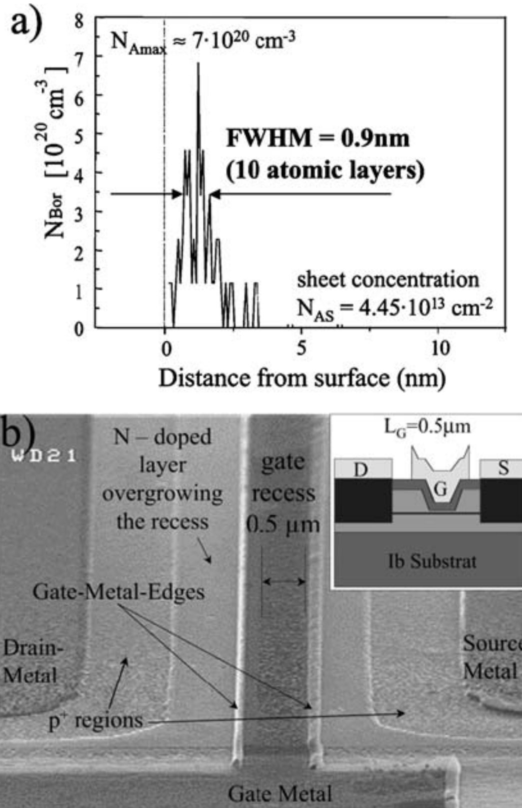


*Figure 9* (a) ERD-analysis of a $\delta$-doped layer showing a FWHM of 0.9 nm (10 atomic layers); (b) fabricated recessed gate $\delta$-channel-JFET with roughness visible at the bottom of the epitaxially overgrown recess trench. The gate length of 0.5 $\mu$m is given by the width of the gate recess (ref. [170]).

and 5 mA/mm, respectively. The maximum usable drain source voltage $V_{DSmax}$ at room temperature and 350 °C were 100 V and 70 V, respectively. A $\delta$-channel JFET, with a $\delta$-doping profile width of 1 nm, has been fabricated and the DC output performance has been investigated at a temperature of 250 °C and −125 °C [170]. The mobility of such $\delta$-doped channels would be ~350 cm$^2$/Vs. At temperature 250 °C all the carriers are activated and a maximum drain current $I_{Dmax}$ of 120 mA/mm has been measured for a transistor with a gate length of 2 $\mu$m and a gate width of 100 $\mu$m. Fig. 9 shows $\delta$-doping profile and fabricated recessed gate $\delta$-channel-JFET.

All FETs were fabricated from homoepitaxial films deposited on HTHP diamond single crystal substrates, since the use of polycrystalline diamond films significantly reduced the FETs' performance. In addition, encouraging results which can be regarded as an important breakthrough in the development of high power diamond electronics on the wafer scale, have been reported recently. The fabrication of high performance p-type surface channel MESFETs with sub-micron gate length from a heteroepitaxially grown diamond film. The diamond film was grown on $SrTiO_3$ ceramic substrate with an intermediate iridium buffer layer [92]. The

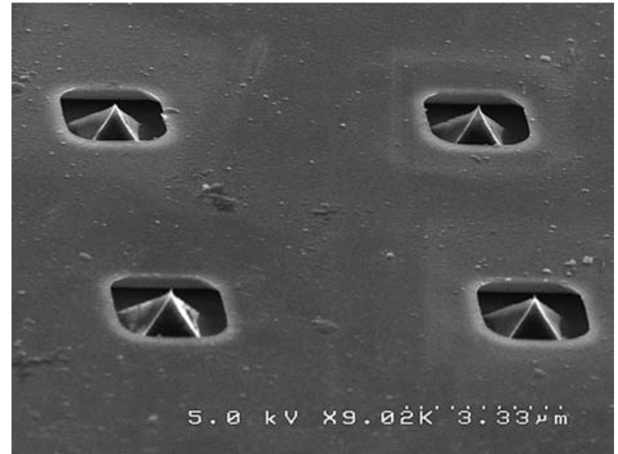


*Figure 10* SEM picture of a 2 × 2 array of gated diamond emitter (ref. [182]).

components exhibited similar performance as structures fabricated from homoepitaxial diamond films. The devices have been analysed at room temperature under DC, small signal and large signal RF power conditions. For devices with the smallest gate length 0.24 $\mu$m the following values were obtained, $I_{Dmax}$ ~250 mA/mm, transconductance ~97 mS/mm and $V_{Dmax}$–90 V. The cut-off $f_T$ and maximum frequencies $f_{max(MAG)}$ were measured to be 9.6 and 16.3 GHz, respectively.

In connection with the solid state diamond FETs, the diamond vacuum field effect transistor (VFET) ought to be mentioned. This component is part of vacuum electronics using diamond electrodes [181]. The diamond field emitter has been integrated with silicon based microelectromechanical system processing technology in order to obtain a monolithic diamond field emitter triode on Si wafer [182]. The monolithic VFET with a self aligned n++ gate has been operated in a vacuum in triode configuration, with an external anode placed 50 $\mu$m above the gate. The low turn-on gate voltage of 10 V, the high anode emission current of 4 $\mu$A at an applied gate voltage of 20 V, and the high gain factor of 250, indicate that high speed diamond VFETs for low and high power can be realized.

### 3.2.3. *Passive components*

The highly oriented heteroepitaxial diamond films grown on wafer size Si, HOD films, are polycrystalline and cannot therefore be used for the fabrication of transistors or as substrates for the homoepitaxial growth of diamond. Nevertheless, these films possess properties that approach the properties of ideal diamond, and may be the most suitable material for MEMS technologies, heavy duty, high frequency and high temperature electronic components for integrated high power microwave circuits, and passive components like e.g. capacitors, switches, and planar waveguides. This should also enable the integration with Si- and 3C-SiC-electronics.

In connection with high temperature devices two passive components can be mentioned here, capacitors [183] and switches [184]. The capacitor has been realized using a diamond membrane as the dielectric and Au as the contacts. The diamond films were grown on large area Si substrate by MPCVD technique. The dielectric loss of the capacitor has been measured up to 600 °C and the C–V characteristics for up to 500°C. The capacitor functioned up to 450 °C with low loss and constant capacitance, whereas for higher temperatures the capacitance was temperature dependent. The micro-switch has been fabricated using the same type of diamond. The properties of diamond make it an ideal material for switch fabrication. Switches often operate in a vacuum at temperatures around 650 °C in a kHz frequency range. Moreover no change in the switching threshold voltage indicates that there has been no change in the device's mechanical properties.

### 3.2.4. Heat spreading elements

The properties of diamond suggest that its main application will be in power electronics at high frequencies and high temperature. Natural diamond has the highest known thermal conductivity, 2200 W/mK at room temperature. The highest quality synthetic diamond grown by CVD technique has an identical thermal conductivity. This implies that power devices can be built on an integrated heat spreader. The high thermal conductivity and thermal stability of diamond will allow ideal heat sinks to be combined with high power microelectronic and optoelectronic devices operating at high temperatures. Although the thermal conductivity of CVD diamond reduces with decreasing layer thickness, it still it exceeds the conductivity of gold, even when the thickness is as low as 2 $\mu$m [185, 186]

The GaN based FETs have owing to their excellent characteristics, a great potential for high frequency power amplifiers [21]. A limitation of the GaN FETs performance is the rise in operating temperature caused by heat dissipation leading to large leakage currents and reduced channel mobility [187, 188]. It has been demonstrated that a heat spreading diamond film can be deposited on GaN FETs, without any degradation of the transistors characteristics [186]. The films of thickness 0.7 and 2 $\mu$m were deposited by CVD technique using a new seeding process at low temperatures (less than 500 °C). The GaN FETs were fabricated by a standard process for GaN transistors.

A correlation between the integrated absorption in IR range from 2700 up to 3030 cm$^{-1}$, associated with stretch modes of $CH_4$, and the measured thermal conductivity at 300 K were reported for CVD diamond samples of different optical quality [189]. This provides a quick and reliable method of ascertaining a film's thermal quality. The measured integrated absorption as a function of the thermal conductivity is shown in Fig. 11.

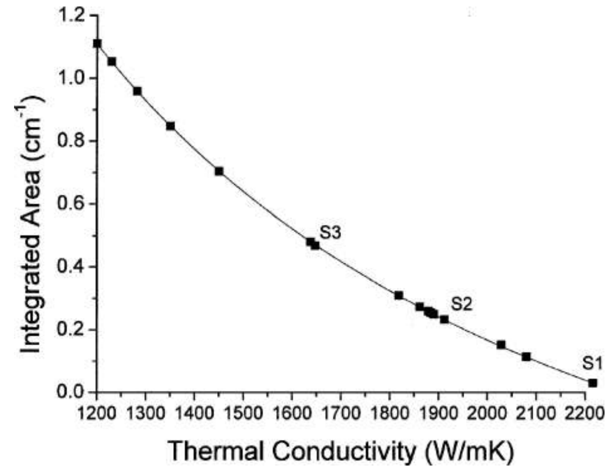


*Figure 11* The measured integrated absorption between 2760 and 3030 cm$^{-1}$ plotted against the thermal conductivity determined using the laser flash technique. Samples S1-S3 are marked, the other data points are measured from a range of material with as-grown thickness varying from 100 to 800 $\mu$m (ref. [189]) (*Figure supplied courtesy of Element Six Ltd.*).

### 3.2.5. Field emission

The emission of electrons from an electrically active surface by means of tunneling into vacuum is commonly referred to as field emission. The emission properties of diamond, diamond-like carbon (DLC) and carbon based materials are very robust [181]. Thin diamond film deposited by CVD technique is an excellent cold electron emitter. The electron density yield is around 1 mA/cm$^2$ for an applied field of 10–100 V/$\mu$m. There is much scientific and technological interest in electron field emission from carbon based materials for applications in many fields, e.g. vacuum field effect transistors, diodes and triodes, ion sources, electron guns, flat panel displays, scanning microscopes, energy conversion, and many others. A very large number of reports concerning the field emission from carbon based materials has been published since the first reported electron emission from diamond in 1991 [190]. The physical reason behind the outstanding emission properties of these materials however is still under discussion [191].

Depending on the surface termination, diamond can exhibit a low or even negative electron affinity (NEA) [161]. The surfaces of diamond and DLC (Diamond like Carbon) prepared by the CVD technique are naturally terminated by physisorbed hydrogen, making diamond the only semiconductor for which a true negative electron affinity can be obtained. It means, the vacuum level can be below the conduction band minimum at the surface barrier [161]. The hydrogen layer lowers the electron affinity and reduces the turn-on voltage required to achieve field emission. Many reports treating different aspects of the field emission process has been published to date, e.g. [192–194]. However, there are several problems connected with a direct application of diamond, DLC or other forms of carbon emitters, for instance non-uniform emitter microstructures resulting

in inconsistent emission and poor long term stability. In diamond there are no free electrons to be easily emitted. A three step emission model was proposed by Cutler *et al.* [195]. According to this model the electrons are injected through the back contact, transported through the diamond, and emitted at the diamond—vacuum surface. This model was extended by a proposition [196] that (i) electrons are transferred by the applied electric field from the substrate to the nitrogenated DLC conduction band through a band to band tunneling process, (ii) electrons are transported across the nitrogenated DLC film through its conduction band, and (iii) electrons emit into the vacuum at the surface of nitrogenated DLC film by tunneling through the barrier. The barrier was crated by the strong upward band-bending at the surface.

Hydrogen has been the most commonly used element for inducing NEA on diamond surfaces. It has been reported that other materials e.g. a Ti layer, can also induce NEA on diamond surfaces [197]. High temperature thermionic electron emission has been studied for several decades [198]. Fowler-Nordheim theory, the theoretical foundation of field emission, neglects the effects of temperature on emission characteristics. The temperature dependence of field emission from diamond film surfaces has been reported recently. The electron emission properties of nitrogen doped diamond films were studied as a function of temperature for up to 950 °C [199]. The films were prepared by microwave assisted CVD technique for application as a low temperature thermionic field emission cathode. The film surfaces were terminated with hydrogen or titanium. Measurements at elevated temperatures showed the importance of a stable surface passivation. Hydrogen passivated films showed enhanced electron emission, but measurements at elevated temperatures, e.g. 725 °C, showed that the hydrogen layer had degraded rapidly. The titanium terminated films showed a similar enhanced emission as the hydrogen terminated ones but the titanium passivated surfaces were stable up to 950 °C. The electron emission increased with increasing temperature, implying that the field emission is strongly temperature dependent. At temperatures below 500 °C no emission was detected, while increasing the temperature above 700 °C a strong contribution to the electron emission was detected. At constant temperature the emission current was nearly constant at low anode voltages, whereas it increased exponentially for anode voltages above 15 kV. At low anode voltages, below 10 kV, the activation energy was approximately 1 eV. This energy value indicates contributions from nitrogen donor levels and defect states to the emission current. It was suggested, according to the emission characteristics, that the emission at low anode voltages could be attributed to thermionic emission of electrons in the diamond's conduction band, whereas the exponential increase at higher voltages indicated a tunneling through or thermionic emission over the potential barrier.

The temperature dependence of electron field emission characteristics of nitrogen doped polycrystalline diamond films has also been investigated by [200]. The films were grown by PECVD technique for high temperature applications. The measurements show that maximum current density increased and the turn-on voltage decreased for temperatures between 300 and 500 °C. The experimental results were interpreted in terms of the Fowler-Nordheim theory and by means of an alternative model that included size and temperature effects explicitly. Furthermore, analysis of the temperature dependence of emission was carried through by parameter estimation of the effective emitting area, field enhancement factor, and work function. All of the estimates indicated that the emission characteristics exhibit a strong dependence on temperature. From these results it was suggested that the thermally excited electrons are responsible for improved emission at high temperature.

### *3.2.6. Resistors*

An attractive feature of diamond films is their ability to be an excellent dielectric when undoped, or as an interesting resistors when doped. Even polycrystalline or nanocrystalline diamond films, depending on the process deposition conditions, exhibit breakdown strength (as a dielectric) and power density capability (as a resistor) with values particularly interesting for high temperature and high power applications. Diamond resistors were fabricated on a ceramic substrate of aluminum nitride [201], by etching in oxygen plasma from the CVD deposited layer of boron doped diamond films. The resistors were intended for investigation of high power density characteristics of boron doped diamond. The resistor exhibits ohmic behavior at low to medium current levels, e.g. up to ~3 mA. At higher currents, thermal excitations are important, and the carrier density enhancement and conductivity increases. The component enters a thermal runaway situation, but unlike conventional devices, the resistor by virtue of diamonds tolerance for high power, continues to operate at very high power and temperature conditions. Operating the resistor under load at high voltages is not unlike operating certain devices in the reverse breakdown mode, except for the much higher power density levels. For example, the resistance at low power is typically 315 kΩ. The power density just before entering the thermal runaway region is 480 kW/cm$^2$. At a maximum current 14.2 mA and voltage 413.2 V the resistance fell to 29 kΩ. At the end of the test the power was 5.87 W and the current density was 4730 A/cm$^2$ [201].

Technological applications of micro electromechanical systems (MEMs) and optoelectronic system can be broadened by the existence of thermally stable thin film resistive microheaters. Thermally stable resistors working in a wide temperature range were presented recently [202]. Amorphous carbon material metal

containing films, CrSiDLC and MoSiDLC, were prepared by the CVD technique and doping with Mo and Cr. The resistors, in the form of strips, were deposited on glass ceramic substrates. The films were studied at 700–800 °C. The average resistivity was $2 \cdot 10^{-3}$ Ω. The thermal coefficient of resistance was $1 \cdot 7\ 10^{-4}$ Ω/K and the activation energy was 30 meV.

## 4. Summary

This paper reviewed the advances in research and technology of the wide bandgap semiconducting material SiC and diamond for high temperature electronics. The hexagonal 4H-SiC structure is the most appealing for high temperature power electronics. Basic SiC devices for use in power electronics that can opera te at elevated temperature were presented. Four major device concepts: Schottky and pn-diode, high frequency devices, power switching devices and high current devices were discussed. PiN high blocking voltage power diodes can operate above 300 °C with an order of magnitude increase in the reverse leakage current density. JFET is supposed to be the most promising power device. The transistors with blocking voltage up to 5 kV were characterized up to 300 °C. MOSFETs are still under development, and their operation has been tested up to 400 °C. The operation of high frequency transistors are limited by to Schottky barrier height and possible applications may be limited to below 350 °C. The most probable near future devices are thyristors and GTOs since their junctions can withstand higher temperatures, and exhibit large blocking voltages and high conduction currents.

Concerning high temperature/high power electronics, diamond has the most superior properties and it is at different stage of research than SiC, since the technology of diamond electronic devices is in its infancy. The foremost progress in diamond research has been in the preparation of high quality heteroepitaxial diamond, which is the prerequisite for wafer scale fabrication.

The state of the art concerning high temperature devices are pn-diodes and Schottky diodes that operate up to 400 °C and 1000 °C, respectively, and passive component capacitors and switches that operate up to 450 and 650 °C, respectively. Moreover, the development of FETs have reached important milestones for both dc and rf modes. The performances of these components however, are still below standard, and components that can operate at high temperatures and high powers are still far away. The development of the BJT is hindered by the unavailability of n-type diamond with high electron concentrations. The application of diamond for field emission has made a lot of progress, since vacuum FET has been fabricated and field emission from diamond has been studied at high temperatures. Diamond as a heat sink for high power electronic devices can soon find wide applications due to the recent progress in the preparation of large area high quality diamond films. The carbon based resistors exhibit excellent thermal stability, and with the continuing progress in the preparation of carbon based materials will find increasing application in the fabrication of high temperature devices.

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