Silicon carbide coated silicon nanowires as robust electrode material for aqueous micro-supercapacitor

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The development of passivated silicon nanowire (SiNW) based micro-supercapacitor electrodes for on-chip applications using an environmentally benign aqueous electrolyte is reported. The SiNWs, produced by low-temperature (50 °C) electrochemical etching, corrode during charge/discharge cycling in the aqueous environment, but upon coating with a silicon carbide passivation layer, the corrosion is mitigated. The as-formed materials are in electrical contact with the substrate, requiring no additional current collector. The passivated NWs achieve capacitance values up to ~1.7 mF/cm^2 projected area (comparable to state-of-the art carbon based micro-supercapacitor electrodes), exhibit robust cycling stability, and maintain capacitive behavior over a wide range of charge/discharge rates. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4704187]

Micro and nanoelectromechanical systems (M/NEMS) based remote sensors play an ever increasing role in human society including monitoring the structural health of major civil works, the physical health of human patients, and the environmental presence of toxic or explosive compounds.[1–3] Integration of high power, robust, micro scale energy storage devices with these sensors is important in terms of device reliability, providing burst energy for data relay, and allowing for the continuing densification of components by reducing bulky external power sources. Micro-batteries based on 3-d architectures have been proposed for application in high-power devices and boast scalable energy capacity. However, these devices have not yet been demonstrated to overcome typical battery failure modes resulting from material degradation during cycling.[4] Micro-supercapacitors are attractive candidates to fill this important energy market due to their high specific power capacity and robust cycling stability (~10^6 cycles vs ~10^3 cycles for batteries).[5]

Current supercapacitor technologies based on high surface area carbons are commercially available in prepackaged form and are widely used for macro-scale devices.[6] Scaling down these technologies for integration on the micro-scale is not trivial and issues with electrical contact to the substrate and precision placement of the materials must be overcome. Various solutions to these issues have been demonstrated in the literature including the use of carbon nanotube arrays or carbide-derived carbons,[7,8] which may be directly grown on current collectors, and inkjet or electrophoretic controlled deposition of materials onto prefabricated current collectors.[9–11] Capacitance values of up to 4.2 mF/cm^2 projected area have been achieved with these electrodes.[11] However, the above solutions require one or multiple undesirable fabrication steps including high temperature processing (>1000 °C), harsh chemical treatments, complex patterning, or intricate material deposition procedures. All silicon-based materials produced with low temperature methods using chemistries compatible with basic microfabrication techniques are promising in simplifying all aspects of processing and integration, making them an even more attractive electrode material.

Previously silicon nanowires (SiNWs) produced via the well-established vapor-liquid-solid (VLS) mechanism were demonstrated as supercapacitor electrode materials operating in ionic liquids.[12] In this work, we present on the performance of SiNWs fabricated with a spontaneously self-assembling, low-temperature, one-step electroless metal assisted etch technique.[13] This process avoids the metal catalyst pre-seeding step and high temperature chemical vapor deposition growth conditions required for VLS-type nanowires as well as the complexities associated with doping of bottom-up NWs. The SiNW arrays used in this work, see Figure 1(a), are produced via wet etching of p-type (1–5 mΩ · cm) Si (100) substrates using an oxidant/etchant bath of 20 mM $AgNO_3$ and 5 M HF, respectively, at the bath temperature of 50 °C. Residual silver is removed by a dilute HNO_3 etch and the wires are then dried by critical point drying (Tousimis Autosamdri815B). These conditions result in nanowires with a diameter range of ~20–300 nm and an average of approximately 100 nm, as reported elsewhere.[14] It has also been shown that this SiNW synthesis technique is compatible with standard lithography and patterning technologies.[15] The electrode materials' performance is characterized by cyclic voltammetry (CHI 660D electrochemical station) in 1 M KCl utilizing a three electrode cell consisting of an Ag/AgCl reference electrode, Pt wire counter electrode, and the NW array as the working electrode. Electrical connection was made directly to the substrate by Ag paste deposited on an unetched region, which was protected during the etching step by a polymer resist. The capacitance, C, was calculated using[16]

$$C = \frac{I}{dV/dt} \quad (1)$$

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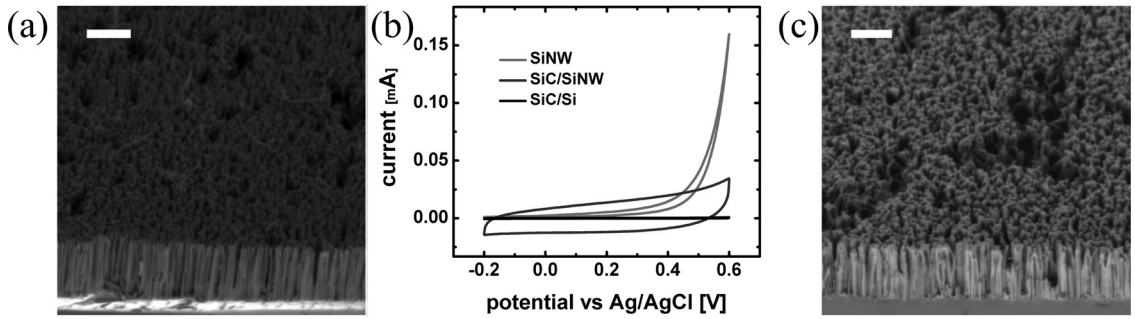

FIG. 1. (a) Cross sectional SEM micrograph (NovelX mySEM) of wet-etched silicon nanowires. (b) Results of CV testing (1 M KCl at a 50 mV/s scan rate) for SiNW array, SiC coated SiNW array and SiC coated planar Si for comparison. (c) Cross sectional SEM micrograph of SiC coated SiNW from (a). Scale bar is 10 μm in both (a) and (c).

utilizing the current, I, at the midpoint of the voltage, V, sweep in the negative direction, which neglects current contributions due to any redox reactions.

The I-V response for the SiNWs tested in aqueous solution, Figure 1(b), indicates an electrochemical reaction beginning during the positive potential sweep and no capacitive behavior is observed. The location and shape of this peak implies the oxidation of silicon to SiO_2[17] and is confirmed in the present study by the complete dissolution in HF of the NWs after cycling. It is well known that silicon carbide (SiC) coatings are stable in harsh chemical environments,[18,19] and thus a thin SiC layer is selected for chemically passivating the SiNWs. Herein, we deposit SiC onto SiNW arrays using low pressure chemical vapor deposition (CVD) (Tek-Vac CVD-300-M). 1,3-disilabutane (DSB, Gelest, inc., >95% purity) was used as the single source SiC precursor according to previously published growth parameters for polycrystalline SiC.[20] The deposition, performed after the removal of surface oxide in HF, was carried out at 800 °C, 5×10^{-6} Torr, and a flow rate of 5 sccm DSB. A deposition time of 3 min was used corresponding to a ~90 nm film, as measured on a planar Si (100) substrate coated at the same time. The films appear to coat the SiNWs conformaly as indicated by a lack of aggregated material or wire bridging in the representative SEM image provided of the wires post deposition in Figure 1(c). The SEM images indicate that the coating on the wires is qualitatively thinner than that obtained on the planar substrate, most likely due to limitations of precursor transport into the dense array.

The conformality and performance of the coating, in terms of passivating the SiNWs, is clear from the near ideal capacitance behavior during CV testing as indicated in Figure 1(b). The chemical identity of the coating is confirmed by Raman (HoribaJY LabRAM) spectra which show a broad peak corresponding to polycrystalline SiC,[21] see Figure 2(a). TEM images of the coated wires (JEOL 2010), Figure 2(a) inset, indicate a polycrystalline grain structure on the exterior, expected from SiC film growth under these conditions.[19] This is in contrast to the single crystalline morphology of the SiNW's as formed by this technique.[14] Furthermore, the robustness of the coating is demonstrated by a 95% capacitance retention for the coated arrays after 1000 charge/discharge cycles, presented in Figure 2(b).

The scalability of these materials, in terms of wire length and hence total energy storage, is investigated by synthesizing nanowires between ~7 and 32 μm in length (see Figure 3(a)), through varying the immersion time in the etch bath between 10 and 30 min. It is found that the capacitance increases linearly with the wire length, shown in Figure 3(b), as expected if the entire NW surface area is accessible to the electrolyte. The longest wire array tested, ~32 μm in length, exhibits a specific capacitance of ~1.7 mF/cm^2 projected area at a 50 mV/s scan rate, comparable to the state of the art carbon based micro-supercapacitor electrodes.[7–11] This corresponds to an energy storage capability of ~850 μJ/cm^2 projected area.

Along with the advantages in terms of processing and scalability of these materials as compared to typical micro-supercapacitor electrodes, the aligned nanowire configuration provides for excellent transport of ions to the active surface area. This is demonstrated by performing CV measurements over a wide range of scan rates from 10 mV/s to 5 V/s. The capacitive behavior of the materials is maintained over this

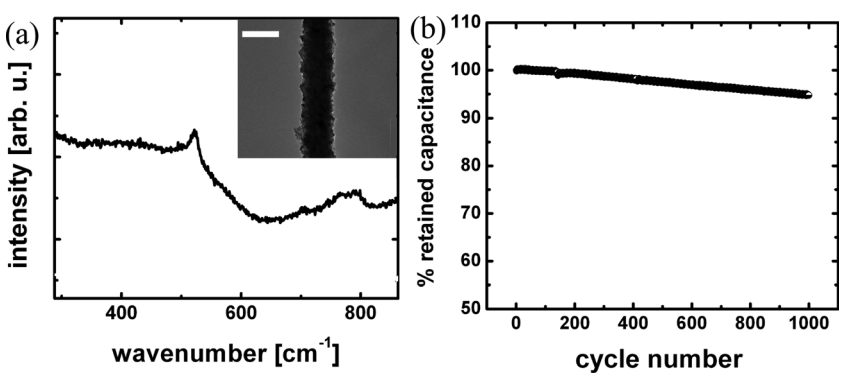

FIG. 2. (a) Raman spectrum of an isolated SiC/SiNW. A broad SiC band is prominent around 790 cm^{-1}, corresponding to polycrystalline SiC. Inset shows TEM image of wire indicating a rough polycrystalline coating, expected of SiC coating as deposited. Scale bar is 200 nm. (b) Capacitance retention results for SiC coated SiNWs. 95% of the original capacitance is retained after 1000 cycles. A 50 mV/s scan rate in 1 M KCl was used.

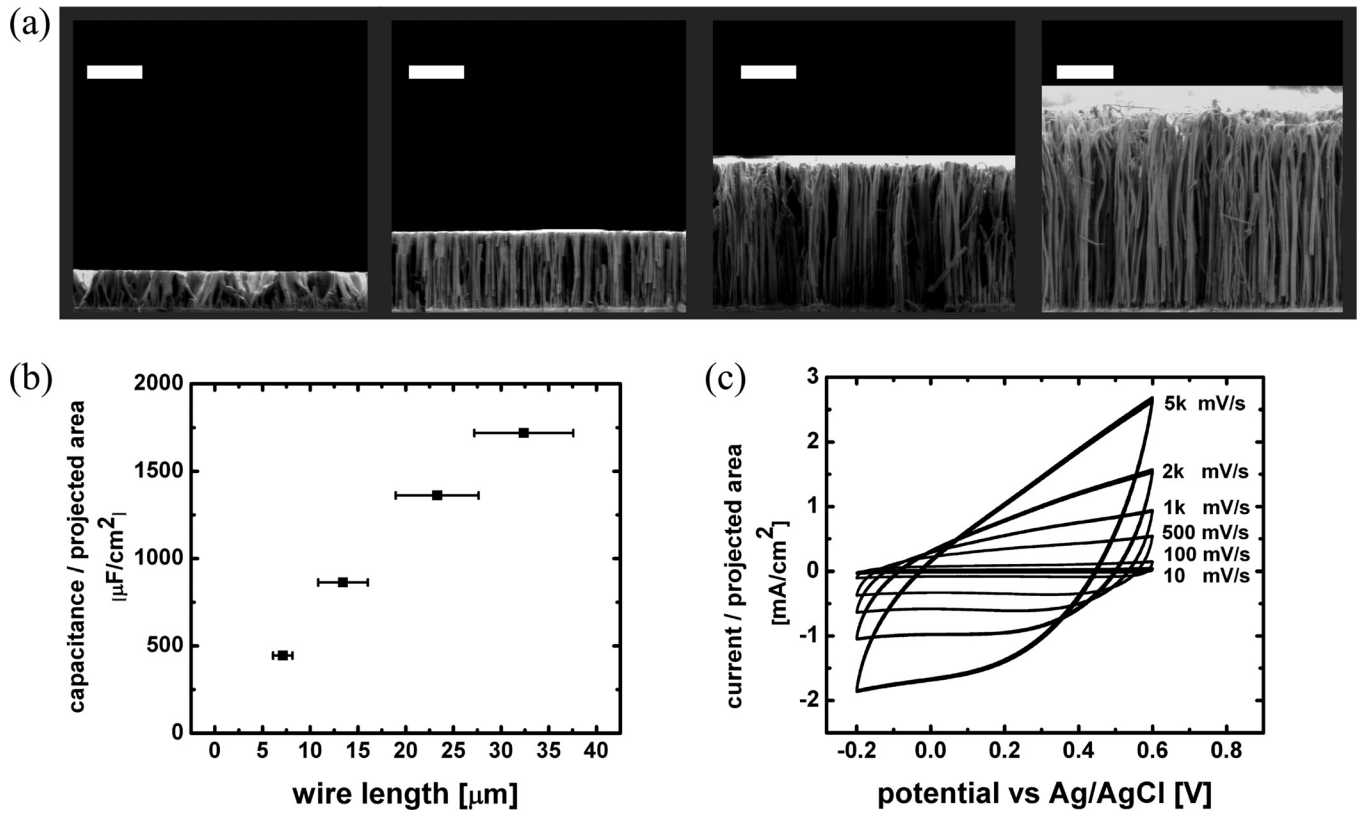

FIG. 3. (a) Cross sectional SEM images of SiC/SiNW arrays etched for different times, corresponding to results in (b). Scale bar is 10 μm. (b) Results of capacitance testing for SiC/SiNWs from (a) at 50 mV/s scan rate in 1 M KCl. (c) CV results for SiC/SiNWs (~13 μm in length) scanned over a range of 10 mV/s to 5 V/s in 1 M KCl.

range, see Figure 3(c), although a slightly more tilted I-V response, characteristic of resistive behavior, is observed.[22] This may be mitigated through the use of highly doped SiC films which are currently under investigation.

In summary, we have demonstrated the application of SiC coated wet-etch formed SiNWs as high-performance supercapacitor electrode materials for use with green electrolytes. The materials are fabricated in a facile and IC compatible scheme. The highest temperature used in the described process, 800 °C may also be further reduced by alternative SiC coating schemes, such as PECVD.[23] Capacitances of up to 1.7 mF/cm^2 are achieved, comparable to state-of-the art micro-supercapacitors, and remain stable over 10^3 charge/discharge cycles. As well, the nanowires as formed are in electrical contact with the underlying substrate, mitigating the requirement of an additional current collector and implying straight forward integration with Si chip based devices. We are currently investigating application of these energy storage materials for integration with on-chip sensors and actuators.

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[1]N. Tanner, J. R. Wait, C. R. Farrar, and H. Soon, J. Intell. Mater. Syst. Struct. **15**, 43 (2003).
[2]U. Kawoos, G. K. Mugalodi, M. R. Tofighi, S. Neff, and A. Rosen, in *Proceedings of 2005 IEEE 31st Annual Northeast Bioengineering Conference*, Hoboken, NJ, USA, 2–3 April (IEEE, Piscataway, NJ, USA, 2005), pp. 17–19.
[3]T. K. Bhattacharyya, S. Sen, D. Mandal, and S. K. Lahiri, in *Proceedings of the 19th International Conference on VLSI Design held jointly with 5th International Conference on Embedded Systems and Design*, Hyderabad, India, 3–7 January (IEEE Computer Society, Los Alamitos, CA, USA, 2006), pp. 4.
[4]D. R. Rolison, J. W. Long, J. C. Lytle, A. E. Fischer, C. P. Rhodes, T. M. McEvoy, M. E. Bourga, and A. M. Lubersa, Chem. Soc. Rev. **38**, 226 (2009).
[5]P. J. Hall, M. Mirzaeian, S. I. Fletcher, F. B. Sillars, A. R. Rennie, G. O. Shitta-Bey, G. Wilson, A. Cruden, and R. Carter, Energy Environ. Sci. **3**, 1238 (2010).
[6]P. Simon and Y. Gogotsi, Philos. Trans. R. Soc. London, Ser. A **368**, 3457 (2010).
[7]Y. Q. Jiang, Q. Zhou, and L. Lin, in *Proceedings of the 2009 IEEE 22nd International Conference on MEMS, Sorrento, Italy*, 25–29 January (IEEE, Piscataway, NJ, USA, 2009), pp. 587–590.
[8]F. Liu, A. Gutes, I. Laboriante, C. Carraro, and R. Maboudian, Appl. Phys. Lett. **99**, 112104 (2011).
[9]J. Chmiola, C. Largeot, P. L. Taberna, P. Simon, and Y. Gogotsi, Science **328**, 480 (2010).
[10]D. Pech, M. Brunet, P. L. Taberna, P. Simon, N. Fabre, F. Mesnilgrente, V. Condedera, and H. Durou, J. Power Sources **195**, 1266 (2010).
[11]D. Pech, M. Brunet, H. Durou, P. H. Juang, V. Mochalin, Y. Gogotsi, P. L. Taberna, and P. Simon, Nat. Nanotechnol. **5**, 651 (2010).
[12]J. W. Choi, J. McDonough, S. Jeong, J. S. Yoo, C. K. Chan, and Y. Cui, Nano Lett. **10**, 1409 (2010).
[13]K. Peng, Y. Shie, S. Gao, and J. Zhu, Adv. Mater. **14**, 1164 (2002).
[14]A. I. Hochbaum, R. Chen, R. D. Delgado, W. Liang, E. C. Garnett, M. Najarian, A. Majumdar, and P. Yang, Nature **451**, 163 (2007).
[15]M. Zahedinejad, M. Khaje, A. Erfanian, and F. Raissi, J. Micromech. Microeng. **21**, 065006 (2011).
[16]B. E. Conway, *Electrochemical Supercapacitors: Scientific Fundamentals and Technological Applications* (Plenum, New York, NY, USA, 2009), pp. 59–63.

[17]F. N. Jing, H. Tong, and C. M. Wang, J. Solid State Electrochem. **8**, 877 (2004).
[18]M. Mehregany, C. A. Zorman, N. Rajan, and C. H. Wu, Proc. IEEE **86**, 1594 (1998).
[19]C. Roper, V. Radmilovic, C. Carraro, R. T. Howe, and R. Maboudian, J. Electrochem. Soc. **153**, C562 (2006).
[20]M. B. J. Wijesundara, G. Valente, W. R. Ashurst, R. T. Howe, A. P. Pisano, C. Carraro, and R. Maboudian, J. Electrochem. Soc. **151**, C210 (2004).
[21]S. Rohmfeld, M. Hundhausen, and L. Ley. Phys. Rev. B **58**, 9858 (1998).
[22]E. Frackowiak and F. Beguin, Carbon **39**, 937 (2001).
[23]C. Iliescu, B. Chen, J. Wei, and A. J. Pang, Thin Solid Films **516**, 5189 (2008).