Silicon-Germanium Avalanche Receivers with fJ/bit Energy Consumption

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***Abstract*—Fast, low-noise and sensitive avalanche photo-receivers are needed for surging short-reach photonic applications. Limitations concerning bandwidth, throughput and energy consumption should be overcome. In this work, we comprehensively study the performance opportunities provided by avalanche p-i-n photodetectors with lateral silicon-germanium-silicon heterojunctions. Our aim is to circumvent the need for chip-bonded electronic amplifiers. In particular, we demonstrate that avalanche photodetectors based on silicon-germanium-silicon heterostructures yield reliable opto-electrical performances, with high gain-bandwidth products up to 480 GHz and low effective ionization ratios down to 0.15. Moreover, they improve power sensitivities for high-speed optical signals and have a low energy dissipation of only a few fJ per received information bit. These results pave the way for high-performing receivers for energy-aware data links, in next-generation short-distance data communications.**

***Index Terms*—Group-IV semiconductors; Integrated photonics; Avalanche photodetectors; Energy consumption; Short-reach communications; CMOS technology**

I. Introduction

THE relentless demands of data-hungry devices as in data centers [1], high-performance computers and servers [2] or big data clouds and storages [3] places exponential requirements on electrical wire signaling. Data overflow in metal wires is a critical bottleneck that hampers the take-off of such devices. The benefits of optical interconnects extend from long-distance to short-distance systems. Components used in long-haul systems are too costly and complex to be adopted in short-reach systems, however. Short-reach architectures comprise opto-electrical and electro-optical input/output (I/O) interfaces connected to basic building blocks such as circuit transceivers. Future transitions to Tbps communications and exascale computing levels [4] set new challenges in the following fields: increase and optimization of use bandwidths with allocation and dynamic scaling, high throughput, low-energy consumption and performance-cost trade-offs [5,6].

Integrated group-IV photonics is appealing for optical interconnects, in particular for optical transceivers . Transceivers combine transmitters and receivers in a single circuit. Their high-bit-rate and energy-aware operation is attractive for use in various types of devices. Photonic integration, thanks to group-IV semiconductors, should open a squeezing of complex functions into a single chip, while reducing process cost. Such integration also facilitates high-yield and large-scale electronics-photonics production. It is indeed based on mature complementary metal-oxide-semiconductor (CMOS) microelectronics processes [7-10]. Better connectivity and optimization at different levels (device, circuit, and system-to-network) are needed, however. On a component level, several levers are available to tackle on-going challenges. Optimizing optical receivers is key. High-speed receivers can be fabricated at reduced cost in CMOS cleanrooms [11,12]. However, they are still energy inefficient, for the most part [13-18].

A photonic receiver converts an incoming optical signal into an electrical one. Receiver designs are more complex for the digital-coherent systems used in long-haul communications. This is due to the multi-level modulation increasing spectral information density and to the digital signal processing (DSP) techniques used to compensate fiber-channel impairments [15-18]. In contrast, intensity-modulation and direct detection (IM-DD) receivers are preferred in short-distance connections, because of their simplicity [11]. Mainstream receivers are based on III/V [19,20] or silicon-germanium (Si-Ge) photodiodes [21]. They are then used together with an additional electronic circuitry with trans-impendence (TIA), limiting (LA) or gain-controlled (GCA) amplifiers. Digital-coherent and IM-DD receivers have different performance attributes to be considered, depending on the device targeted. The total energy consumed per transmitted information bit governs short-reach link scenarios [14].

Metal-semiconductor-metal (MSM) [22-25], p-i-n's [26-30], or avalanche photodetectors (APDs) [31-44] are widely used in Si-Ge receivers. MSM devices, having a Schottky barrier on

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Ge, typically have very high dark currents [22-24]. This not only limits the device sensitivity, but also dissipates a large amount of energy. P-i-n photodiodes are well-established options for digital-coherent and IM-DD receivers. They have very compact footprints and attractive opto-electrical performances. P-i-n devices are mature enough to yield high responsivities (up to the limit imposed by external quantum efficiency), fast responses and low dark-currents [26-30]. On the other hand, power sensitivity remains low or, at best, moderate for high-speed optical signals [30]. Enhancing p-i-n diode sensitivity may also help to improve the overall energy efficiency of the link by lowering the required transmitter power levels. To reduce energy consumption, the diode capacitance should be minimized [5,7]. Moreover, p-i-n photodiodes generate currents or voltages that are not high enough to enable direct signal processing. Further electronic stages are thus needed [22,23,30]. Adding CMOS electronics amplifies p-i-n's output, with, however, an increased parasitic load at the receiver front-end [12]. This is critical for receivers as a higher parasitic capacitance at the input of an amplification stage may deteriorate the overall device bandwidth (limiting thus the detection speed). The device will also consumes far more energy. If the noise current of the p-i-n diode, i.e. the intrinsic noise of device itself, is low – below 1 µA – the performance of a p-i-n photo-receiver is then limited by the noise of its electronic components [45-48]. Major energy savings thus result from the suppression of such electronic stages. Receivers with APDs are also attractive. Such receivers rely on diodes that generates internal gain through photo-carrier-initiated impact ionization. Avalanching the photodiode helps in improving the overall device performance, alleviating the high thermal noise of electronic amplifiers. APDs use MSM [24], p-i-n's [32-34,41], and separate absorption carrier multiplication (SACM) structures [31,35-38,42-44] together with, in some cases, electronic CMOS circuits. However, a prime concern of these devices is the trade-off between speed and optical power sensitivity. So-called "*receiver-less*" APDs, i.e. APDs without chip-bonded nor integrated circuit electronics, would be interesting in chip-scale interconnects, where high-speed, low-noise, and energy efficient operation is sought after.

In this work, we will thus comprehensively investigate the properties of p-i-n avalanche photodetectors with lateral Si-Ge-Si heterojunctions. In particular, we will demonstrate that Si-Ge-Si APDs yield fast, reliable and low-noise on-chip signal detection, improved sensitivity and a rather low fJ/bit energy consumption, without the need for additional electronic amplification components.

II. PHOTODETECTOR STRUCTURE AND FABRICATION

Our waveguide-integrated p-i-n APD is schematically shown in Fig. 1a. APDs were fabricated on 200 mm silicon-on-insulator (SOI) wafers with 220 nm thick silicon (Si) layers and 2 µm buried oxides (BOX's) using Si-foundry manufacturing processes [11,29].

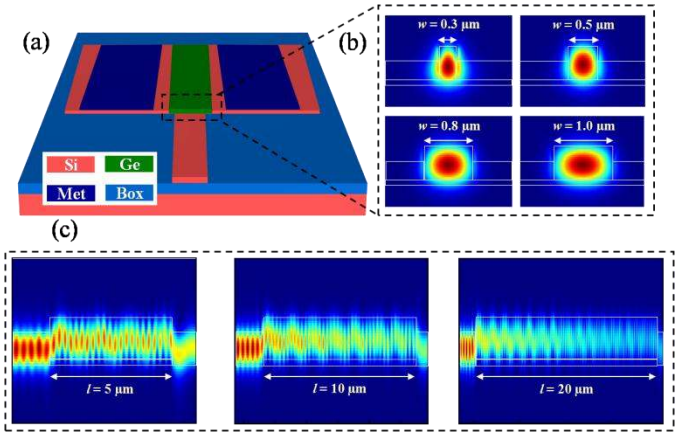

Fig. 1. (a) Schematics of the p-i-n photodetector with a lateral Si-Ge-Si heterojunction. (b) Optical mode profiles of p-i-n photodetectors with various cross-sectional areas. (c) Optical mode propagation through p-i-n photodetectors with various lengths.

The 260 nm thick Ge films at the center of the diodes were epitaxially grown in cavities with ~60 nm thick Si floors at the waveguide ends. Those intrinsic Ge films were sandwiched between ion implanted p-type and n-type Si slabs. Metal plugs and contact electrodes were latter on processed on Si regions only. Details on device fabrication in our Si-foundry facility can be found in Refs. [29,30]. Grating couplers and strip single-mode waveguides were used to efficiently butt-couple off-chip light into our w (width) × l (length) photodetectors. Couplers and waveguides operated with an in-plane waveguide polarization (quasi-TE polarization) at 1.55 µm wavelength. Butt-light-coupled p-i-n photodetectors are robust devices, enabling flexible engineering of opto-electrical performances through changes of the in-plane diode geometry [29]. Figure 1b shows mode profiles of the Si-Ge-Si photodetector for various intrinsic Ge region widths, while Fig. 1c show side views of the optical intensity flowing through various length butt-waveguide-coupled p-i-n photodetectors, modeled with a three-dimensional finite-difference time domain (3D FDTD) simulator.

III. RESULTS AND DISCUSSION

A. Current-voltage characteristics, responsivity and gain

Typical static current-voltage characteristics for different Si-Ge-Si photodetectors are shown in Fig. 2a and 2b in the dark and light illuminated states, respectively. Low dark currents (i_d) ranging from 60 to 200 nA at low operating voltages (from 0.5 V to 3 V) are obtained [48]. The dark current continuously rises up to 600 µA levels, when getting close to the avalanche breakdown. Junction breakdown bias are inversely proportional to the intrinsic diode width. They are around 9 V and 16.5 V for 0.3 µm and 1 µm wide devices, respectively. An optical laser source emitting light at a 1.55 µm wavelength was used to inject light into photodetectors thanks to a grating coupler and a butt-light-coupling scheme. The input optical power coupled into the devices was estimated to be -14 dBm. Responsivities and gains were quantified from photo-current-voltage measurements. The responsivity is the ratio between the net-light current and

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coupled input power ($R = i_{ph}/p_i$), while the gain is the ratio between the photo-responsivity and its reference ($M = R/R_r$). Table I summarizes reference responsivities at unity gain under 0.5 V reverse bias for different p-i-n photodetectors.

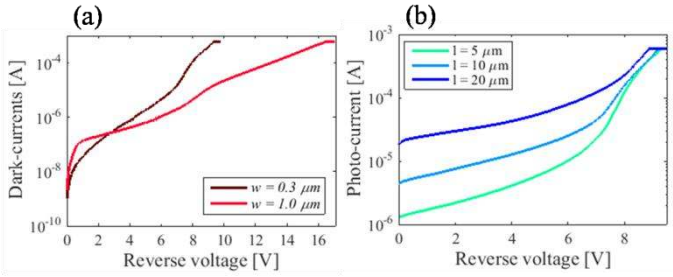

Fig. 2. Current-voltage characteristics (a) without and (b) with light coupled into the p-i-n photodetectors. 0.3 µm wide and 20 µm long or 1 µm wide and 40 µm long photodetectors were studied in (a). 0.3 µm wide photodetectors with different lengths (5, 10 and 20 µm) were probed in (b). The power coupled into the waveguide photodetectors was -14 dBm.

TABLE I
NOMINAL PHOTO-RESPONSIVITIES AT A UNITY GAIN

Width/Length [µm]	***l* = 5**	***l* = 10**	***l* = 20**	***l* = 40**
***w* = 0.3**	0.021	0.051	0.21	-
***w* = 0.5**	-	0.085	0.35	0.51
***w* = 0.8**	-	-	0.47	0.73
***w* = 1.0**	-	-	0.76	1.16

Note: Reference responsivity is defined as net-light current over power coupled into the device at 0.5 V reverse bias.

Figure 3 shows the avalanche multiplication gain as a function of operating reverse bias for different photodetector geometries. This includes variations in device lengths for 0.3 µm wide structures (Fig. 3a) and variations in device widths for 20 µm long devices (Fig. 3b).

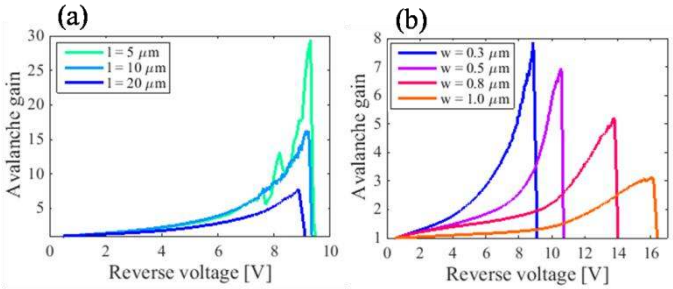

Fig. 3. Gain-voltage characteristics of p-i-n photodetectors for (a) 0.3 µm wide devices with different lengths (5, 10 and 20 µm) and (b) 20 µm long devices with different widths (0.3, 0.5, 0.8 and 1.0 µm).

For a fixed intrinsic Ge region width, the gain is larger in shorter devices. Meanwhile, for the same intrinsic Ge region length, the avalanche multiplication gain is lower in wider photodetectors. These trends are due to several factors and their interplay. First, and in line with the very low nominal responsivities reported in Tab. I, shorter devices absorb less input power. A substantial part of the light thus scatters towards the Si regions, where the impact ionization occurs, resulting in a stronger avalanche effect. As the Si-Ge-Si photodiode is actually an extension of the Si waveguide, it is indeed clear from Fig. 1c that a significant amount of input power is present at the "waveguide" end in shorter diodes. Incident photons are then not fully absorbed by a short intrinsic zone. They are instead subjected to a stronger impact ionization. Nominal responsivities are improved to 0.62, 0.82, and 1.66 A/W with multiplication gains of 29.4, 16.2, and 7.9 for 5, 10, and 20 µm long devices with, nominally, a 0.3 µm wide intrinsic Ge zone. The evanescent tails of the quasi-TE mode otherwise have, as shown in Fig. 1b, large overlaps with lateral Si slabs in narrow photodiodes. This may partially explain the higher multiplication gains in such structures. Although it is undesirable for low-voltage operation (due to the larger absorption loss) [48], a judicious narrowing of the intrinsic diode region might thus help in reaching better responsivities (under avalanche operation) in such devices. Electric fields are indeed strong in narrow Si-Ge-Si diodes. This, in turn, substantially contributes to diode avalanching, even at lower voltages. However, wider photodetectors show better modal confinement inside the intrinsic Ge region [29,30], yielding a much better modal absorption coefficient [26]. This improves nominal diode responsivities, also in line with Tab. I values. As a result, improved responsivities up to 1.66, 2.42, 2.44, and 2.36 A/W were obtained through avalanche multiplications of 7.9, 6.9, 5.2, and 3.1 in 0.3, 0.5, 0.8, and 1 µm wide photodiodes with the same 20 µm length.

B. Bandwidth, gain-bandwidth product and noise

Bandwidth properties of Si-Ge-Si APD photodetectors were assessed using small-signal radio-frequency (RF) tests with a help of Lightwave Component Analyzer (LCA) by measuring the S_{21} response in the 0.1 up to 50 GHz range [29,48]. Figures 4a to 4d show normalized RF responses for different p-i-n APD geometries biased at reverse voltages of 6 V (0.3 and 0.5 µm wide structures) and 10 V (0.8 and 1.0 µm wide structures), respectively. Small-signal RF measurements were perfomed at a *C*-band wavelength of 1.55 µm, with an optical input power coupled to the devices around -16.5 dBm.

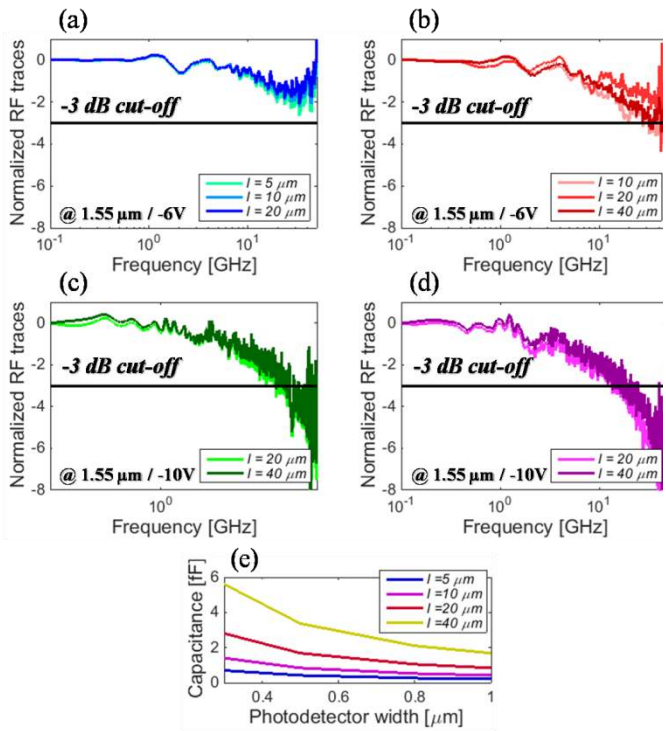

Fig. 4. Normalized frequency responses for different p-i-n APD geometries. (a) 0.3 µm wide by 5, 10, and 20 µm long, (b) 0.5 µm wide by 10, 20, and 40 µm long, (c) 0.8 µm wide by 20 and 40 µm, and (d) 1.0 µm wide by 20 and 40 m long devices. (a) and (b) devices were biased at -6V, while(c) and (d) devices were biased at -10V. The optical power injected into the device was -16.5 dBm at a 1.55 µm emission wavelength. (e) Estimated junction capacitance of the diode versus the intrinsic region width.

Figure 5 sums up -3-dB bandwidths as functions of operating reverse voltages for different Si-Ge-Si APD photodetectors.

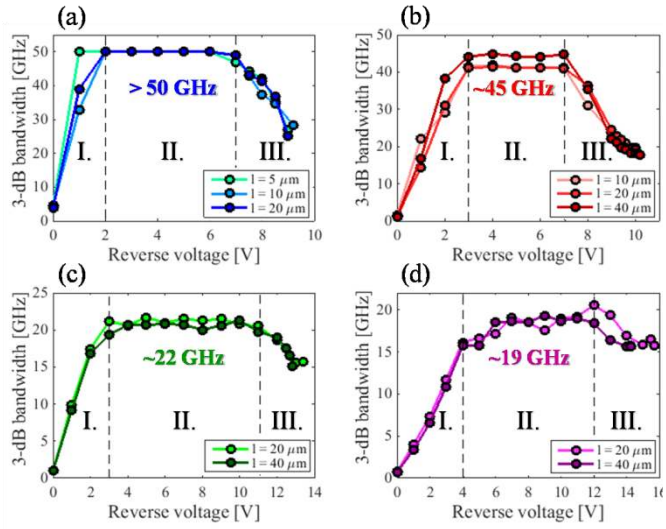

Fig. 5. -3-dB bandwidth versus reverse voltage for p-i-n APD photodetectors with different lengths (see the insets) and various intrinsic region widths: (a) 0.3 µm, (b) 0.5 µm, (c) 0.8 µm, and (d) 1.0 µm. The optical power coupled into the devices was -16.5 dBm.

In all cases, we can clearly distinguish three operation regimes. (I.) Under low-voltage operation, typically in the 0 to 4 V range, the cut-off frequency steadily increases with increasing voltage until the maximum bandwidth is reached [48]. The bias at which the maximum cut-off is reached changes with the intrinsic diode width. Sub-µm dimensions indeed facilitate the generation of high electrical fields inside the diode, helping in avalanching the diode at lower voltages. Maximum bandwidths are larger than 50 GHz (upper limit of our LCA) for 0.3 µm wide structures. They are equal to 45, 22, and 19 GHz for 0.5, 0.8, and 1 µm wide devices. Let us now exclude zero-bias operation and focus instead on the 1 to 4 V operating range. Built-in electrical fields are then strong enough to effectively collect generated electron-hole pairs (region (I.) in Fig. 5 graphs). This is also in line with improved reference responsivities at 0.5 V reverse bias and beyond [30,48]. For higher reverse bias, the -3-dB bandwidths, having reached their maxima, remain stable (region (II.) in Fig. 5 graphs). In this regime, photo-carriers generated by the diode reached their saturation velocity. In regimes (I.) and (II.), the avalanche multiplication gain slowly increases, as well, because of continuous impact ionization, without impairing yet the device frequency response. Operating the diode at even higher voltages, i.e. in region (III.) of Fig. 5 graphs, exponentially amplifies the photo-current and the diode bandwidth starts to drop because of the prevalent ionization build-up time. The bandwidth drop from its peak is much larger in 0.3 µm and 0.5 µm wide photodiodes than in their 0.8 µm and 1 µm wide counterparts. The bandwidth is indeed reduced from 50 and 45 GHz down to ~20 GHz in the former two configurations. This reduction is comparatively small in the latter two configurations, from 22 and 19 GHz down to ~15 GHz. This is likely due to the stronger electrical fields inside narrow than in wide detectors, with therefore higher overall multiplication gains. Moreover, and in line with previous low-voltage-only demonstrations [48], the frequency response of Si-Ge-Si heterostructure photodiodes operated in the avalanche mode only is the same for devices of same widths, but different lengths. It however decreases for wider structures. Heterostructure APDs thus seem not to be limited by the resistance-capacitance product (virtually the same frequency responses within Figs. 4a to 4d). The junction capacitance as a function of the intrinsic diode width is shown in Fig. 4e. The APD speed is instead mainly restricted by the longer carrier transit time (considerably different frequency responses in Figs. 4a to 4d). Adjusting the photodetector length could therefore be harnessed to engineer the static photo-responses (responsivity and gain) without impacting the detection speed, as the avalanche build-up time depends only on diode width and not on length. Experimental electrical eye diagram outputs for 0.5 µm wide and 40 µm long p-i-n APD heterostructure in the three operation regimes are shown in Fig. 6 for a pseudo-random bit sequence at 10 and 40 Gbps data rate.

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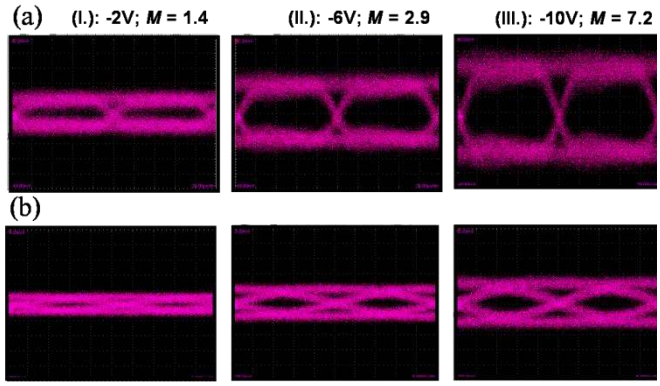

Fig. 6. Eye diagram apertures of w =0.5 µm and l = 40 µm p-i-n avalanche photodetectors in regimes (I.), (II.) and (III.) for transmission bit rates of (a) 10 Gbps and (b) 40 Gbps. The optical power coupled into the devices was about -14.5 dBm.

Figure 7a shows Si-Ge-Si APD gain-bandwidth products (GBPs) for various intrinsic diode region widths. GBPs reached 480, 220, 90, and 50 GHz for p-i-n photodetectors with 0.3, 0.5, 0.8, and 1.0 µm. High GBPs mean that APD are capable of high-speed operation with low noise level. APD's GBP and noise are indeed depending, for a given material, on the ionization coefficients of electrons and holes within the diode's avalanching zone. They more precisely depend on the effective ionization factor (k), which is the ratio of ionization coefficients for electrons (α) and holes (β), i.e. $k = \alpha/\beta$ [47,49,50]. For bulk Ge, k is close to unity ($k \sim 0.9$) as α and β parameters are similar, particularly at high electrical fields. In contrast, the ultra-low k of Si ($k < 0.1$) is advantageously used in many APD designs at visible and near-IR wavelengths [21]. Figure 7b shows the effective ionization coefficient as a function of the avalanche multiplication gain reachable in our heterostructured Si-Ge-Si APDs. Operating avalanche multiplication gains, extracted from measurements, are in the 1 to 8, 1 to 7, 1 to 4 and 1 to 3 ranges for 0.3, 0.5, 0.8 and 1 µm wide photodetectors, respectively.

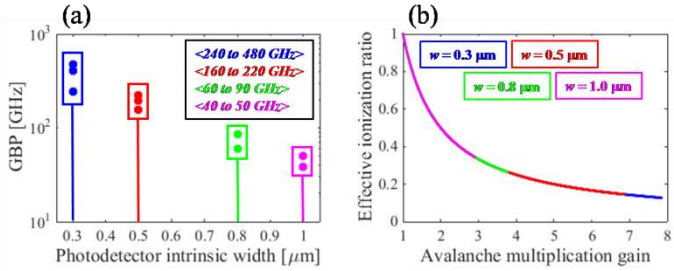

Fig. 7. (a) Gain-bandwidth product as a function the intrinsic region width. (b) Estimated effective ionization ratio as a function of the avalanche multiplication gain for p-i-n photodetectors with different intrinsic zone widths.

In Figure 7b, there is an exponential-like decay of the estimated k-factor as the avalanche multiplication gain increases. Such a trend is in line with GBP evolution (shown in Fig. 7a). Indeed, larger GBPs correspond to lower effective ionization ratios, and vice versa [31-37,41]. From a device geometry point of view, narrower APDs have larger bandwidths and higher multiplication gains, while wider APD have transit-time-limited bandwidths and smaller avalanche multiplication factors. As a result, avalanche diode operation in a mode that has a marginal effect on the bandwidth, and thus on the device speed, corresponds also to the mode that yields low k values (and low avalanche excess noise). Then, the values of k-factor can be estimated as follows $M < 1/k$ [49]. Indeed, high-speed and low-noise operation happening simultaneously is the most attractive practical scenario in an APD. Theoretically, ultra-low k-values of 0.13 - 0.15 only are expected for the smallest diode geometries. Low k values stemming from an aggressive shrinking of the diode geometry would be associated with low avalanche excess noises in Si-Ge-Si APDs. Such reduced excess noises would leverage strongly localized impact ionization at Si-Ge interfaces because of the dead-space effect [32,34,37,41].

C. APD sensitivity and optimal operation

After evidencing high GBPs that would be due to low k-values, we then had a look at the sensitivity of those Si-Ge-Si APDs. Sensitivity analysis was carried out for various APD geometries to estimate their theoretical performances and determine their optimal operation point (defined at a reverse bias that yields the minimum device sensitivity). APDs had different geometries (width × length): 0.3 µm × 20 µm, 0.5 µm × 40 µm, 0.8 µm × 40 µm and 1 µm × 40 µm. The sensitivity to received optical power at a bit-error-rate (BER) of 1×10^{-9} was calculated using the model described in Refs. [50], for 10, 40, and 80 Gbps transmission bit rates. Figure 8a to 8d show power sensitivities of Si-Ge-Si APDs as functions of operating reverse bias for different geometries and thus gain ranges: 1 to 8, 1 to 7, 1 to 4 and 1 to 3, respectively. Magenta and black vertical lines in Figs. 7 show optimum operation points and ±2 V variations around them. Avalanching Si-Ge-Si p-i-n diodes always have a better sensitivity compared to reference points at 0.5 V bias. The sensitivity enhancement compared to the reference value is otherwise larger for device operating with higher multiplication gains, i.e. for narrower APD designs. For 10, 40, and 80 Gbps transmission bit rates, power sensitivities are equal to -18.5, -15.4, and -13.3 dBm for 0.3 µm wide and 20 µm long APDs (-22, -19, and -17.4 dBm for 0.5 µm wide and 40 µm long APDs), see Fig. 8a (Fig. 8b). The optimum operating points otherwise increase with the size of the intrinsic region, from 7 V up to 8V, 11 V and 12.5 V. Those operation optima are close to the boundaries between APD regimes (II.) and (III.) in Fig. 5 graphs showing the experimental bandwidths as functions of the reverse voltage. This means that high-speed and low-noise APD operation is feasible, this with the best-possible device sensitivity. Indeed, lower k-factors enable avalanche multiplication to be obtained before the speed limit, improving thereby the sensitivity to low optical signals. It is also clear, when looking at Fig. 8 graphs, that wider APDs yield better sensitivities for a fixed data rate. Those improved sensitivities are attributed to higher nominal photo-responsivities. The sensitivities for 10 and 40 Gbps bit rates are -21.7 and -18.7 dBm for 0.8 µm wide by 40 µm long diodes, and -23.1 and -20 dBm for 1µm wide by 40

μm long diodes. A stable APD operation is also of practical interest. According to sensitivity predictions, a negative bias variation of -2 V deteriorates the optimal sensitivity by an amount less than for positive bias variations (+2V). Although higher voltages can provide higher operating gains, further sensitivities improvements are hindered by high dark currents which then become limiting. In that situation, the APD sensitivity deviates far more from its optimum due to operation close to the avalanche breakdown. This suggests that sensitivity performance of heterostructured Si-Ge-Si APDs is mostly limited by dark currents instead of avalanche-related aspects such as ionization build-up time or excessively large multiplication avalanche noise.

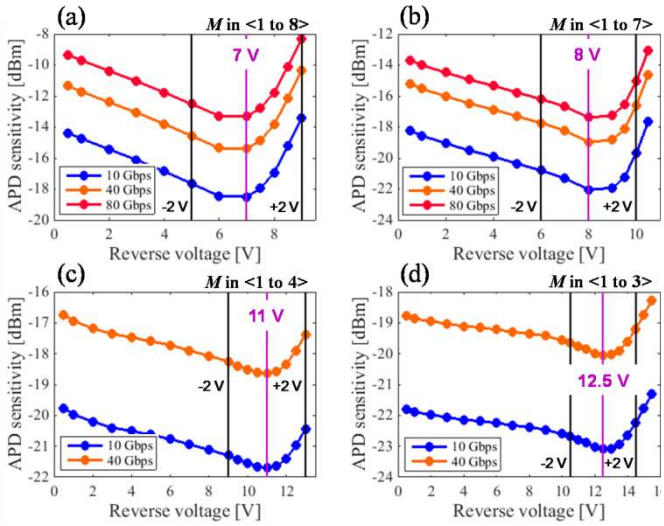

Fig. 8. Calculated optical power sensitivities of p-i-n photodetectors with the following intrinsic region geometries: (a) 0.3 μm × 20 μm, (b) 0.5 μm × 40 μm, (c) 0.8 μm × 40 μm, and (d) 1.0 μm × 40 μm.

D. *Energy efficiency*

Although APDs with electronic CMOS circuitry are used in short-reach interconnections, APDs without additional amplification stages are very compelling because of promising energy savings [2,4,5]. We further elaborate on that by analyzing the energy consumption of Si-Ge-Si photodetectors. The energy consumption (η_e) is defined as a ratio of the by-product of a single driving voltage and total (signal and noise) current generated by the APD and given transmission bit rate [23,50]:

$$\eta_e = \frac{u \cdot \left\langle i_o^2 \right\rangle}{br} \tag{1}$$

where u is the operating reverse voltage of single power supply, br is the transmission bit rate and $\left\langle i_o^2 \right\rangle$ is the total current, i.e. signal and noise current, generated by the APD. The total current is characterized by the shot current noise $\left\langle i_s^2 \right\rangle$ and thermal current noise $\left\langle i_t^2 \right\rangle$. Shot and thermal noise currents are given by $\left\langle i_s^2 \right\rangle = 2qM^2\left(i_{ph} + i_d\right)F\left(M\right)\Delta f$ and $\left\langle i_t^2 \right\rangle = \dfrac{(4k_B T \Delta f)}{R_l}$, respectively. Here, q is the electron charge which is equal to 1.60217662×10^{-19} C, M is the multiplication gain, i_{ph} and i_d are generated photo- and dark-current, $F(M) = (k\cdot M) + (1-k)\cdot(2-1/M)$ is the avalanche excess noise, Δf the receiver bandwidth ($\Delta f \approx br/2$ for a non-return-to-zero bit streams), k_B is the Boltzmann constant, i.e.1.38064852×10^{-23}m^{2}kgs^{-2}K^{-1}, T is the room temperature, and R_l is the load resistance [47,50].

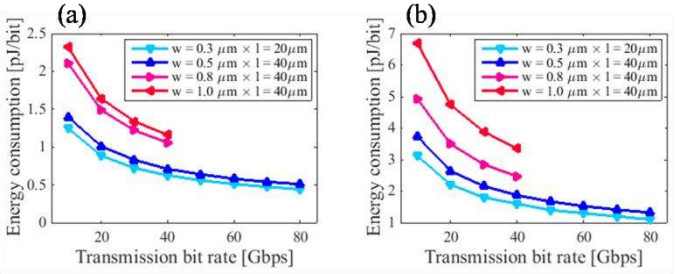

Fig. 9. Energy consumption as a function of transmission bit rate for different p-i-n avalanche-operated photodetectors: (a) at the optimal operation point and (b) under operation at 90% of the avalanche breakdown voltage.

Figure 9 shows the estimated energy consumption of different Si-Ge-Si APDs as a function of detection bit rate. For this analysis, devices are either operated at the optimal reverse bias point (Fig. 9a) (i.e. corresponding to minimal power sensitivity) or at 90% of the avalanche breakdown voltage (Fig. 9b). APD geometries are the same as those used for the sensitivity performance study. In all situations, the energy consumption of heterostructured APDs is very low, a few fJ/bit only. Wider APD devices (0.8 and 1 μm diodes) consume more energy than their narrower counterparts (0.3 and 0.5 μm). Energy consumption is otherwise less when operating Si-Ge-Si APDs at their optimal reverse biases (7, 8, 11, and 12.5 V), with therefore high-speed, low-noise, and high sensitivity, than at 90% of the avalanche breakdown (at 8.1, 9.9, 12.5, and 14.1 V, then). In particular, the estimated energy consumption of APDs operating at their optimal point is in the 1 to 1.5 fJ/bit range for 40 Gbps. At 90% of the avalanche breakdown, it is in the 1.7 to 3.6 fJ/bit range. The higher levels of dissipated energy in the latter case are due to sensitivity degradation, higher dark-currents and bandwidth-limited operation because of the avalanche build-up time. Nevertheless, the energy consumption of Si-Ge-Si APDs is in both situations, much lower than in conventional low-voltage-operated diodes [22,23,48] and can be competitive to other Si-Ge APD configurations with additional electronic amplification circuits [15-18,42,43]. This makes heterostructured Si-Ge-Si APDs promising for applications in short-reach chip interconnects, where the total energy is limited.

IV. Conclusion

In summary, we conducted a comprehensive analysis of

high-speed APDs based on p-i-n structures with lateral Si-Ge-Si heterojunctions. High-speed and low-noise opto-electrical performances were obtained simultaneously in those Si-foundry-compatible APDs, together with enhanced power sensitivities and really low energy consumption of a few fJ/bit. Low-cost heterostructured Si-Ge-Si photodetectors thus have a bright future in on-chip energy-hungry photonic systems.

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Guy Aubin received the Engineer Diploma degree from the École Nationale Supérieure des Télécommunications de Bretagne (now IMT Atlantique), Brest, France, and the M.Sc. degree in information processing from the University of Rennes, France, in 1981. He taught electronics at university level during his National Service. He was engaged with Orange Labs (formerly France Télécom R&D or CNET) in 1983. He was the Head of the Transmission Experimentation Group, Submarine Networks Department, Issy-les-Moulineaux. He contributed to several world premieres of optical transmission demonstrations in the laboratory and to field trials of successive generations of optical systems. He moved to the Concept and Device for Photonics Laboratory, Bagneux, in 1999. In 2001, he joined the Laboratory for Photonics and Nanostructures, Centre National de la Recherche Scientifique at Marcoussis, whose structure has been now included in the Centre of Nanoscience and Nanotechnology since 2016. There, he leads the Experimentations Fiber Optic and RF Team. His research interests include new functionalities for next-generation communication networks with innovative all-optical or optoelectronics devices.

Jean-Michel Hartmann explored, while pursuing the Ph.D. degree at CEAIRIG, Grenoble, France, from 1994 to 1997, the atomic layer epitaxy of CdTe, MnTe, and MgTe for low dimensional structures. During his stay with Imperial College London from 1997 to 1999, he investigated the gas source molecular beam epitaxy of Si/SiGe heterostructures for transport purposes. Since 1999, he has been a permanent position Researcher with CEA-LETI, Grenoble, where he is currently coordinating the Group-IV epitaxy activities for nanoelectronics and photonics.

Farah Amar received the master's degree in telecommunications and RF from Limoges University, Limoges, France, in 2016. In 2017, she joined the Centre for Nanoscience and Nanotechnology (C2N), a joint Laboratory of CNRS, University of Paris Sud, and University of Paris Saclay, France. She works as an RF and Optoelectronic Engineer with the Experimentations Fiber Optic and RF (EXPERFO) Team.

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Delphine Marris-Morini is currently a Professor with Paris Sud University. Her research interests at the Center for Nanosciences and Nanotechnologies include silicon photonics in the near-IR and mid-IR wavelength range. She has published over 100 journal articles. She has been in charge of the group of Micro and Nanophotonic devices on silicon since 2015. She received an ERC Starting Grant (INsPIRE) on Ge-rich photonic integrated chips towards the mid-IR wavelength range for sensing and spectroscopic application. She also received the Bronze Medal from CNRS in 2013.

Frédéric Boeuf was born in 1972. He received the M.Eng. and M.Sc. degrees from the Institut National Polytechnique de Grenoble in 1996 and the Ph.D. degree from the University Joseph Fourier of Grenoble, France, in 2000. Then, he joined STMicroelectronics, where he is involved in advanced devices physics and integration, advanced CMOS devices, and silicon photonics. He is currently a STMicroelectronics Fellow and also managing the Silicon Photonics Technologies Group inside STMicroelectronics's Technology and Design Platform Organization. He has authored or coauthored over 250 technical articles.

Jean-Marc Fédéli received the electronics engineer diploma degree from INPG Grenoble in 1978. Then, he was involved with CEA-LETI in the development of various magnetic memories and magnetic components as the Project Leader, the Group Leader, and a Program Manager. For two years, he acted as the Advanced Program Director with Memscap Company for the development of RF-MEMS. Then, he returned to CEA-LETI in 2002 as a Coordinator of silicon photonic projects up to 2012. Under a larger research partnership, he works on many technological aspects on photonics on CMOS (Si rib and stripe waveguides, a-Si waveguides, and slot waveguides), Si modulators, Ge photodetectors, and InP integrated sources on Si. He has been participating on different European projects, such as EPIXFAB for MPW circuit fabrication, and has coordinated the FP7 PLAT4M project on silicon photonics platform. Since 2014, he has moved to sensing activities with photonics. He is currently a Technical Manager of the H2020 MIRPHAB pilot line on liquid and gas systems sensors. His H factor is around 35 with more than 200 publications and 50 patents. He has written three book chapters: one on magnetic recording and two on silicon photonics.

Bertrand Szelag received the master's degree in physics from the University of Lille in 1994 and the Ph.D. degree in microelectronics from the University of Grenoble in 1999. He was a Visiting Researcher with Tohoku University in 1997, where he was involved in the field of sub-100-nm CMOS transistor properties. In 1998, he joined Thomson Composants Specifiques. In 1999, he moved to STMicroelectronics to work on BiCMOS platform development for Analog/RF applications. He also developed devices for RF power applications. Since 2013, he has been with LETI, MINATEC Institute, Grenoble, France, as a Project Manager and a Senior Process Integration Researcher in the field of silicon photonic devices. He is currently the Head of the Silicon Photonic Laboratory, CEA-LETI. He is also the author or coauthor of more than 50 articles in scientific journals and international conference proceedings in the field of CMOS, bipolar and DMOS transistors, and silicon photonic devices. His current research activities include high speed silicon modulator, germanium photodetectors, and hybrid III–V laser integration in silicon.

Laurent Vivien is currently the CNRS Director of Research with the Centre for Nanoscience and Nanotechnology (C2N), a joint Laboratory of CNRS, University of Paris Sud, and University of Paris Saclay, France. Since 2016, he has also served as the Deputy Director of C2N and the Director of the Photonics Department. His research activities focus on the development of fundamental concepts for silicon photonics, including optoelectronic and hybrid photonic devices. He demonstrated high-speed waveguide integrated germanium photodetectors and carrier depletion-based silicon modulators. He has also been at the forefront of the development of hybrid integration of carbon nanotubes on Si photonics platform and recently on high-speed Pockels effect in strained silicon waveguides. In 2015, he received the European Research Council (ERC) grant as a consolidator on the development of strained silicon photonics platform.