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Silicon Microfabrication Technologies for Nano-Satellite Applications

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Abstract

Silicon (Si) has a strength to density ratio of 3.0(σ_y/δ=(6.8Gpa/2.3g/cc)), an order-of-magnitude higher than titanium, aluminum, or stainless steel. Silicon also demonstrates favorable thermal, optical, and electrical properties making it ideal for use as a structural foundation for autonomous, mesoscopic systems such as nanosatellites. Using Si substrates, a structure that can simultaneously act as a thermal management system, a radiation shield, an optical material, a package, and a semiconductor substrate can be realized.

Introduction

Recently, several semiconductor fabrication processes have been developed to enable the use of Si substrates as structural foundation for autonomous, mesoscopic systems. Perhaps the most important development has been a deep reactive ion etch (DRIE) process which has revolutionized the concept and implementation of mixed technology integration. Using the DRIE process, a Si substrate may be etched to specific depths with highly controlled lateral dimensions. This allows accurate alignment of dissimilar components and materials to one another and accurate wafer-to–wafer alignment. Utilizing on-chip microelectronic and mechanical structures, this technology will enable fabrication of a self-contained, highly versatile, integrated microsystem that will minimize volume, weight, and power requirements. DRIE also enables the pursuit of a collection of advanced packaging capabilities to address the need for complex microsystems that combine multiple materials and functions in a single package or assembly.

Discussion and Results

Pattern transfer into Si has been very successful by both wet chemical and plasma etch techniques. However, the fabrication of deep, high-aspect ratio Si structures has been limited due to low etch selectivity to photoresist masks, slow etch rates, or poor lateral dimensional control. The recent development of the DRIE Si etch process has resulted in anisotropic profiles at room temperature, etch rates > 3.0 μm/min, aspect ratios >30:1, and good dimensional control. Additionally, DRIE has shown etch selectivities of Si to photoresist >75:1 thereby eliminating the use of hard etch masks for features deeper than 100 μm.

The DRIE process (patented by Robert Bosch GmbH) [1] relies on an iterative inductively coupled plasma (ICP) deposition/etch cycle in which a polymer

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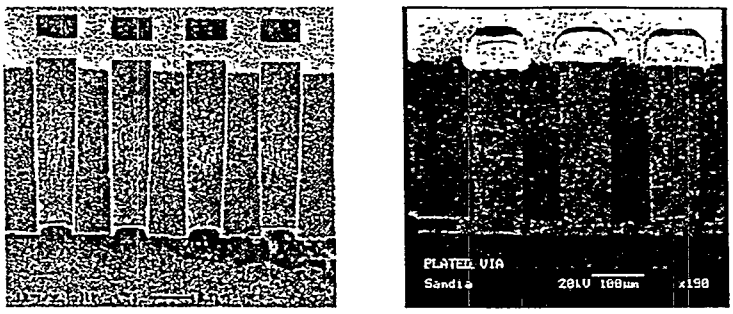
etch inhibitor is conformally deposited over the wafer during the deposition cycle. The polymer deposits over the resist mask, the exposed Si field, and along the sidewall. During the ensuing etch cycle, the polymer film is preferentially sputtered from the Si trenches and the top of the resist mask due to the acceleration of ions (formed in the ICP plasma) perpendicular to the surface of the wafer. Provided the ion scattering is relatively low, the polymer film on the sidewall is removed at a much slower rate, thus minimizing lateral etching of the Si. Before the sidewall polymer is completely removed, the deposition step is repeated and the cycle continues until the desired etch depth is obtained.

Through-wafer plated vias for electrical interconnects are used in many integrated microsystems including nano-satellites. Recently, a robust electroplated via technology for through-wafer interconnects has been developed using several microfabrication processes. These processes included Si DRIE to form the through-wafer via holes, steam oxidation to isolate the metal via plugs from the silicon substrate, and electroplating to form the metal plugs. As shown in Figure 1a, 100 μm wide vias are formed in ~ 425 μm thick Si using the DRIE process. Electrical isolation of the silicon substrate from the metal via plugs is achieved using steam oxidation. For high aspect ratio (>1:1) vias, neither LPCVD nor PECVD deposition processes will adequately isolate the via. These processes are limited by the diffusion of large molecules into the via and the diffusion of reaction products out of the via. As a result, the deposited film thickness decreases with depth into the via.

However, steam oxidation of silicon can completely insulate vias by growing the oxide in place, rather than depositing films onto exposed surfaces. In this case, only water and oxygen molecules need to enter the via while hydrogen is the only reaction product. The oxide grown in the vias is uniform throughout the entire depth. The rate of oxidation of films over 1000 Å thick is limited by diffusion of water and oxygen through the existing oxide film. At one atmosphere pressure, the practical limit for oxide growth is about 2 μm at 1200°C. In high pressure (25 atmospheres) oxidation systems, it is possible to grow thicker films in shorter times or to oxidize at temperatures as low as 500°C. The breakdown voltage for steam oxidized films is about 100 volts per μm film thickness.

Following oxidation, the vias are electroplated using the following process. A copper substrate is coated with polymethylmethacrylate (PMMA) photoresist and solvent bonded to the Si wafer. The PMMA is removed in the via locations with a deep ultraviolet (DUV) blanket exposure and development cycle using the oxidized silicon wafer as a stencil mask. The vias are then electroformed using an electrolytic nickel deposition. Finally the copper plating fixture is completely removed in a simple wet etch process. Plated vias are shown in Figure 1b for 100 μm wide vias. A series of plated vias were tested electrically and determined to be isolated from the Si wafer. A similar fabrication sequence for copper and gold vias is also possible, as well as for nickel-iron (Permalloy) to allow the incorporation of through wafer magnetic flux paths.

Another fabrication process required for integrated microsystems is wafer bonding. There are many device applications that can benefit from joining two silicon wafers or a silicon and Pyrex wafer. These seals could be hermetic, which

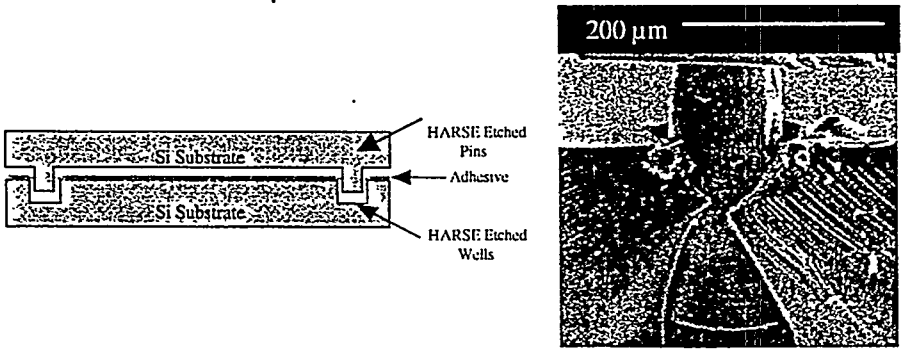


(a) (b)

Figure 1. SEM micrographs of 100µm diameter vias a) etched using the DRIE process and b) Ni electroplated.

allows silicon to serve as a packaging medium as well as a device substrate. If two or more substrates can be accurately aligned before sealing, the possibility for making inexpensive and sophisticated devices from divergent technologies exists. After wafer bonding occurs, the resultant sealed devices can be diced into individual packages.

DRIE provides a process which enables accurate alignment of wafers as well as precision die-to-wafer alignment for advanced packaging technologies. A Si substrate can be etched to multiple, specific depths while retaining accurately controlled dimensions in the mask plane. This permits accurate alignment of discrete components to one another with alignment tolerances < 5 µm. In Figure 2, the DRIE process was used to accurately align two Si samples to one another. A 130 µm wide pin was DRIE etched in the top Si wafer while a 132 µm wide well was DRIE etched in the bottom Si wafer. The pins and wells were aligned and then attached using a UV curing adhesive to tolerances of < 5 µm on pieces ~ 10 cm^2. Using a slightly different pattern, pieces as large as ¼ of a 3 inch Si wafer have been aligned to tolerances of ~25 µm.



(a) (b)

Figure 2. Schematic (a) and (b) SEM micrograph or DRIE etched Si pins and wells for precision alignment for advanced packaging technologies.

Wafers can then be bonded together using a number of different techniques. Commercially available wafer alignment/bonding systems are available with alignment accuracies of ± 2 µm. These machines can heat to 600°C, and apply

programmed pressure, and voltage for anodic bonding. They can also provide a controlled atmosphere or vacuum during the bonding process. Wafer bonding techniques include: direct wafer fusion, anodic bonding, frit glass bonding, solder bonding, and adhesive bonding. In direct wafer fusion, wafers are aligned and bonded at 600°C with no additional material. The lightly bonded wafers are then transferred to a high temperature furnace where bonding is completed at >1000°C. Anodic bonding relies on the formation of an oxide grown on silicon at the interface with Pyrex glass. A high voltage is applied to the wafer, which causes the alkali metal ions in the Pyrex to migrate to the cathode. An oxide is formed at the silicon interface from the applied field if oxygen is present at about 300°C. Two silicon wafers can also be joined by this technique if Pyrex is sputter deposited on one of the wafers. Pyrex is used because its coefficient of thermal expansion (CTE) matches silicon. Frit glass bonding uses a screened film of low melting temperature glass to seal two wafers directly. Glasses with CTE matched to silicon and with melting points below 600°C are commercially available. In solder bonding the solder pre-forms or pastes can be applied to either wafer surface. Some solders need fluxes to create wetting. When the wafers are heating to the solder melting point, solder dams may be necessary to prevent flow into unwanted regions. Solder bonding can serve both an electrical function, as well as to attach other die to the package. Adhesive sealing is similar to solder bonding, but either conductive or non-conductive material can be used. Adhesives do not make hermetic seals, but can be water resistant.

Several of these microfabrication technologies have been incorporated into the fabrication of a planar-fabricated micro-battery for potential nano-satellite applications. A schematic diagram of the planar micro-battery is shown in Figure 3. A set of 4 Si wafers is used to form the structure. The two exterior wafers or Si frames are used to enclose the anode and cathode while providing support for the circuitry. On one Si frame wafer, power management circuitry is either pre-fabricated on the wafer or attached as hybrid circuits to the wafer using the DRIE process to precisely locate the die. The other exterior Si frame wafer can be used to support photovoltaic cells that can be used to power the device. Through-wafer

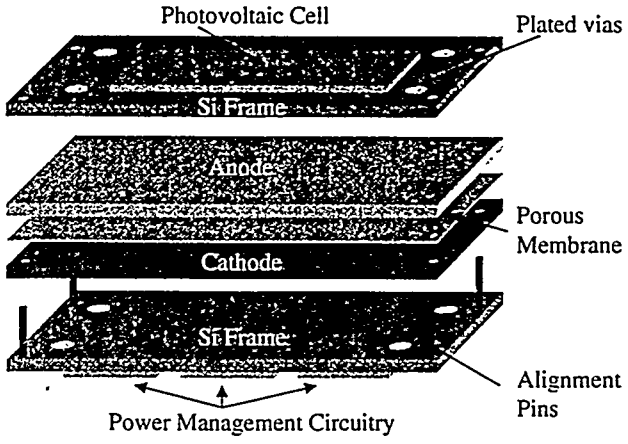
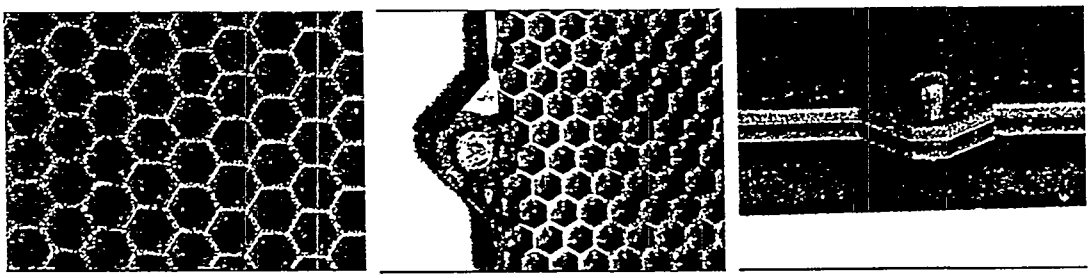


Figure 3. Schematic diagram of a micro-battery .

plated vias are used to provide electrical contact from the Si frame to the anode and cathode. The two interior Si wafers are patterned using DRIE in a honeycomb cell structure to store the battery material (see Figure 4a). As shown in Figure 3, a porous film is located between the anode and cathode wafers to prevent contact of the anode and cathode material and allow the flow of the electrolyte material between electrodes. The four wafers are accurately aligned using through-wafer via holes and alignment pins. Stainless steel alignment pins were press-fit into the lower frame wafer and used to align the upper wafers. Alignment of one Si frame wafer, the anode wafer, the porous membrane thin film, and the cathode wafer are shown in Figures 4b and c. Anodic bonding will be used to form a hermetically sealed structure. In summary, a power system using micro-fabrication technologies may be tailored to provide a self-contained, multi-functional structure that may be of use to the nano-satellite community.



2 mm (a) 2 mm (b) 2 mm (c)

Figure 4. SEM micrograph of a) honeycomb structure etched into Si ~ 400 μm deep using the DRIE process, b) top, and c) side view of 3 wafer Si battery aligned using a press-fit alignment pin.

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References

[1] Patent No. 5501893: Method of Anisotropically Etching Silicon. Inventors: Franz Laermer, and Andrea Schilp of Robert Bosch GmbH. Issued March 26, 1996.