Silicon Micromachined D-Band Diplexer Using Releasable Filling Structure Technique

Xinghai Zhao, *Graduate Student Member, IEEE*, Oleksandr Glubokov, *Member, IEEE*, James Campion, *Graduate Student Member, IEEE*, Adrian Gomez-Torrent, *Graduate Student Member, IEEE*, Aleksandr Krivovitca, Umer Shah, *Member, IEEE*, and Joachim Oberhammer, *Senior Member, IEEE*

***Abstract*— A D-band waveguide diplexer, implemented by silicon micromachining using releasable filling structure (RFS) technique to obtain high-precision geometries, is presented here for the first time. Prototype devices using this RFS technique are compared with devices using the conventional microfabrication process. The RFS technique allows etching large waveguide structures with nearly 90° sidewall angles for the 400-μm-tall waveguides. The diplexer consists of two direct-coupled cavity six-pole bandpass filters, with the lower and the upper band at 130–134 and 141–148.5 GHz, respectively. The measured insertion loss of the two bands is 1.2 and 0.8 dB, respectively, and the measured return loss is 20 and 18 dB, respectively, across 85% of the passbands. The worst case adjacent channel rejection is better than 59 dB. The unloaded quality factors of a single cavity resonator are estimated from the measurements to reach 1400. Furthermore, for the RFS-based micromachined diplexer, an excellent agreement between measured and simulated data was observed, with a center frequency shift of only 0.8% and a bandwidth deviation of only 8%. In contrast to that, for the conventionally micromachined diplexer of this high complexity, the filter poles are not well controllable, resulting in a large center frequency shift of 3.5%, a huge bandwidth expanding of over 60%, a poor return loss of 6 and 10 dB for the lower and the upper band, respectively, and an adjacent channel rejection of only 22 dB.**

***Index Terms*— Diplexer, fabrication tolerance, high-Q resonators, microwave engineering, releasable filling structure (RFS), silicon micromachining, sub-terahertz, waveguide filter.**

I. Introduction

With increasing data rates, high-speed broadband wireless communication links are in large demand, such as 5G or beyond mobile communication, wireless local area networks (WLANs), satellite communication, or autonomous vehicles. The sub-terahertz (sub-THz) frequency spectrum offers the best possibility to reach wireless transmission rates over 100 Gb/s [1], [2], being promising for broadband fixed wireless links over short/medium ranges [3].

The D-band, comprising frequencies between 110 and 170 GHz, has a large available bandwidth to attain a higher wireless transmission data rate while offering a relatively low attenuation, even in rainy conditions, making this band suitable for short-/medium-distance backhaul gigabit communications [3]. With the W-band already commercially exploited for this application, the D-band is promising to be allocated to a fixed wireless system within the next decade [4]. A system demonstration with a data rate of up to 48 Gb/s has been reported [5], and higher data rate in this band is expected and investigated [6], [7]. Combining microwave-photonics millimeter-wave frequency generation, an ultrabroadband D-band wireless signal delivery system with over 100-Gb/s wireless transmission capacity has been demonstrated experimentally [1]. All these efforts are aiming to facilitate the deployment of fixed services links in this frequency range.

Filters and diplexers are important elements in frequency-multiplexed telecommunication transceiver front ends, where Rx and Tx circuits are using the same antenna port to complete channel selection and isolation is facilitated by the diplexer [8]. For sub-THz systems, rectangular waveguides are the best choice of transmission media and for microwave components of larger electrical dimensions. Silicon micromachined waveguides were demonstrated with very low losses, for instance 0.02 dB/mm in the 220–330-GHz band [9]. The authors have already proposed a sub-THz micromachined integration platform for telecommunication links [10] with integrated SiGe microwave monolithic integrated circuits (MMICs), but no filtering function has been shown in this technology platform yet. Frequency diplexers fulfilling their specifications in terms of insertion loss (IL), in-band flatness, selectivity, and rejection are one of the most challenging components to fabricate in the THz frequency range due to the stringent requirements on the accuracy of the geometrical features, which, for higher complexity filters, requires high precision in micro level even at the relatively low D-band frequencies. In addition to the geometrical accuracy, the very low loss of micromachined waveguides and cavities offers high-Q resonators and, thus, low ILs.

Manuscript received February 29, 2020; revised May 9, 2020; accepted May 13, 2020. Date of publication July 3, 2020; date of current version August 5, 2020. This work was supported in part by the European Research Council (ERC) through the European Union's Horizon 2020 Research and Innovation Program under Grant 616846, in part by the Swedish Foundation for Strategic Research Synergy Grant Electronics SE13-007, and in part by the European Union's Horizon 2020 Research and Innovation Programme under Grant 644039 (M3TERA). *(Corresponding author: Xinghai Zhao.)*

The authors are with the Division of Micro and Nanosystems, KTH Royal Institute of Technology, SE-100 44 Stockholm, Sweden (e-mail: xinghai@kth.se).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2020.3004585

TABLE I
PERFORMANCES OF DIPLEXERS ABOVE 100 GHZ, FABRICATED IN DIFFERENT FABRICATION TECHNOLOGIES

Ref.	f_0* (GHz)	Δf_0* (GHz)	BW* (%)	ΔBW* (%)	IL* (dB)	RL* (dB)	AR* (dB)	Technology
[11]	265/300	8**/5**	7.5**/6.7**	N/A	7.6/8	10/13.4	N/A	SU-8
[12]	323/335**	N/A	2/5**	N/A	3/3	N/A	N/A	Photonic-Crystal
[13]	324/442	N/A	30/26	N/A	2-3.8/1.5-2.5	15/15	35	Milling
[14]	190/220	3/3	2.1/2.7	25**/33**	1.5/1.5	10/10	N/A	CNC
This work	132/145	1/1.4	3/5.1	7.5/8	1.2/0.8	20/18	59	DRIE

*f_0 – center frequencies of diplexers' lower and upper passband, Δf_0 – lower/upper passband's shift of measured bandwidth as compared to the simulated, BW – lower/upper passband's bandwidth, ΔBW – lower/upper bandwidth's relative change of measured bandwidth as compared to the simulated, IL- lower/upper passband's insertion loss, RL–lower/upper passband's return loss, AR–adjacent channel rejection.
**Estimated values – estimated from figures, as no explicit numbers given.

At D-band frequencies, very few examples of waveguide components, including filters and diplexers, have been demonstrated so far. In [15], the first D-band waveguide filter based on deep reactive ion etching (DRIE) technology was reported with the lowest IL of 0.45 dB in passband, although for a 15% (three-pole) or 11.5% (five-pole) fractional bandwidth, the unloaded quality factor Q_u of the fabricated filter was estimated to reach 163 (five-pole), and the return losses were not characterized, which demonstrates to some extent the huge potential capability of DRIE to fabricate sub-THz frequency waveguide devices. A micromachined waveguide filter based on ultralow-loss silicon waveguide technology has been presented recently by Campion *et al.* [16] with an average IL in the passband of only 0.5 dB for a designed fractional bandwidth of 5.2%, and Q_u of a single cavity resonator is expected to reach 1600, but the fabricated filter had a center frequency shift by 4.75 GHz and a bandwidth increase by 61.5% due to fabrication inaccuracies.

Diplexers are very complex filtering structures, and their fabrication remains challenging at sub-THz frequencies. At frequencies above 100 GHz, only very few diplexers are reported. A WR-3 (220-325 GHz) waveguide diplexer based on SU-8 technology was presented in [11], which had a high IL, a significant center frequency shift and a bandwidth shrinking. In [12], a photonic-crystal diplexer with about 3-dB IL was reported. A milled 275–500-GHz ultrawideband frequency splitter based on two couplers and individual high- and low-pass filters had an IL of 1.5–3.8 dB [13] and an adjacent channel rejection of 35 dB, requiring feature sizes for which 30-μm-diameter milling tools had to be used. A CNC-milled G-band (170–260 GHz) diplexer reported with an IL of only 1.5 dB, but the center frequencies of its passbands shifted downward by 3 GHz and the bandwidths expanded by 30% due to fabrication errors [14]. A comparison of previous diplexer works is summarized in Table I.

In this work, the first D-band waveguide diplexer to date is presented, which is implemented by silicon micromachining. Also, a releasable filling structure (RFS)-based microfabrication process is presented for the first time, which enables accurate fabrication. An RFS-based microfabricated prototype is implemented and compared experimentally to a conventionally microfabricated diplexer, and the influence of fabrication tolerances on filter performance is investigated, proving the advantages of this process which even allow for scaling such high-complexity diplexers higher up to THz frequencies.

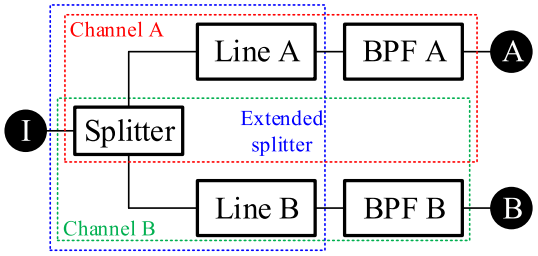


Fig. 1. Functional diagram of the diplexer with input I and outputs A and B. Highlighted parts, namely the extended splitter, channels A and B are used to simplify the description of the design procedure. Blocks "Line" and "BPF" represent waveguide sections and bandpass filters for channels A and B, respectively.

II. DIPLEXER AND CHANNEL FILTERS DESIGN

This section explains the procedure to design a diplexer with a frequency response, which fulfills the following design specifications worked out for a D-band communication link in the European Commission-funded M3TERA project [17].

1) *Channel A Passband:* $f_{\min A} \ldots f_{\max A} = 130 \ldots 134$ GHz.
2) *Channel B Passband:* $f_{\min B} \ldots f_{\max B} = 141 \ldots 148.5$ GHz.
3) *Maximum Return Loss in Passbands:* RL = 20 dB.
4) *Adjacent Channel Rejection:* AR = 65 dB.

Fig. 1 shows a functional diagram of the designed diplexer. The diplexer consists of two channel filters connected through a splitter with waveguide sections attached to its outputs, which acts as a nonresonating star junction. Synthesis and design techniques for diplexers/multiplexers with star junctions are described in detail in [18]–[20]. It has been determined that the specifications can be satisfied by the sixth-order all-pole filters for each channel; the corresponding coupling scheme is shown in Fig. 2. The final layout of the diplexer, containing two chips with dimensions, is shown in Fig. 3. The algorithm we utilized for finding the final design parameters is outlined as follows.

For the diplexer design, a hybrid multifidelity optimization approach was used [21]–[23], which allows avoiding

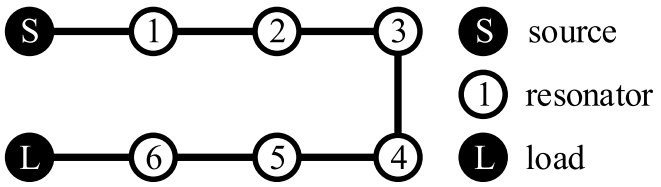


Fig. 2. Coupling scheme of each individual channel filter.

computationally expensive optimization of the full structure with many design variables. Instead, each of the channel filters and the splitter with the attached waveguide sections are optimized separately while being connected to the entire circuit.

The algorithm exploits several models of various parts of the diplexer, as shown in Fig. 1. The responses of low-fidelity (or coarse) models of all the blocks are denoted as $\boldsymbol{R}^c(\boldsymbol{x})$ and the responses of high-fidelity (or fine) models are denoted as $\boldsymbol{R}^f(\boldsymbol{x})$, where $\boldsymbol{x}$ is a vector of design parameters corresponding to the block evaluated in their coarse and fine models, respectively. The coarse models are composed of cascaded waveguide sections and irises represented as analytical models and evaluated in MATLAB. In contrast, the fine models use full-wave simulations in CST Studio Suite with a dense mesh.

In order to simplify the evaluation of the coarse models, a fine response surface model of the splitter was created, which depends on a single design parameter: $\boldsymbol{R}_S^f(L_p)$. Taking this into account, all the models of diplexer's parts containing the splitter cascaded with other blocks represented as coarse models are denoted as hybrid models with responses $\boldsymbol{R}^h(\boldsymbol{x})$.

The design algorithm operates with the following set of models.

1) *Response Surface Fine Model of the Splitter:* $\boldsymbol{R}_S^f(L_p)$.
2) *Hybrid and Fine Models of the Extended Splitter:* $\boldsymbol{R}_{\mathrm{ES}}^h(L_p, L_A, L_B)$ and $\boldsymbol{R}_{\mathrm{ES}}^f(L_p, L_A, L_B)$.
3) *Coarse and Fine Models of the Both Bandpass Filters:* $\boldsymbol{R}_{\mathrm{BPFA}}^c(\boldsymbol{L}_{Ak}, \boldsymbol{W}_{An,n+1})$, $\boldsymbol{R}_{\mathrm{BPFB}}^c(\boldsymbol{L}_{Bk}, \boldsymbol{W}_{Bn,n+1})$, $\boldsymbol{R}_{\mathrm{BPFA}}^f(\boldsymbol{L}_{Ak}, \boldsymbol{W}_{An,n+1})$, and $\boldsymbol{R}_{\mathrm{BPFB}}^f(\boldsymbol{L}_{Bk}, \boldsymbol{W}_{Bn,n+1})$, where $k = 1 \ldots 6$ and $n = 0 \ldots 6$.
4) *Hybrid and Fine Models of the Channels:* $\boldsymbol{R}_{\mathrm{Ch}A}^h(\boldsymbol{x})$, $\boldsymbol{R}_{\mathrm{Ch}B}^h(\boldsymbol{x})$, $\boldsymbol{R}_{\mathrm{Ch}A}^f(\boldsymbol{x})$, and $\boldsymbol{R}_{\mathrm{Ch}B}^f(\boldsymbol{x})$.

The design algorithm contains the following steps.

Step 1: Design a response surface model of the splitter $\boldsymbol{R}_S^f(L_p)$.

Step 2: Design and optimize both filters using coarse models $\boldsymbol{R}_{\mathrm{BPFA}}^c(\boldsymbol{L}_{Ak}, \boldsymbol{W}_{An,n+1})$ and $\boldsymbol{R}_{\mathrm{BPFB}}^c(\boldsymbol{L}_{Bk}, \boldsymbol{W}_{Bn,n+1})$.

Step 3: Find L_p, L_A, and L_B by optimizing hybrid model $\boldsymbol{R}_{\mathrm{ES}}^h(L_p, L_A, L_B)$ with respect to design specifications with attached channel filters.

Step 4: Optimize $\boldsymbol{R}_{\mathrm{Ch}A}^h(\boldsymbol{x})$ by varying design parameters of and BPF A only.

Step 5: Optimize $\boldsymbol{R}_{\mathrm{Ch}B}^h(\boldsymbol{x})$ by varying design parameters of and BPF B only.

Step 6: If the specifications are satisfied, go to 7. If not, go back to 3.

Step 7: Adjust L_A and L_B to match responses of extended splitters in coarse and fine models by aggressive space mapping (ASM): $[L_A, L_B] = \arg\{\min||\boldsymbol{R}_{\mathrm{ES}}^f(L_p, L_A, L_B) - \boldsymbol{R}_{\mathrm{ES}}^h(L_p, L_A, L_B)||\}$.

Step 8: Find design parameters $\boldsymbol{L}_{Ak}$ and $\boldsymbol{W}_{An,n+1}$ of BPF A by minimizing $||\boldsymbol{R}_{\mathrm{BPFA}}^f(L_{Ak}, \boldsymbol{W}_{An,n+1}) - \boldsymbol{R}_{\mathrm{BPFA}}^c(L_{Ak}, \boldsymbol{W}_{An,n+1})||$ through ASM.

Step 9: Find design parameters $\boldsymbol{L}_{Bk}$ and $\boldsymbol{W}_{Bn,n+1}$ of BPF B by minimizing $||\boldsymbol{R}_{\mathrm{BPFB}}^f(L_{Bk}, \boldsymbol{W}_{Bn,n+1}) - \boldsymbol{R}_{\mathrm{BPFB}}^c(L_{Bk}, \boldsymbol{W}_{Bn,n+1})||$ through ASM.

Step 10: Fine-tune channel filters of the diplexer, repeating steps 4 and 5 for the fine models $\boldsymbol{R}_{\mathrm{Ch}A}^f(\boldsymbol{x})$ and $\boldsymbol{R}_{\mathrm{Ch}B}^f(\boldsymbol{x})$.

The presented algorithm can be used for designing diplexers of the same configuration with various specifications, i.e., the parameters of the passbands can be adjusted. Moreover, the procedure can be generalized to enable designs with various filter orders in each passband. The final dimensions of the diplexer designed by the procedure listed earlier are presented in Table II.

TABLE II
FINAL DIMENSIONS OF THE PRESENTED DIPLEXER

Dimension	Value, μm	Dimension	Value, μm	Dimension	Value, μm
L_p	204	L_{B2}	1134	W_{A56}	606
L_A	990	L_{B3}	1176	W_{A67}	896
L_B	960	L_{B4}	1177	W_{B01}	957
L_{A1}	1240	L_{B5}	1153	W_{B12}	698
L_{A2}	1420	L_{B6}	1005	W_{B23}	587
L_{A3}	1434	W_{A01}	920	W_{B34}	570
L_{A4}	1432	W_{A12}	600	W_{B45}	576
L_{A5}	1412	W_{A23}	548	W_{B56}	632
L_{A6}	1251	W_{A34}	541	W_{B67}	892
L_{B1}	945	W_{A45}	550	W_{wg}	1651

III. Effects of Fabrication Tolerances on Filter Performance

The absence of a high-efficiency, low-cost and high-accuracy fabrication method limits the implementation of complex waveguide filters, in particular multiport components, at frequencies over 100 GHz. DRIE is the most promising micromachining technique to fabricate high-aspect-ratio and high-precision silicon structures to date [32]–[34]. However, at some sub-THz frequencies, where the cross section of rectangular waveguides ranges from 0.254×0.127 mm^2 (WR-1) to 2.032×1.016 mm^2 (WR-8), it has been always challenging to use DRIE to realize high-quality sidewalls, especially when etching superdeep (larger than 300 μm) and large-opening (wider than 500 μm) trenches [35], [36]. DRIE is an inherently geometry-dependent technology: different underetching for different cavities and feature sizes, as well as etching depths, seriously affects etching accuracy and verticality of the sidewalls [37], [38]. At submillimeter/THz frequencies, very high-precision machining is required for the device fabrication [36], [39], [40]. Fabrication tolerances and sidewall slope significantly degrade the desired RF performance of the final devices [27], [28]. Many researchers suffered from these

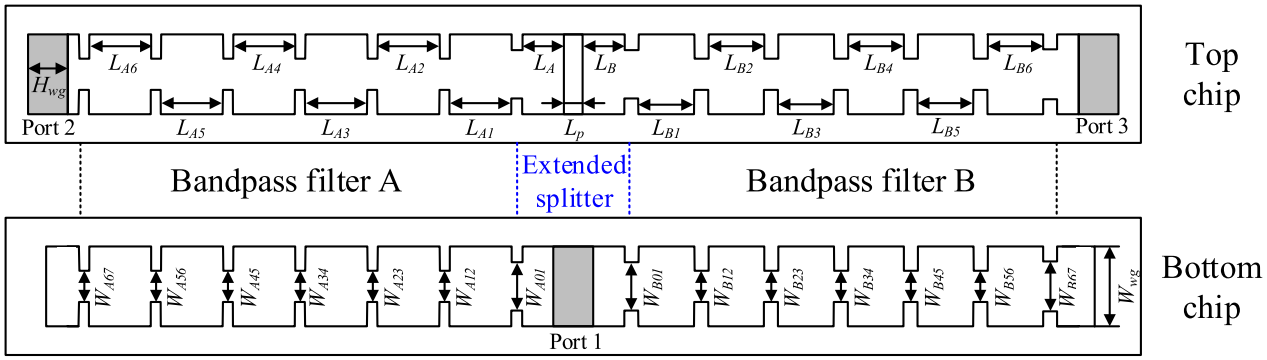


Fig. 3. Layouts of the two chips making up a complete diplexer chip with dimensions. Extended splitter containing a splitter with a perturbation and two waveguide sections, as well as two bandpass filters are highlighted for comparison with the functional diagram in Fig. 1.

TABLE III
PERFORMANCE COMPARISON OF DRIE MICROMACHINED *H*-PLANE WAVEGUIDE FILTERS ABOVE 100 GHZ

Ref.	f_0 GHz	Δf_0 GHz	BW %	ΔBW %	IL dB	Q_u †	RL dB	Etch depth μm	Sidewall angle deg	GT + μm
[15]	140	~2	11.5	13	≥0.6	~720	N/A	825	~0.5	10
[16]	145	4.75	5.2	57.3	~0.5	1270	20	400	4.2	7
[24]	170	~4	9.2	39	≥1.5	~580	15	648	~1	20
[25]	380	5	2.6	52	≥2.7	~190	~8	280	1.65	8
[26]	570	N/A	8.8	N/A	0.9	350	~8	190	2	N/A
[27]	550	10	6	N/A	2.5	330	~10	200	3	2
[28]	1000	18	11.7	12	2.5	150	~15	130	0.5	2
[29]	400	5	8.05	6.6	2.8	95	~16	280	1.46	5
[30] *	300	2	2.5	5	1.65	900	15	400	3.8	N/A
This work	132	1.1	3	5	1.25	1360	20	400	<1	3
This work	145	1.3	5.2	7.7	0.65	1490	20	400	<1	3

† Estimated unloaded quality factor extracted from measured data for a single cavity resonator assuming all resonators have equal performance [31]
* Fabrication errors where predicted and compensated in the design

problems [16], [32], [41]–[43] and started to be aware of the gravity of these problems [42], [44].

Table III summarizes the key performance metrics of typical reported rectangular waveguide filters based on the DRIE technique at frequencies above 100 GHz. Although these show that DRIE is capable of achieving good etching results by using an optimized fabrication process, different processes and different geometries have different sidewall angles ranging from 0.5° to 4.2° and geometrical tolerance (GT) varying from 2 to 20 μm, which resulted in very large fluctuation on the RF performances. DRIE is a very demanding process, which usually requires significant optimization of its etching parameters in order to obtain the desired etching quality.

Furthermore, for complex filter designs, the center frequency and bandwidth are highly sensitive to the verticality of sidewalls, which mainly determines the actual size and shape of the resonating cavities. In our work, using the RFS-based method, less than 1° tilting angles for all the sidewalls have been achieved without any extra laborious optimization of the DRIE process.

In this article, we introduce the critical dimension (CD) loss and sidewall angle to quantify the fabrication tolerances. Fig. 4 shows the definitions of CD-loss Δd and sidewall angle θ

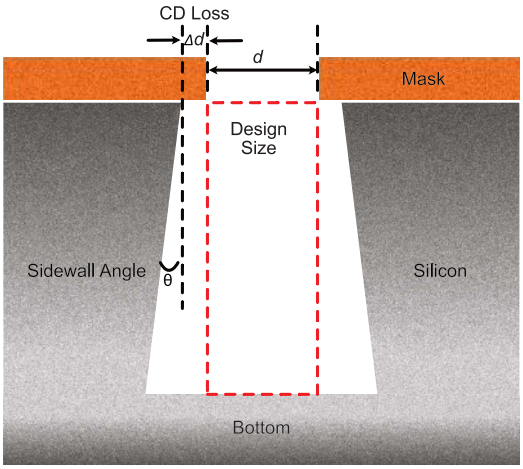


Fig. 4. Schematic cross section of an etched silicon trench.

in these simulations. The feature shape is quantified through CD-loss Δd, the mismatch between the mask layout and the actual silicon dimension, and the sidewall angle θ, the angle between the feature sidewall and the etching direction. The sidewall angle θ is positive when the sidewalls are reentrant

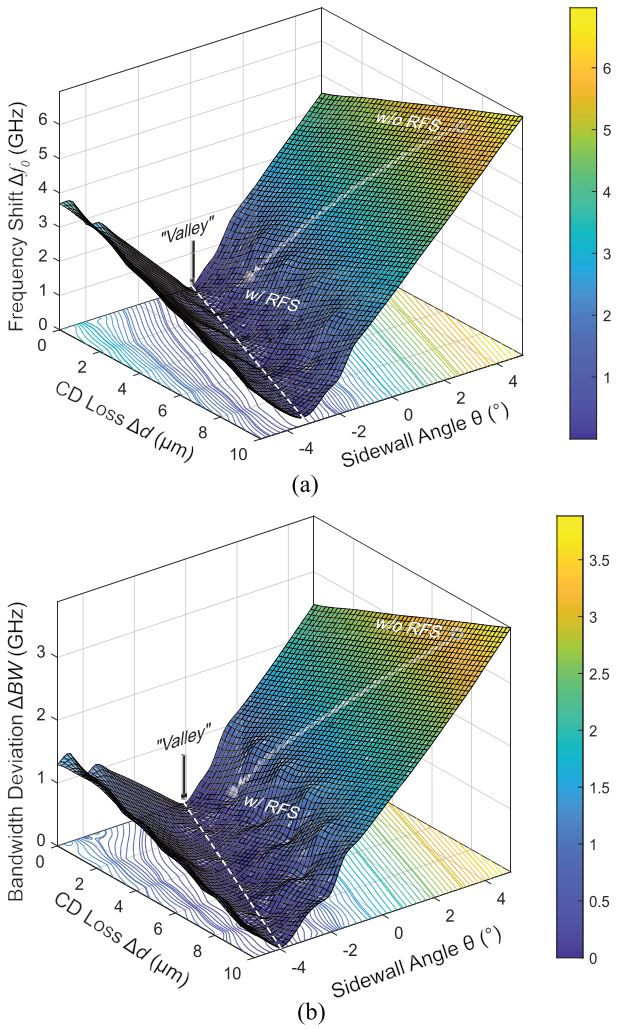


Fig. 5. Simulation results on (a) center frequency shift Δf_0 and (b) bandwidth deviation ΔBW as a function of CD-loss Δd and sidewall angle θ. The circle maker denotes the conventional microfabrication process without RFS (w/o RFS), whereas the sphere maker denotes the RFS-based filter (w/ RFS).

(upper opening is smaller than the bottom opening) and negative when the sidewalls are tapered (upper opening is larger than the bottom opening).

In order to figure out the detailed effects of fabrication tolerances on filter performance, an analysis has been carried out based on electromagnetic (EM) simulation. Sidewall angle θ ranging from $-5°$ to $5°$ and CD-loss Δd ranging from 0 to 10 μm are used in simulation and act as independent variables, which are typical fabrication inaccuracy values due to fabrication tolerances. Center frequency shift Δf_0 or bandwidth deviation ΔBW is the dependent variable here. The maximum point in both cases [see Fig. 5(a) and (b)] appears at the coordinate position of $5°$ of the sidewall angle θ and 10 μm of CD-loss Δd, which represents the maximum geometric deformation to the resonating cavities as well. Obviously, we can suppress the undesired Δf_0 or ΔBW by decreasing the fabrication tolerances in terms of the sidewall angles and CD-losses as small as possible to obtain the designed structures. Furthermore, multiple zeros or approximate zeros of Δf_0 or ΔBW show up in specific positions besides (0, 0) point in the coordinate system, which bring us more opportunities to suppress the undesired Δf_0 or ΔBW. Therefore, another possible approach can be to counteract Δf_0 or ΔBW by selecting the proper combination of the tapered sidewall angle and the CD-loss, which needs to adjust the design parameters to the processing parameters. In Fig. 5, the noticeable "valley" in the plot represents the lowest contour line where Δf_0 or ΔBW is approximately equal to zero due to the counteraction between the tapered sidewall effect and the CD-loss effect on frequency shift or bandwidth deviation. In other word, we can get better desired center frequency and bandwidth if the locations that are decided by sidewall angle and CD-loss together are closer to the "valley." Thus, this mechanism provides an alternative solution to suppress the frequency shift and bandwidth deviation in the practical fabrication by tuning the sidewall angle and CD-loss. A simplified alternative has been preliminarily investigated in our previous work [30], [42]. To maintain the specified center frequency, the sidewall angle was predicted and considered in the designs, which shows a certain impact on compensation of frequency shift. Since the sidewall slope varies with the size of the single cavity, the fabrication variations of different runs, and the predicted errors, this method is of limited use.

IV. Fabrication and Assembly

A. Fabrication

The Bosch DRIE process alternates between etching and sidewall passivation steps [45]. The commonly used etching gas is SF_6 and the passivation gas is C_4F_8 or CHF_3. The process can be characterized by many parameters, such as etch rate, sidewall "scallop" size, etch anisotropy (sidewall verticality), etch uniformity, undercut, loading effects, RIE-lag, micrograss, and notching, all of which have been found and proved to be trench width or aspect ratio-dependent directly or indirectly [45]–[47]. Therefore, some of the toughest problems, such as etch anisotropy, underetching, and RIE-lag, can be tempered simultaneously by introducing RFS technology to control the trench width or etch area. After the features are etched, the RFSs are completely released from the cavities.

Prototype devices are fabricated separately by the conventional microfabrication process [see Fig. 6A(a)–(d)] and the RFS-based microfabrication process [see Fig. 6B(a)–(f)] on silicon-on-insulator (SOI) wafers. SOI wafers consist of a device layer (DL) of 100 μm, a handle layer (HL) of 400 μm, and a buried oxide layer (BOX) of 1 μm.

To achieve a high height (800 μm) of the waveguide for minimizing losses while avoiding excessively deep etches, the waveguide height is split into two pieces in the H-plane to be etched separately [see Fig. 7(a)], and then, the two halves are bonded together to form a complete, full-height rectangular waveguide for both methods [see Fig. 7(b)].

In the RFS-based microfabrication process, the RFSs are employed in the large etching areas for waveguide resonating cavities to improve the sidewall verticality. The process flow and scanning electron microscope (SEM) pictures are shown in Figs. 6B(a)–(f) and 8, respectively. Both sides (DL and HL) of the SOI wafer are thermally oxidized by 2-μm silicon

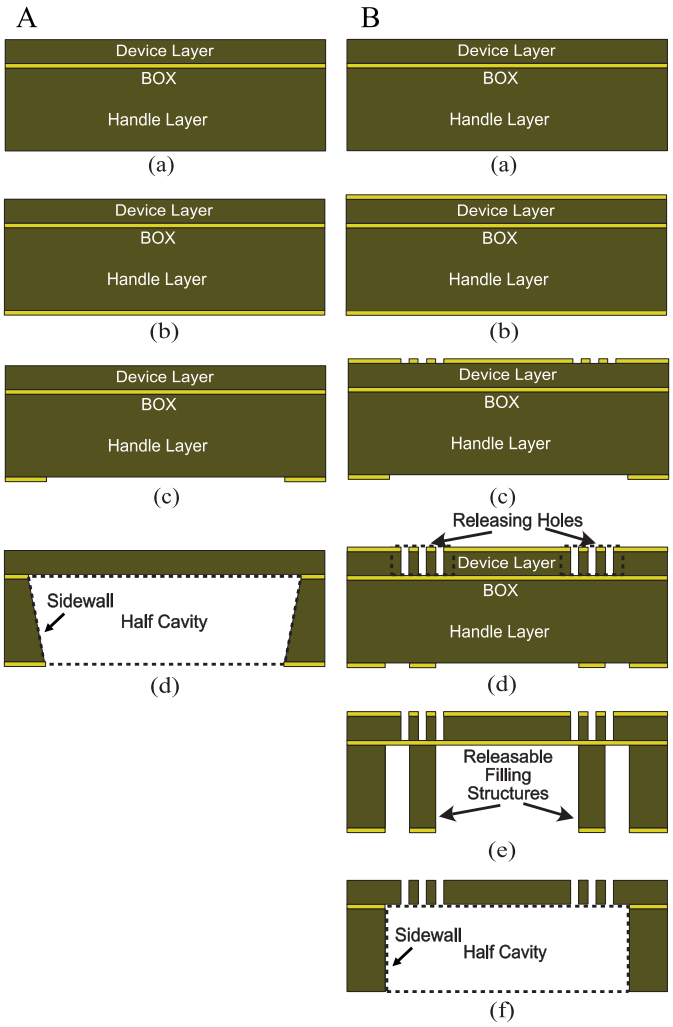


Fig. 6. Schematic of key steps for conventional microfabrication process (A) and RFS-based microfabrication process (B). (a) SOI wafer preparation. (b) SiO_2 thermal deposition. (c) Patterning for hard masks. (d) and (e) DRIE of the DL and HL. (e) Release of filling structures. (f) Two H-plane-split chips after DRIE.

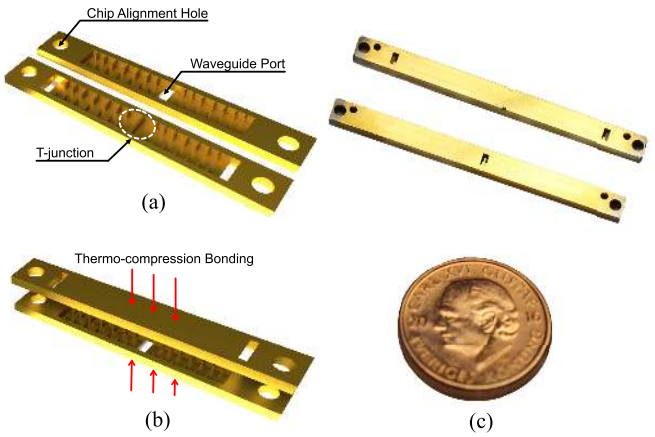


Fig. 7. Diplexer after DRIE etching. (a) Two H-plane-split chips after DRIE. (b) Thermocompression bonding of two split chips. (c) Photograph of fabricated diplexers.

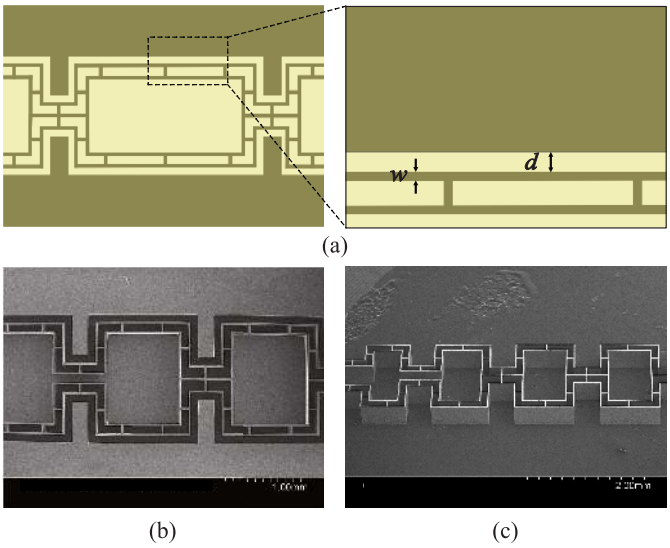


Fig. 8. Waveguide with RFSs. (a) Layout of the RFS. (b) SEM image of the waveguide with RFS. (c) SEM image of released RFS.

oxide (SiO_2) and then patterned by photoresist, and RIE etching is used to etch SiO_2 to form the hard masks for the subsequent DRIE silicon etching. The HL is etched by the standard Bosch process to obtain the waveguide cavities with irises and transitions from the diplexer to the ports. Both etching processes stop at the interface with the BOX layer, so the etching depth is accurately controlled. Therefore, the complete waveguide with a total height of 800 μm can be obtained by bonding two wafers with the HLs facing each other. A photograph of two completed diplexer prototypes is shown in Fig. 7(c). The RFS technique enables all the trenches surrounding the sidewalls of the waveguide cavities and irises to be of an uniform and well-controlled 100-μm width d, with a grid width w of 25 μm, as shown in Fig. 8(a). This results in a very uniform, geometry-independent etching of the waveguide cavities.

For the conventional process (see Fig. 6A), a 300-μm underetching [see Fig. 9(a)] corresponding to a 4° sidewall angle was induced for the 400-μm deep etching. A significant sidewall slope in the iris window is observed in Fig. 9(a) and (b). In contrast, Fig. 9(c) shows a nearly 90° vertical sidewall for the proposed RFS-based process. Moreover, the shapes and dimensions of the irises are well retained, as shown in Fig. 9(d). The CD-losses of irises with RFS are only 2–4 μm comparing to 7–9 μm without them. It is clear from Fig. 9 that the RFS-based process can significantly improve the etching quality. After the DRIE step, the RFSs are released by hydrofluoric (HF) acid etching of the BOX layer. Etching holes in the DL allow the HF solution to reach specific areas on the BOX layer where the etching should be performed. The etching holes are designed to be 10 μm × 10 μm squares with a pitch of 6 μm (see Fig. 10), which are small enough (210 times smaller than the wavelength) to avoid unnecessary radiation losses. After HF releasing, the entire filling structure [see Fig. 8(b) and (c)] can automatically fall out of the cavity without any residues.

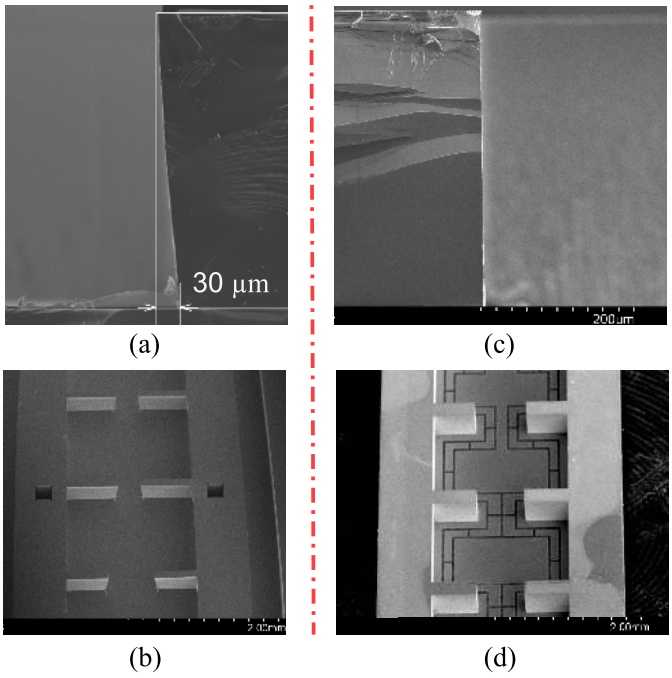


Fig. 9. Visual comparison of DRIE processes for (a) sidewall of waveguide and (b) irises inside waveguide without using RFSs to (c) sidewall and (d) irises with using RFSs.

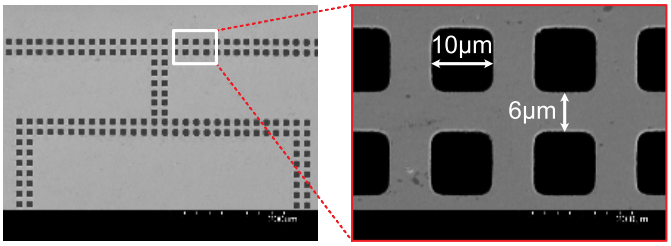


Fig. 10. SEM images of etch holes on DL of the diplexer for the RFS geometries.

Subsequently, the chips are metallized by sputtering a 2-μm gold layer on HL and a 1-μm gold layer on DL, both using a 50-nm-thick titanium–tungsten (TiW) adhesion layer.

Although the RFS-based process mainly adds a few additional steps to the manufacturing process, it has the advantages of higher fabrication accuracy and reproducibility, independent of the etched structures, and thus requires neither geometry-dependent process optimization nor geometrical corrections for designs with varying feature sizes.

B. Assembly

After the metallization, these two half chips are aligned manually under a microscope. The alignment is facilitated via alignment holes [see Fig. 7(a)] and Vernier scales (see Fig. 11) in each piece. The final average alignment accuracy was found to be 2–4 μm in any direction. The assembled waveguide halves are then bonded together [see Fig. 7(b)] by using the thermocompression bonding process [9], [10], [42], [44]. No differences in the mechanical stability when bonding structures with or without RFS could be observed. The overall

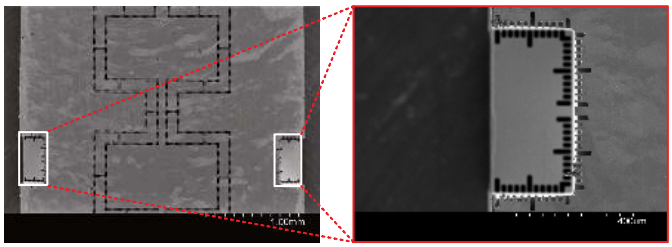


Fig. 11. SEM images of Vernier scales on the chip used for accurate chip-to-chip alignment.

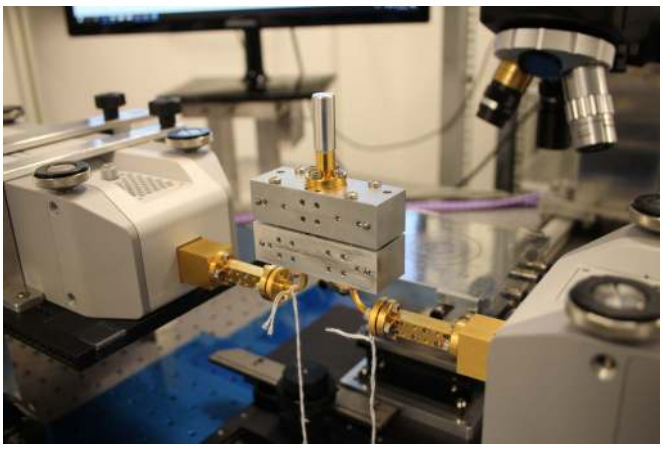


Fig. 12. Setup for measurement of the three-port diplexer. Two ports are fed by ZVA-Z170 frequency extenders, whereas the remaining port is terminated with a waveguide load.

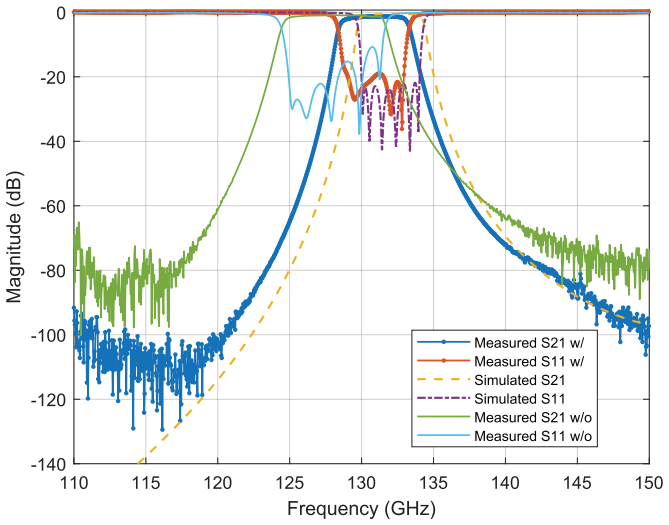
mechanical stability during bonding is ensured by the thick DL (100 μm) and wide irises (200 μm).

V. Measurement Results and Discussion

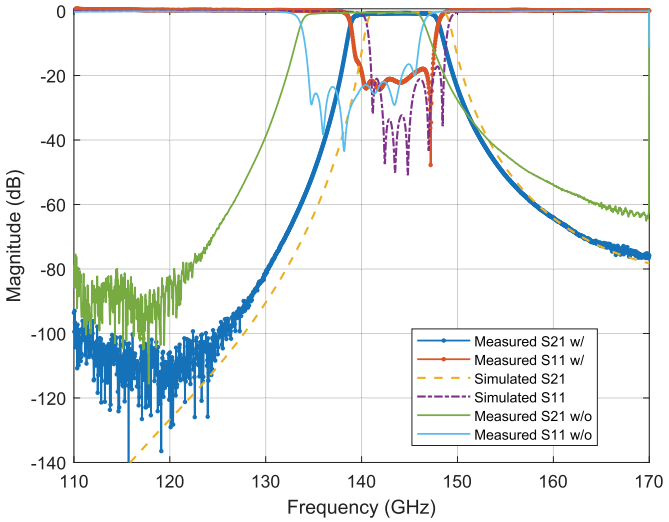
Characterization of the fabricated filters and diplexers is implemented using Rohde & Schwarz ZVA-Z170 frequency extenders driven by a ZVA-24 VNA. The measurement setup uses a metal split block as in [16]. For the diplexers with three ports, the characterization is more complex, the complete details of which are out of the scope of this article. The reference planes for measurement of the two-port filters are shifted to 500 μm away from the first iris using an on-chip line–reflect–line calibration kit [9]. An elliptical alignment hole method is employed to improve the alignment accuracy between waveguide ports on the chips and on the measurement setup [48]. For measurement of the diplexers, the measurement setup is shown in Fig. 12, and the reference plane at all three ports is shifted to the outer surface of the chip (i.e., the effect of the split blocks and feeding waveguides is removed) via a series of one- and two-port calibrations. As only two frequency extenders are available, the diplexer was measured in three different configurations, in which the remaining port was terminated with a waveguide load. Complete three-port S-parameters of the diplexer were then reconstructed following deembedding of the split blocks and feed waveguides.

A. Channel Filters

In order to characterize the processing effects of the RFS-based technology, initially, two all-pole iris-coupled



(a)

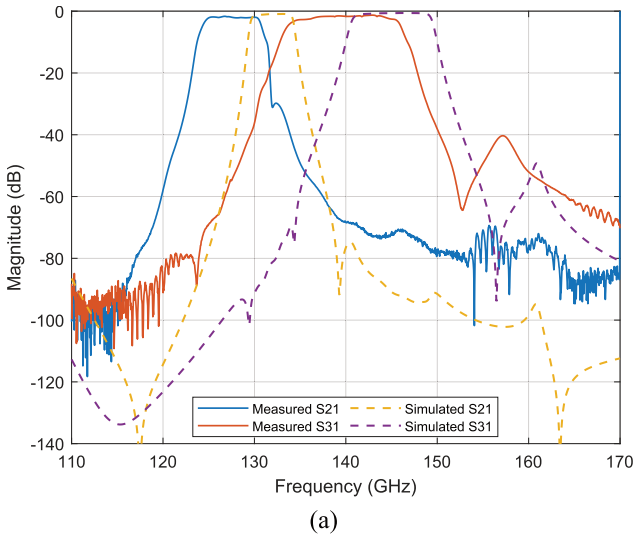


(b)

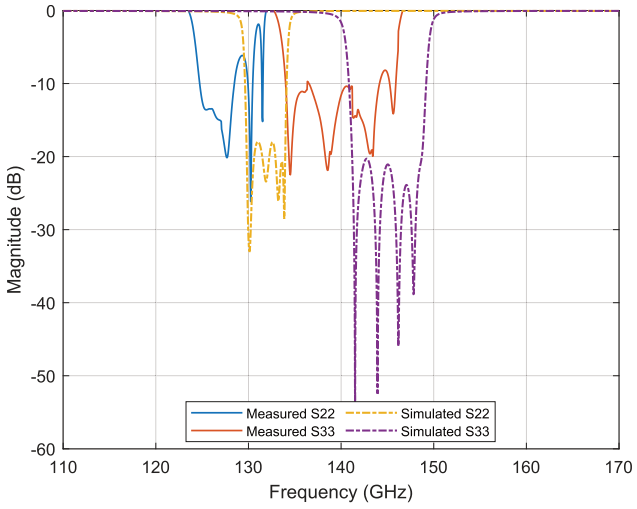
Fig. 13. Measured and simulated S-parameters of the filter with (w/) and without (w/o) RFS at (a) 132 and (b) 145 GHz.

rectangular waveguide filters with center frequencies at 132 and 145 GHz are implemented, respectively, by a conventional microfabrication process without RFS (w/o RFS) and with RFS-based microfabrication process (w/ RFS), as shown in Figs. 6 and 7.

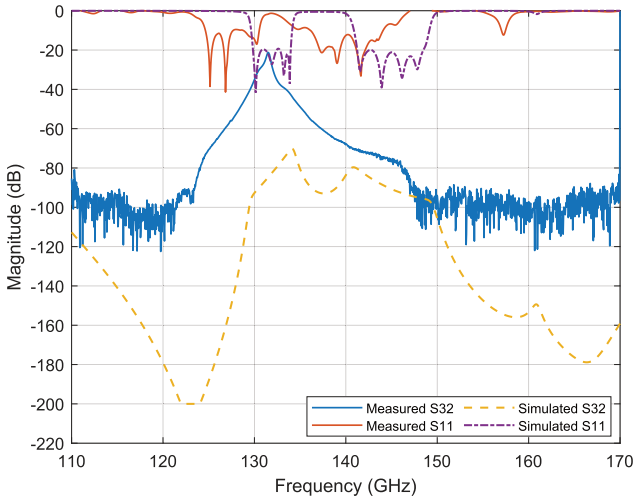
Fig. 13(a) shows that the filter with using RFS at lower band (130–134 GHz) has only Δf_0 1.1 GHz and ΔBW 5% compared with Δf_0 4 GHz and ΔBW 66% of the filter without using RFS. Fig. 13(b) shows the higher band filter at 141–148.5 GHz. The filter with using RFS has only Δf_0 1.3 GHz and a negligible ΔBW 7.7% compared with Δf_0 4.75 GHz and the ΔBW 57.3% of the filter without using RFS [16]. It is visible that the RFS-based filters have a negligible ΔBW ($<$10%) compared with the significant ΔBW more than 50% of the filters without RFS. The comparison of the S-parameters in Fig. 13 clearly demonstrates that the filters fabricated by the RFS technology have much better agreement



(a)



(b)



(c)

Fig. 14. Measured and simulated S-parameters of the diplexer without (w/o) RFS on (a) transmission losses S21 and S31, (b) reflection responses S22 and S33, and (c) reflection S11 and adjacent channel rejection S32.

with the expected results simulated by the 3-D EM simulation software CST. The main specifications of the RFS-based filters are listed in Table III to compare with other works

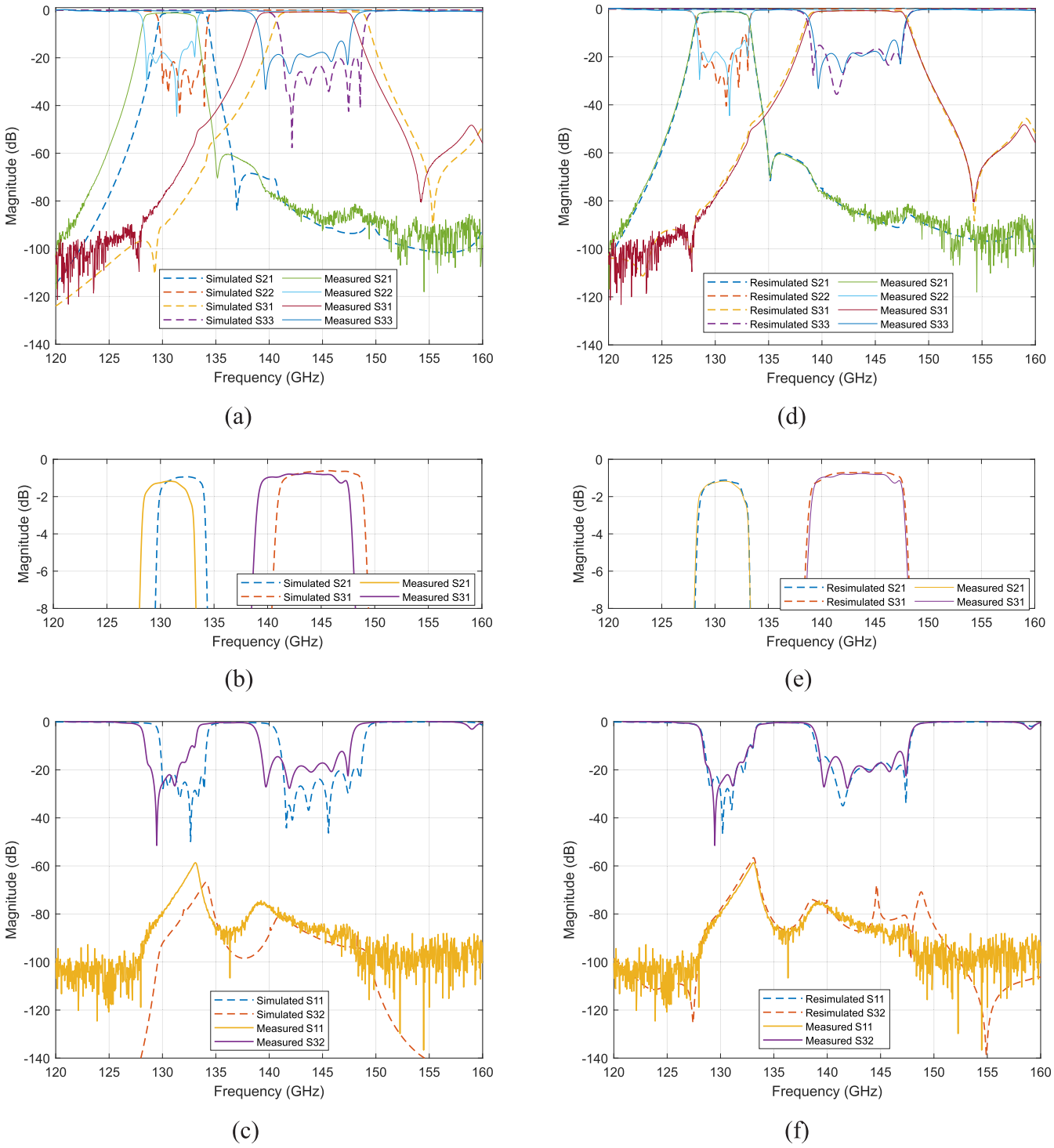


Fig. 15. Measured and simulated S-parameters of the RFS-based micromachined diplexer on (a) transmission and reflection responses of port 2 or port 3 to port 1. (b) Close-up view of S21. (c) Reflection of port 1 and adjacent channel rejection between ports 2 and 3. Also, the corresponding comparisons with (d)–(f) results of the resimulated diplexer according to the measured geometries of the fabricated one.

based on the conventional DRIE technology. Q_u of 1360 and 1490 has been achieved for these two RFS-based filters, respectively.

In addition, we assessed the center frequency shift and bandwidth deviation by applying the postprocess measured fabrication inaccuracies to the model of Section III, which is shown in Fig. 5. The sphere marker on this map approaches considerably closer to the optimum "valley" compared with the location of the circle marker, due to the proposed RFS technology. For the frequency shift Δf_0, the predicted values by the simulation model have 0.9- and 0.4-GHz difference with respect to the measured values of the filter fabricated without RFS and the filters with RFS, respectively. Similarly, for the bandwidth deviation ΔBW, the predicted values show 13% and 5% differences between the measured values of the filters without RFS and with RFS.

TABLE IV
COMPARISON OF SIMULATED AND MEASURED PERFORMANCE PARAMETERS OF THE DIPLEXERS IN THIS WORK

Parameters	Lower Band (channel A)					Upper Band (channel B)				
	Sim.	w/o	w/	Δ. w/o [+]	Δ. w/ [+]	Sim.	w/o	w/	Δ. w/o [+]	Δ. w/ [+]
IL (dB)	1.1	1.9	1.2	73 %	9 %	0.7	1.6	0.8	129 %	14 %
RL (dB)	≥24 [*]	≥6 [*]	≥20 [*]	75 %	17 %	≥20	≥10 [*]	≥18 [*]	50 %	10 %
AR (dB)	≥64	≥22	≥59	65.6 %	7.8 %	≥64	≥22	≥59	65.6 %	7.8 %
f_0 (GHz)	132	127.4	131	3.5 %	0.8 %	144.5	139.9	143.1	3.2 %	1 %
BW(GHz)	4	6.8	4.3	70 %	7.5 %	7.5	12.3	8.1	64 %	8 %
Q_u [†]	1600	570	1410	64.4 %	18.8 %	1500	400	1200	73.3 %	20 %

[*] 85% of the whole passband. [+] Δ (%) - relative change of measured value as compared to simulated

[†] Estimated unloaded quality factor for a single cavity resonator assuming all resonators are equal.

B. Diplexers

Fig. 14 shows the measured results of the diplexer fabricated by the conventional method (w/o RFS) compared with the simulated performance. The measured results demonstrate around 1.9 dB of IL, less than 10 dB of return loss, and only 20 dB of adjacent channel rejection; 5-GHz center frequency shifts Δf_0 are observed in both bands due to a large inclination of up to 4° in the vertical walls. The bandwidth expansion ΔBW reaches 70% at the lower band and 64% at the upper band. The return loss degrades to less than 10 dB due to detuning, which can be explained by the underetching and CD-loss in the areas of the coupling irises [27]. The adjacent channel rejection degraded severely following the detuning of the channels. The measured result has a nonnegligible offset with the simulation in terms of center frequency, bandwidth, and isolation. According to the analysis in Section III, the sidewall verticality of the waveguide or irises is the first factor to induce Δf_0 and ΔBW. Furthermore, H-plane waveguide devices, especially with narrow bandwidths, are very sensitive to the change of dimensions in the H-plane.

Another prototype of the diplexer is implemented by the RFS-based process (w/ RFS). Fig. 15 shows the measured performance of the diplexer compared with the simulations. The center frequency shifts Δf_0 have been suppressed to only 1–1.4 GHz and the bandwidth deviations ΔBW have been induced to 7.5% at the lower band and 8% at the upper band. Two channels have the ILs of 1.2 and 0.8 dB and the return losses of 20 and 18 dB across 85% of the passbands, respectively. The adjacent channel rejection is enhanced to be better than 59 dB. In order to complete the self-consistency analysis, resimulations based on the measured geometries of the fabricated diplexer have been carried out using a reduced, effective bulk gold conductivity of 1.2×10^7 S/m. The resimulated model has a CD-loss 3 μm in dimensions, and the sidewall angle is less than 1°. The resimulated and measured results match perfectly as shown in Fig. 15(d)–(f), which also confirms that our simulation model can be used to accurately predict the real results.

Table IV summarizes the simulated and measured performances of the diplexers fabricated by these two techniques. In order to characterize fabrication accuracy and the degree of agreement of the measured data with the simulated results, a performance factor "Δ" is defined here. The "w/o" refers to the measurement from conventional method without RFS, "w/" refers to the measurement from the RFS-based method. It is clearly visible that "Δ. w" based on the RFS technology is far smaller than "Δ. w/o" based on the conventional process in terms of the IL, return loss, isolation, center frequency, bandwidth, and unloaded quality factor Q_u, meaning that the RFS-based microfabricated diplexer is closer to the desired performance ("Sim." in Table IV). Furthermore, "Δ.w/" is possible to further reduced by optimizing the initial DRIE etching recipe for the fixed 100-μm-wide trench etching used in this work in terms of the verticality of the sidewall and surface roughness. The performance of the diplexer has been improved significantly by enhancing the verticality of the sidewalls by the proposed RFS-based microfabrication method. The Q-factor is affected by several parameters, including surface roughness and the geometry of the resonator [42], [49], [50]. The measured Q_u of a single cavity reaches 1410 and 1200 for the lower and upper bands of the diplexer with RFS technology, respectively.

VI. CONCLUSION

Micromachined high-Q waveguide diplexer and filters in the D-band were implemented by the silicon-based DRIE technology. The effect of fabrication inaccuracies, inducing center frequency shift and bandwidth offset, has been investigated. The declination of vertical sidewalls is primarily responsible for any performance degradation. The CD-loss is an additional factor. To solve those problems, the RFS-based microfabrication method to improve the verticality of sidewall and fabrication precision is introduced and verified in this article by comparing the performance deviations with expected values. The RFS-based micromachined prototypes show very good agreement between simulations and measurements in return loss, IL, and isolation, and this has been compared with devices fabricated by the conventional micromachining processes. The measured results presented in this article set the state of the art of D-band diplexers.

The RFS in the HL of the SOI wafer has been used to protect the sidewalls, which allows obtaining almost 90°-vertical sidewalls and good fabrication uniformity independent on the opening sizes. To our knowledge, it is the first

attempt to solve this problem for micromachined waveguide devices from a different perspective compared with the conventional parameter optimization method for ICP machines. While the performance improvement of the RFS-based microfabrication method is demonstrated in this work at D-band, this will be even more important when scaling to higher frequencies, as even higher geometrical confidentially is required when approaching THz frequencies.

ACKNOWLEDGMENT

The authors would like to thank C. Aronsson and M. Bergqvist of KTH Royal Institute of Technology and M. Lindberg of RISE for their help with machine use and measurement setup.

REFERENCES

[1] X. Li and J. Yu, "Over 100 Gb/s ultrabroadband MIMO wireless signal delivery system at the D-band," *IEEE Photon. J.*, vol. 8, no. 5, pp. 1–10, Oct. 2016, doi: 10.1109/JPHOT.2016.2601780.

[2] S. Koenig *et al.*, "Wireless sub-THz communication system with high data rate," *Nature Photon.*, vol. 7, no. 12, pp. 977–981, Dec. 2013, doi: 10.1038/nphoton.2013.275.

[3] T. Schneider, A. Wiatrek, S. Preussler, M. Grigat, and R.-P. Braun, "Link budget analysis for terahertz fixed wireless links," *IEEE Trans. THz Sci. Technol.*, vol. 2, no. 2, pp. 250–256, Mar. 2012, doi: 10.1109/TTHZ.2011.2182118.

[4] *FCC Online Table of Frequency Allocations*, Federal Commun. Commission, Washington, DC, USA, 2019.

[5] S. Carpenter *et al.*, "A -band 48-Gbit/s 64-QAM/QPSK direct-conversion I/Q transceiver chipset," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 4, pp. 1285–1296, Apr. 2016, doi: 10.1109/TMTT.2016.2533491.

[6] M. G. L. Frecassetti *et al.*, "D-band radio solutions for beyond 5G reconfigurable meshed cellular networks," in *Proc. 16th Int. Symp. Wireless Commun. Syst. (ISWCS)*, Aug. 2019, pp. 427–431, doi: 10.1109/ISWCS.2019.8877298.

[7] L. Pometcu and R. D'Errico, "An indoor channel model for high data-rate communications in D-band," *IEEE Access*, vol. 8, pp. 9420–9433, 2020, doi: 10.1109/ACCESS.2019.2960614.

[8] A. Vosoogh *et al.*, "Compact integrated full-duplex gap waveguide-based radio front end for multi-Gbit/s point-to-point backhaul links at E-band," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 9, pp. 3783–3797, Sep. 2019, doi: 10.1109/TMTT.2019.2919539.

[9] B. Beuerle, J. Campion, U. Shah, and J. Oberhammer, "A very low loss 220–325 GHz silicon micromachined waveguide technology," *IEEE Trans. THz Sci. Technol.*, vol. 8, no. 2, pp. 248–250, Mar. 2018, doi: 10.1109/TTHZ.2018.2791841.

[10] J. Campion *et al.*, "Toward industrial exploitation of THz frequencies: Integration of SiGe MMICs in silicon-micromachined waveguide systems," *IEEE Trans. THz Sci. Technol.*, vol. 9, no. 6, pp. 624–636, Nov. 2019, doi: 10.1109/tthz.2019.2943572.

[11] T. Skaik, M. Lancaster, M. Ke, and Y. Wang, "A micromachined WR-3 band waveguide diplexer based on coupled resonator structures," in *Proc. 41st Eur. Microw. Conf.*, Oct. 2011, pp. 770–773, doi: 10.23919/EuMC.2011.6101851.

[12] M. Yata, M. Fujita, and T. Nagatsuma, "Diplexer for terahertz-wave integrated circuit using a photonic-crystal slab," in *Proc. Microw. Photon. (MWP) 9th Asia–Pacific Microw. Photon. Conf. (APMP) Int. Topical Meeting*, Oct. 2014, pp. 40–43, doi: 10.1109/MWP.2014.6994484.

[13] A. Gonzalez, T. Kojima, K. Kaneko, and S. Asayama, "275–500 GHz waveguide diplexer to combine local oscillators for different frequency bands," *IEEE Trans. THz Sci. Technol.*, vol. 7, no. 6, pp. 669–676, Nov. 2017, doi: 10.1109/TTHZ.2017.2758789.

[14] X. Chen, J. Hu, and X. Le, "G-band diplexer based on E-plane waveguide structures," in *Proc. Prog. Electromagn. Res. Symp. (PIERS-Toyama)*, Aug. 2018, pp. 1343–1346, doi: 10.23919/PIERS.2018.8597690.

[15] X. H. Zhao *et al.*, "D-band micromachined silicon rectangular waveguide filter," *IEEE Microw. Wireless Compon. Lett.*, vol. 22, no. 5, pp. 230–232, May 2012, doi: 10.1109/LMWC.2012.2193121.

[16] J. Campion *et al.*, "An ultra low-loss silicon-micromachined waveguide filter for D-band telecommunication applications," presented at the IEEE MTT-S Int. Microw. Symp. Dig., Philadelphia, PA, USA, Jun. 2018.

[17] *M3TERA—Micromachined Terahertz Systems*. Accessed: Feb. 6, 2020. [Online]. Available: https://m3tera.eu/

[18] G. Macchiarella and S. Tamiazzo, "Novel approach to the synthesis of microwave diplexers," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 12, pp. 4281–4290, Dec. 2006, doi: 10.1109/TMTT.2006.885909.

[19] G. Macchiarella and S. Tamiazzo, "Synthesis of star-junction multiplexers," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 12, pp. 3732–3741, Dec. 2010, doi: 10.1109/TMTT.2010.2086570.

[20] P. Zhao and K.-L. Wu, "An iterative and analytical approach to optimal synthesis of a multiplexer with a star-junction," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3362–3369, Dec. 2014, doi: 10.1109/TMTT.2014.2364222.

[21] J. W. Bandler *et al.*, "Space mapping: The state of the art," *IEEE Trans. Microw. Theory Techn.*, vol. 52, no. 1, pp. 337–361, Jan. 2004, doi: 10.1109/TMTT.2003.820904.

[22] S. Koziel and J. W. Bandler, "Space mapping with multiple coarse models for optimization of microwave components," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 1, pp. 1–3, Jan. 2008, doi: 10.1109/LMWC.2007.911969.

[23] O. Glubokov and S. Koziel, "EM-driven tuning of substrate integrated waveguide filters exploiting feature-space surrogates," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2014, pp. 1–3, doi: 10.1109/MWSYM.2014.6848277.

[24] X. Zhao *et al.*, "G-band rectangular waveguide filter fabricated using deep reactive ion etching and bonding processes," *Micro Nano Lett.*, vol. 7, no. 12, pp. 1237–1240, Dec. 2012, doi: 10.1049/mnl.2012.0567.

[25] J. Hu, S. Xie, and Y. Zhang, "Micromachined terahertz rectangular waveguide bandpass filter on silicon-substrate," *IEEE Microw. Wireless Compon. Lett.*, vol. 22, no. 12, pp. 636–638, Dec. 2012, doi: 10.1109/LMWC.2012.2228179.

[26] K. M. K. H. Leong *et al.*, "WR1.5 silicon micromachined waveguide components and active circuit integration methodology," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 4, pp. 998–1005, Apr. 2012, doi: 10.1109/TMTT.2012.2184296.

[27] C. A. Leal-Sevillano *et al.*, "Silicon micromachined canonical E-plane and H-plane bandpass filters at the terahertz band," *IEEE Microw. Wireless Compon. Lett.*, vol. 23, no. 6, pp. 288–290, Jun. 2013, doi: 10.1109/LMWC.2013.2258097.

[28] T. Reck, C. Jung-Kubiak, C. Leal-Sevillano, and G. Chattopadhyay, "Silicon micromachined waveguide components at 0.75 to 1.1 THz," in *Proc. 39th Int. Conf. Infr., Millim., Terahertz Waves (IRMMW-THz)*, Sep. 2014, pp. 1–2, doi: 10.1109/IRMMW-THz.2014.6956008.

[29] J.-X. Zhuang, Z.-C. Hao, and W. Hong, "Silicon micromachined terahertz bandpass filter with elliptic cavities," *IEEE Trans. THz Sci. Technol.*, vol. 5, no. 6, pp. 1040–1047, Nov. 2015, doi: 10.1109/TTHZ.2015.2480844.

[30] X. Zhao, O. Glubokov, U. Shah, and J. Oberhammer, "Highly compact silicon micromachined filter with axial ports at sub-terahertz band," in *Proc. IEEE Asia–Pacific Microw. Conf. (APMC)*, Dec. 2019, pp. 768–770, doi: 10.1109/APMC46564.2019.9038461.

[31] A. R. Brown, P. Blondy, and G. M. Rebeiz, "Microwave and millimeter-wave high-Q micromachined resonators," *Int. J. RF Microw. Comput.-Aided Eng.*, vol. 9, no. 4, pp. 326–337, 1999, doi: 10.1002/(sici)1099-047x(199907)9:4<326::Aid-MMCE4>3.0.CO;2-Y.

[32] O. Glubokov, X. Zhao, B. Beuerle, J. Campion, U. Shah, and J. Oberhammer, "Micromachined multilayer bandpass filter at 270 GHz using dual-mode circular cavities," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2017, pp. 1449–1452, doi: 10.1109/MWSYM.2017.8058894.

[33] A. A. Ayón, X. Zhang, and R. Khanna, "Anisotropic silicon trenches 300-500 μm deep employing time multiplexed deep etching (TMDE)," *Sens. Actuators A, Phys.*, vol. 91, no. 3, pp. 381–385, 2001, doi: 10.1016/S0924-4247(01)00611-2.

[34] G. Chattopadhyay, T. Reck, C. Lee, and C. Jung-Kubiak, "Micromachined packaging for terahertz systems," *Proc. IEEE*, vol. 105, no. 6, pp. 1139–1150, Jun. 2017, doi: 10.1109/JPROC.2016.2644985.

[35] Y. Tang, A. Sandoughsaz, K. J. Owen, and K. Najafi, "Ultra deep reactive ion etching of high aspect-ratio and thick silicon using a ramped-parameter process," *J. Microelectromech. Syst.*, vol. 27, no. 4, pp. 686–697, Aug. 2018, doi: 10.1109/JMEMS.2018.2843722.

[36] S. Biber, J. Schur, and L.-P. Schmidt, "Technological issues for micromachining of new passive THz components based on deep-trench silicon etching," in *Proc. Infr. Millim. Waves, Conf. Dig. Joint 29th Int. Conf. 12th Int. Conf. Terahertz Electron.*, Sep./Oct. 2004, pp. 145–146, doi: 10.1109/ICIMW.2004.1421995.

[37] K.-S. Chen, A. A. Ayon, X. Zhang, and S. M. Spearing, "Effect of process parameters on the surface morphology and mechanical performance of silicon structures after deep reactive ion etching (DRIE)," *J. Microelectromech. Syst.*, vol. 11, no. 3, pp. 264–275, Jun. 2002.
[38] M. K. Hooda, M. Wadhwa, S. Verma, M. M. Nayak, P. J. George, and A. K. Paul, "A systematic study of DRIE process for high aspect ratio microstructuring," *Vaccum*, vol. 84, no. 9, pp. 1142–1148, 2010, doi: 10.1016/j.vacuum.2010.01.052.
[39] J. Oberhammer, "THz MEMS—Micromachining enabling new solutions at millimeter and submillimeter-wave frequencies (invited paper)," in *Proc. IEEE Asia Pacific Microw. Conf. (APMC)*, Nov. 2017, pp. 81–84, doi: 10.1109/APMC.2017.8251382.
[40] G. Chattopadhyay *et al.*, "Silicon micromachining for terahertz component development," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Dec. 2013, pp. 1–4, doi: 10.1109/IMaRC.2013.6777696.
[41] O. Glubokov, X. Zhao, J. Campion, U. Shah, and J. Oberhammer, "Micromachined filters at 450 GHz with 1% fractional bandwidth and unloaded q beyond 700," *IEEE Trans. THz Sci. Technol.*, vol. 9, no. 1, pp. 106–108, Jan. 2019, doi: 10.1109/TTHZ.2018.2883075.
[42] O. Glubokov, X. Zhao, J. Campion, B. Beuerle, U. Shah, and J. Oberhammer, "Investigation of fabrication accuracy and repeatability of high-Q silicon-micromachined narrowband sub-THz waveguide filters," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 9, pp. 3696–3706, Sep. 2019, doi: 10.1109/TMTT.2019.2926244.
[43] J. Li, A. Q. Liu, and Q. X. Zhang, "Tolerance analysis for comb-drive actuator using DRIE fabrication," *Sens. Actuators A, Phys.*, vol. 125, no. 2, pp. 494–503, Jan. 2006, doi: 10.1016/j.sna.2005.08.002.
[44] A. Gomez-Torrent, U. Shah, and J. Oberhammer, "Compact silicon-micromachined wideband 220–330-GHz turnstile orthomode transducer," *IEEE Trans. THz Sci. Technol.*, vol. 9, no. 1, pp. 38–46, Jan. 2019, doi: 10.1109/TTHZ.2018.2882745.
[45] B. Wu, A. Kumar, and S. Pamarthy, "High aspect ratio silicon etch: A review," *J. Appl. Phys.*, vol. 108, no. 5, pp. 051101-1–051101-20, Sep. 2010, doi: 10.1063/1.3474652.
[46] C. Chen-Kuei, "Geometrical pattern effect on silicon deep etching by an inductively coupled plasma system," *J. Micromech. Microeng.*, vol. 14, no. 4, p. 656, 2004.
[47] G. Gattere, F. Rizzini, L. Corso, A. Alessandri, F. Tripodi, and S. Paleari, "Geometrical and process effects on MEMS dimensional loss: A frequency based characterization," in *Proc. IEEE Int. Symp. Inertial Sensors Syst. (INERTIAL)*, Apr. 2019, pp. 1–4, doi: 10.1109/ISISS.2019.8739744.
[48] J. Campion, U. Shah, and J. Oberhammer, "Elliptical alignment holes enabling accurate direct assembly of micro-chips to standard waveguide flanges at sub-THz frequencies," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2017, pp. 1262–1265, doi: 10.1109/MWSYM.2017.8058838.
[49] G. Mendez-Jeronimo, S. C. Sejas-Garcia, and R. Torres-Torres, "Modeling and parameter extraction for the metal surface roughness loss effect on substrate integrated waveguides from S-parameters," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 2, pp. 875–882, Feb. 2018, doi: 10.1109/TMTT.2017.2765328.
[50] M. Abdelfattah and D. Peroulis, "High-Q tunable evanescent-mode cavity SIW resonators and filters with contactless tuners," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 9, pp. 3661–3672, Sep. 2019, doi: 10.1109/TMTT.2019.2925092.

Xinghai Zhao (Graduate Student Member, IEEE) received the dual B.S. degrees in electronic engineering and integrated microelectronics from the University of Electronic Science and Technology, Chengdu, China, in 2004, and the M.S. degree in physical electronics from the Institute of Engineering Physics, Beijing, China, in 2007. He is currently pursuing the Ph.D. degree at the Division of Micro and Nanosystems, KTH Royal Institute of Technology, Stockholm, Sweden.

His current research interest includes terahertz MEMS.

Oleksandr Glubokov (Member, IEEE) was born in Kiev, Ukraine, in 1985. He received the M.Sc. degree in telecommunications from the National Technical University of Ukraine (KPI), Kiev, in 2007, and the Ph.D. degree in electronic and electrical engineering from the University of Westminster, London, U.K., in 2011.

From 2012 to 2014, he was a Post-Doctoral Research Fellow with Reykjavík University, Reykjavík, Iceland. Since 2015, he has been a Post-Doctoral Researcher on MEMS THz systems project with Micro- and Nanosystems at the KTH Royal Institute of Technology, Stockholm, Sweden. His research interests include filter design at RF/microwave/millimeter-wave/terahertz (THz) frequency ranges, passive sub-THz devices, and their numerical optimization.

James Campion (Graduate Student Member, IEEE) received the B.E. degree (Hons.) in electronic engineering from University College Dublin, Dublin, Ireland, in 2012, and the M.Sc. degree in electrical engineering from the Chalmers University of Technology, Gothenburg, Sweden, in 2015.

He specialized in microwave engineering, MMIC design, and VNA calibration and measurement techniques at the Chalmers University of Technology. He joined the Department of Micro and Nanosystems, KTH Royal Institute of Technology, Stockholm, Sweden, in 2015. His current research interests include terahertz (THz) MEMS sources, systems, and measurement techniques.

Adrian Gomez-Torrent (Graduate Student Member, IEEE) was born in Artariain, Spain, in 1990. He received the B.Sc. and M.Sc. degrees from the Public University of Navarra (UPNA), Pamplona, Spain, in 2014.

From 2013 to 2017, he was with the Antennas and Microwave Components Group, UPNA, where he was involved with microwave passive devices and silicon micromachining for RF/terahertz (THz) components. Since 2017, he has been with the Division of Micro and Nanosystems, KTH Royal Institute of Technology, Stockholm, Sweden. His research interests include silicon micromachining for microwave and sub-THz passive waveguide components, antennas, and switching matrices for beam-steering applications.

Aleksandr Krivovitca was born in Stary Oskol, Russia, in 1991. He received the B.S. degree in electronics and nanoelectronics and the Master of Science degree (Hons.) in electronics and nanoelectronics, nano and microsystem technology from Saint Petersburg Electrotechnical University "LETI," Saint Petersburg, Russia, in 2012 and 2014, respectively. He is currently pursuing the Ph.D. degree at the Micro and Nanosystems Group, KTH Royal Institute of Technology, Stockholm, Sweden.

His research interests include SIW platform development at RF/microwave/millimeter-wave/terahertz (THz) frequency ranges and design of passive and MEMS-based sub-THz devices.

Umer Shah (Member, *IEEE*) was born in Bannu, Pakistan, in 1981. He received the B.S. degree in engineering from the Ghulam Ishaq Khan Institute of Engineering Sciences and Technology, Topi, Pakistan, in 2003, the M.Sc. degree in wireless engineering from the Technical University of Denmark, Kongens Lyngby, Denmark, in 2007, and the Ph.D. degree in microsystem technology from the KTH Royal Institute of Technology, Stockholm, Sweden, in 2014.

Since May 2014, he has been a Post-Doctoral Researcher with the Micro and Nanosystems Group, KTH Royal Institute of Technology. He has authored or coauthored more than 30 reviewed articles. His research interests include RF MEMS-based filters, phase shifters, matching circuits, and antennas.

Dr. Shah was a recipient of the Best Student Paper Award presented at the Asia–Pacific Microwave Conference 2010, Yokohama, Japan, and the 2014 IEEE MTT-S Graduate Fellowship Award for his research activities.

Joachim Oberhammer (Senior Member, IEEE) was born in Italy in 1976. He received the M.Sc.EE degree from the Graz University of Technology, Graz, Austria, in 2000, and the Ph.D. degree from the KTH Royal Institute of Technology, Stockholm, Sweden, in 2004.

He was a Post-Doctoral Research Fellow with Nanyang Technological University, Singapore, in 2004, and Kyoto University, Kyoto, Japan, in 2008. Since 2005, he has been leading radio frequency/microwave/terahertz microelectromechanical systems research at the KTH Royal Institute of Technology. In 2010, he was an Associate Professor with the KTH Royal Institute of Technology, where he has been a Professor in microwave and terahertz (THz) microsystems since 2015. He was a Guest Researcher with Nanyang Technological University, Singapore, in 2007, a Guest Researcher with the NASA-Jet Propulsion Laboratory, Pasadena, CA, USA, in 2014, and a Guest Professor with the Universidad Carlos III de Madrid, Madrid, Spain, in 2019. He has authored or coauthored more than 100 reviewed research articles and holds four patents.

Dr. Oberhammer served as a TPRC Member for the IEEE Transducers in 2009, 2015, and 2019, the IEEE International Microwave Symposiums from 2010 to 2018, the IEEE Micro Electromechanical Systems in 2011 and 2012, the IEEE Radio and Wireless Week in 2015 and 2016, and EuMCE in 2019. He has been a Steering Group Member of the IEEE MTT-S and AP-S Chapters Sweden since 2009. He was a Steering Group Member of the Young Academy of Sweden from 2014 to 2016. He received an award by the Ericsson Research Foundation, a grant by the Swedish Innovation Bridge, and a scholarship by the Japanese Society for the Promotion of Science in 2004, 2007, and 2008, respectively. The research work that he is heading received six best paper awards (five of which at IEEE conferences) and four IEEE Graduate Fellowship Awards (by MTT-S and by AP-S) since 2009. In 2013, he received an ERC Consolidator Grant by the European Research Council. He was a Representative of Sweden/Norway/Iceland in the European Microwave Association from 2016 to 2018. He has been an Associate Editor of the IEEE TRANSACTIONS ON TERAHERTZ SCIENCE AND TECHNOLOGY since 2018.