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2008

Kim, T. H., Persaud, R., & Kim, C. H. (2008). Silicon odometer: an on-chip reliability monitor for measuring frequency degradation of digital circuits. IEEE Journal of Solid State Circuits. 43(4), 874-880.

https://hdl.handle.net/10356/93518

https://doi.org/10.1109/JSSC.2008.917502

Silicon Odometer: An On-Chip Reliability Monitor for Measuring Frequency Degradation of Digital Circuits

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***Abstract*—Precise measurement of digital circuit degradation is a key aspect of aging tolerant digital circuit design. In this study, we present a fully digital on-chip reliability monitor for high-resolution frequency degradation measurements of digital circuits. The proposed technique measures the beat frequency of two ring oscillators, one stressed and the other unstressed, to achieve 50× higher delay sensing resolution than that of prior techniques. The differential frequency measurement technique also eliminates the effect of common-mode environmental variation such as temperature drifts between each sampling points. A 265×132 μm^2 test chip implementing this design has been fabricated in a 1.2 V, 130 nm CMOS technology. The measured resolution of the proposed monitoring circuit was 0.02%, as the ring oscillator in this design has a period of 4 ns; this translates to a temporal resolution of 0.8 ps. The 2 μs measurement time was sufficiently short to suppress the unwanted recovery effect from concealing the actual circuit degradation.**

***Index Terms*—Aging, degradation, monitoring circuit, NBTI, reliability.**

I. Introduction

As CMOS process technology continues to follow an aggressive scaling roadmap, designing reliable circuits has become ever more challenging with each technology node. Reliability issues such as bias temperature instability (BTI), hot carrier injection (HCI), and time-dependent dielectric breakdown (TDDB) has become more prevalent as the electrical field continues to increase in nanoscale CMOS devices. One of the most pressing of these challenges is negative bias temperature instability (NBTI) [1]–[4] caused by the trap generation in the Si–SiO_2 interface of pMOS transistors (Fig. 1). Structural mismatch at the Si-SiO_2 interface causes dangling bonds, which act as interfacial traps. During the hydrogen passivation process that follows oxidation, dangling Si bonds are transformed into Si-H bonds. These bonds are weak enough to break during device operation, causing H atoms to diffuse into gate oxide, and the broken bonds that remain become traps, effectively degrading the drive current of pMOS transistors. NBTI is characterized by a positive shift in the absolute value of the pMOS threshold voltage ($|\mathrm{Vtp}|$), which occurs when the device is stressed ($\mathrm{Vgs} = -\mathrm{VCC}$), and this effect is more pronounced at high temperatures. This degradation in Vtp has believed to exhibit a power-law dependency on time and is an exponential function of the stress voltage level as well as temperature. When the stress conditions are removed (i.e., $\mathrm{Vgs} = 0$), the device enters a recovery or passivation phase, where H atoms diffuse back towards the Si–SiO_2 interface and anneal the broken Si–H bonds, thereby reducing $|\mathrm{Vtp}|$ [Fig. 1(b) and (c)] [5]–[11].

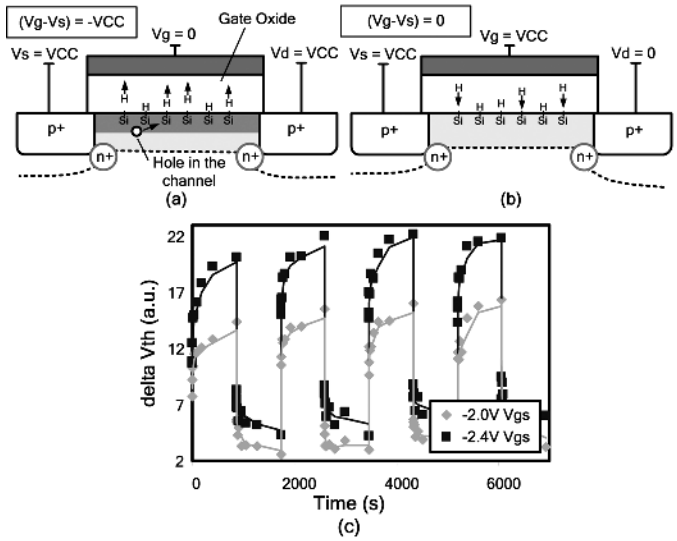

Fig. 1. Cross section of pMOS device under (a) NBTI stress and in (b) recovery mode. (c) pMOS Vt degradation for alternating stress and recovery periods in 130 nm CMOS [5].

To estimate the impact of NBTI on circuit performance and eventually design aging-tolerant circuits, accurate measurement of digital circuit reliability is imperative. Previous reliability measurements relied on device probing or on-chip ring-oscillator frequency monitoring, which either require an extensive measurement setup or have limited sensing resolution [12], [13]. Moreover, they were inefficient in collecting a statistically significant number of data points under various stress conditions, which is crucial in understanding the complexities of aging (e.g., statistical behavior and process and frequency dependencies.). In this study, we propose an on-chip reliability monitor that can remedy the shortcomings of previous techniques and accurately characterize and track the aging effect in digital circuits. The remainder of this paper is organized as follows. Section II reviews the previous reliability monitoring techniques. Section III is devoted to the design of the proposed reliability monitoring circuit, the "silicon odometer," as well as simulation results [14]. Section IV addresses the implementation of the test chip and present the measurement results. The paper concludes in Section V.

Manuscript received August 24, 2007; revised October 29, 2007.

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Digital Object Identifier 10.1109/JSSC.2008.917502

II. Previous Reliabiltiy Monitoring Techniques

The typical approach used when measuring NBTI is to apply stress for a given duration, remove it, and then perform an *I–V* measurement. To accurately measure the effects of NBTI, this measurement must be done quickly to avoid the effects of recovery, which has been reported to occur even for measurement windows of a few microseconds [7]. On-the-fly techniques that minimize the recovery effect have been examined in [6], [7], [9], [13], [14], and [16]. Denais *et al.* proposed a measurement technique in which the stress voltage is kept quasi-constant while the linear drain current is measured to monitor device degradation. However, it still requires extra equipment for the accurate measuring of device current under test which limits its application for run-time NBTI monitoring in actual products. In [16], this on-the-fly technique was extended to characterize the recovery after stress conditions are removed. Fernández *et al.* proposed on-chip circuits for the characterization of device degradation due to AC NBTI stress, which is claimed to be viable up to the GHz range [15]. The authors assert that a high frequency stress signal can be reliably applied to the devices under test, and utilize this information to extract data regarding the frequency dependency of NBTI aging. A frequency degradation monitoring circuit was proposed in [9], where a ring oscillator is stressed and the difference of ring oscillator period before and after the stress is measured. However, this circuit has a low sensing resolution and requires highly accurate and expensive test hardware, making it an invasive and intractable approach for run-time monitoring of NBTI. In addition, the measurement results are very sensitive to environmental variations such as temperature shifts, which make it difficult to determine what portion of device degradation is due solely to NBTI.

In this paper, we propose an aging monitoring circuit which is capable of taking fast and precise degradation measurements by detecting the beat frequency of a pair of ring oscillators, where only one is placed under stress. This differential measurement method eliminates the effect of environmental variations that plague other approaches, such as changes in temperature and supply voltage. This implementation also facilitates the application of both DC and AC stress signals, allowing the effects of both types of phenomenon to be studied. No specialized measurement equipment is required for the proposed measurement circuit, as on-chip structures have been implemented which convert performance degradation into a simple digital code. The proposed circuit can also be used for adaptive techniques that can compensate for the performance loss due to device aging by adjusting the supply voltage or clock frequency.

III. Silicon Odometer: Proposed Reliability Monitoring Circuit

A. Beat-Frequency Detection Scheme

The core circuit for detecting frequency degradation consists of two free-running ring oscillators and a phase comparator, as shown in Fig. 2(a). During the stress period, one of the ring oscillators is stressed, while the other remains unstressed. The supply voltage of the stressed ring oscillator is raised to V_{DD-STR} during stress periods and lowered to V_{DD-NOM} during the periodic measurements, while the supply of the reference oscillator is lowered to 0 V and raised to V_{DD-NOM}

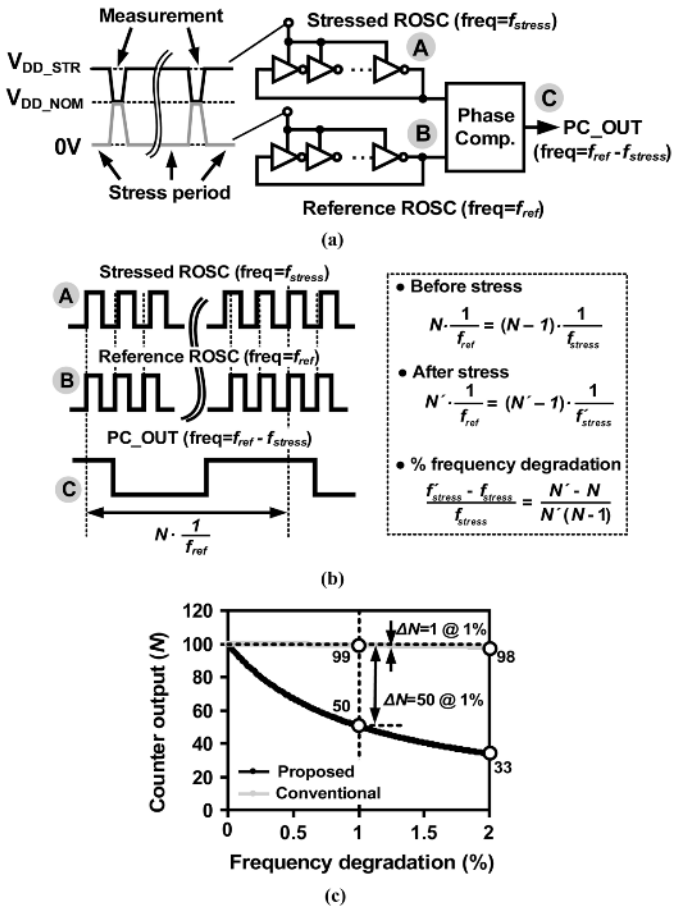


Fig. 2. (a) Proposed beat-frequency detection circuit for high-resolution NBTI monitoring. (b) Principle of proposed circuit. (c) Comparison of frequency sensing resolution between conventional and proposed techniques. Proposed scheme provides 50× higher sensing resolution for detecting 1% frequency degradation.

during the stress and measurement periods, respectively. The reference oscillator's supply voltage is grounded during the stress periods to prevent device aging. Once the measurement signal is triggered, a phase comparator uses the reference ring oscillator to sample of the output of its stressed duplicate. The output of this phase comparator exhibits the beat frequency $f_{\rm stress} - f_{\rm ref}$, where $f_{\rm stress}$ is the stressed ring oscillator frequency and $f_{\rm ref}$ is the reference ring oscillator frequency. A counter which uses the reference ring oscillator signal as a clock measures the beat frequency. The counter's output N is measured after each stress period to calculate the percent frequency degradation, and the relationship between these two properties is shown in Fig. 2(b). The period of the beat frequency is equal to the time when there is one clock difference between the number of reference and stress clock pulses, and the details of this beat frequency calculation is shown in Fig. 2(b). Before stress, if the output of the counter is N, the number of clocks counted in the stressed ring oscillator is $N-1$. The period of beat frequency can be calculated by $N/f_{\rm ref}$ or $(N-1)/f_{\rm stress}$. After stress, if the output of the counter is N', the number of clock pulses counted in the stressed ring oscillator is $N'-1$. Analogous to the calculation described above, the period of beat frequency is $N'/f'_{\rm ref}$ or $(N'-1)/f'_{\rm stress}$. Using these two relations, the percentage of the frequency degradation can

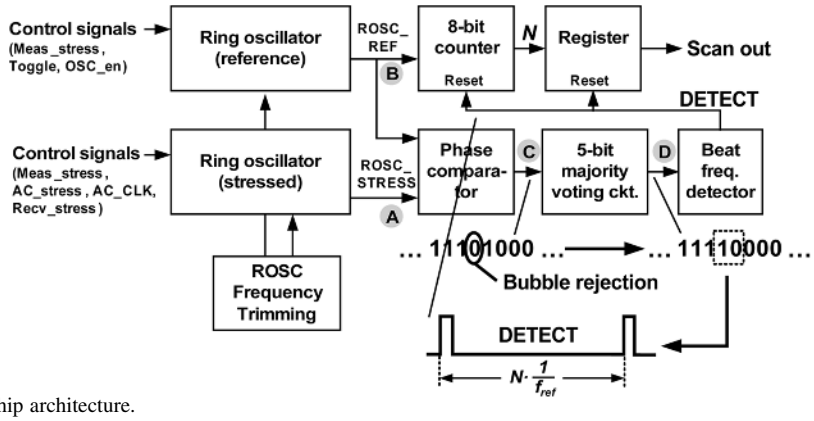


Fig. 3. Silicon-odometer test chip architecture.

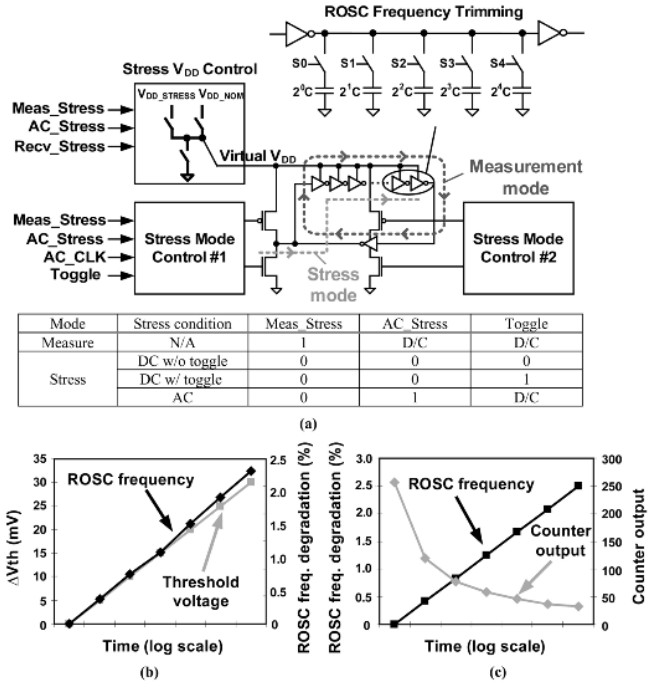
be obtained as illustrated in Fig. 2(b). Previous measurement techniques that utilized only a single stressed ring oscillator [9] have a much more limited sensing resolution, as the counter output N is directly proportional to the frequency degradation. For example, in [9], 1% degradation in ring oscillator frequency translates into 1% change in counter output [Fig. 2(c)]. Using our proposed design, 1% degradation in ring oscillator frequency results in a 50% change in the counter output, offering $50\times$ sensing resolution in the early stages of degradation. Increasing measurement sensitivity at the early stage of degradation generates less sensitivity when there is large frequency degradation. However, frequency degradation caused by device aging is usually less than 10% [9]. The proposed measurement circuit uses 90% of the total code to detect a 10% frequency change, which has a higher sensing resolution compared with the previous scheme using only 10% of the total code [9]. The proposed silicon odometer circuit with a high sensing resolution can provide a number of benefits such as reduced test time, the capability to study aging under various stress conditions, and enabling nonaccelerated stress measurements. Note that the resolution of the proposed reliability monitor (i.e., $\Delta N/\Delta f_{\mathrm{stress}}$) depends on the initial counter output N, which is set before the commencement of stress experiments. An initial N of 100 (or 256) allows a sensing resolution of 0.02% (or 0.0015%) at the early stage of degradation. The closer the frequencies of the two ring oscillators are brought together initially (i.e., the larger the initial N), the larger the change in counter output that can observed for the same degradation in ring oscillator frequency. Measurement accuracy can be easily programmed by changing the initial counter output using the simple capacitor trimming circuits shown in Fig. 4(a).

B. Silicon Odometer Test Chip Architecture

The architecture of the silicon odometer test chip is illustrated in Fig. 3. The two 105-stage ring oscillators are identical structures only differentiated by the different control inputs. Process-voltage-temperature (PVT) variations that affect both structures equally will not alter the monitor output as the differential measurement approach cancels out this common-mode noise. Thick-oxide I/O devices are used for the peripheral control circuits that are connected to the stress voltage. As described above, the phase comparator produces a digital signal representing the relationship between the frequencies of the reference and stressed ring oscillators. Bubbles (i.e., a lone "1" in a stream of "0"s or a "0" in a stream of "1"s) that may appear in the phase comparator output due to jitter and other circuit uncertainties can be eliminated by using a 5-bit majority voting circuit. The DETECT pulse generated by the beat-frequency detector causes the register to sample the counter output and resets the counter for the next measurement cycle. For robust measurement results, multiple measurements are executed and the measured counter outputs are analyzed to calculate the frequency degradation. A parallel-to-serial register is used to scan out the measurement data.

C. Ring Oscillator Circuit

Fig. 4 shows a detailed schematic of the ring oscillator, as well as the various stress mode controls. The virtual $\mathrm{V_{DD}}$ can be switched to $\mathrm{V_{DD-STRESS}}$, $\mathrm{V_{DD-NOM}}$, and 0 V to allow for stress, measurement, and recovery periods for the reference and stressed ring oscillators. During the stress period, the virtual $\mathrm{V_{DD}}$ in the stressed ring oscillator is connected to $\mathrm{V_{DD_STRESS}}$, while that of the reference ring oscillator is connected to 0 V to remove stress and keep its devices fresh. Only half of devices that are turned on are stressed. In the measurement period, the virtual $\mathrm{V_{DD}}$ port in both ring oscillators is connected to $\mathrm{V_{DD}}$, to allow measurement of the NBTI-induced degradation. Based on the values of the control signals, stress-mode control #1 applies either AC or DC inputs. The AC_CLK signal utilized for AC stress is generated from an internal VCO. The ring oscillator input can also be toggled during each stress period to measure the circuit recovery with stress in alternating inverter stages. Stress-mode control #2 disconnects the ring oscillator during stress mode to allow for various stress inputs to be applied. The table in Fig. 4 lists the control signals and corresponding measurement and stress modes. To achieve a high-resolution frequency degradation measurement, the initial counter output should be large. The size of the initial counter output is highly sensitive to mismatches between two ring oscillators, so we have implemented a 5-bit binary-weighted switched-capacitor stage to allow adjustments to the initial ring oscillator frequencies. The desired counter output N is set prior to the stress experiments by scanning in control signals S0–S4. While in this work we have chosen to utilize an inverter chain-based ring oscillator for the test structure; other logic gates, such as NANDs, NORs, and pass gates, can also be utilized.



Mode	Stress condition	Meas_Stress	AC_Stress	Toggle
Measure	N/A	1	D/C	D/C
Stress	DC w/o toggle	0	0	0
	DC w/ toggle	0	0	1
	AC	0	1	D/C

Fig. 4. Ring oscillator circuit and measurement/stress modes. (b) Simulation results of stress time versus pMOS threshold voltage and ring oscillator frequency. (c) Frequency and counter output as a function of stress time.

The effect of threshold voltage degradation on frequency degradation was simulated and is shown in Fig. 4(b). The threshold voltage before stress was 320 mV, and an inverter-based ring oscillator was used. It was assumed that all pMOS devices in the ring oscillator are stressed, which is equivalent to the ring oscillator under AC stress condition. Simulations show that frequency and threshold voltage degradation are proportional to one another. A 30 mV change in pMOS threshold voltage causes 2.79% degradation in ring oscillator frequency. Fig. 4(c) shows the counter output and the ring oscillator frequency degradation versus stress time. As explained in Section III.A, the initial small degradation in delay translates into a large change in the counter output making our sensor effective in detecting extremely small frequency shifts. The output code changed by 139 for a frequency degradation of 0.45% as shown in Fig. 4(c).

D. Phase Comparator Circuit

A phase comparator shown in Fig. 5 is used as a core circuit for detecting the beat frequency. A clock tapped out from the reference ring oscillator signal is used as the CLK input to control the operation modes of the phase comparator. When the CLK is low, the phase comparator is in pre-charge mode and resets the phase comparator output (PC_OUT). When the CLK becomes "1," the phase comparator switches to an evaluation mode and the PC_OUT is determined based on the arrival time of the two input signals, ROSC_REF and ROSC_STRESS. If there is an overlapped region between A' and B, the pre-charged node is discharged and phase comparator goes high. No overlapped region will keep the pre-charged node high while giving a low output.

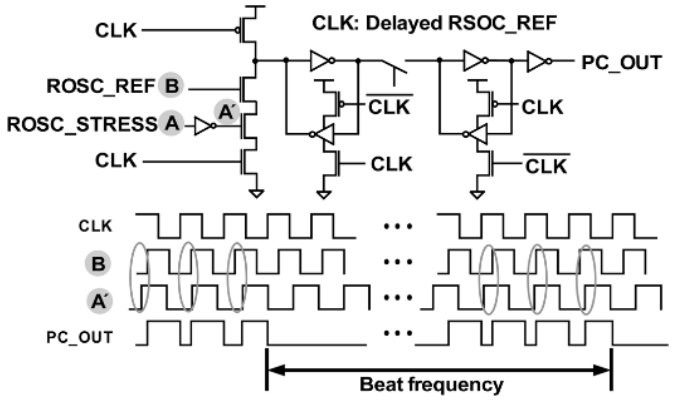


Fig. 5. Phase comparator circuit.

When the measurement begins, the rising edges of two input signals are aligned to each other and cause PC_OUT to go high. If the stressed ring oscillator has not been stressed, the frequency of two input signals will be identical, which makes PC_OUT always high. In this case, the maximum counter output is sent as read data. If the stressed ring oscillator has experienced the effects of aging, the frequency of the stressed ring oscillator decreases. As a result, the overlapped region between B and A' decreases in evaluation mode and the phase comparator output becomes low. The phase comparator will continuously generate a low output until there is a region of overlap between its two inputs. The data pattern at the phase comparator output repeats whenever there is one clock cycle difference between two input signals, which is used to measure the beat frequency.

In general, accurate measurement of phase differences requires a high-resolution phase comparator. However, the proposed beat-frequency detection scheme relaxes this design requirement. Any offset in the phase comparator simply shifts the start and end point of the measured time, without affecting the period. In addition, the measured period of the beat frequency is more sensitive to the degradation in ring oscillator frequency than the resolution of the phase comparator. For example, assume a jitter of 40 ps in phase comparator, a period of 4 ns in ring oscillator, and 1% frequency degradation in the ring oscillator. Forty ps of jitter represents 1% frequency error which is equal to the target frequency degradation, so a direct nondifferential frequency degradation measurement can have an error of 100%. However, in our beat-frequency detection scheme, the time in which the measurement could be affected by phase comparator jitter is much smaller than the total measured period. Under the same assumptions discussed above and an initial counter output N of 100 before stress is applied, the 40 ps jitter can only shift the clock count by one. By utilizing the equations in Fig. 2, the calculated frequency degradation including the error caused by the jitter in phase comparator becomes 1.05% or 0.97% while the true degradation is 1%. Our measurement technique has a 5% error which improves upon the direct measurement scheme by $20\times$.

E. Majority Voting Circuit

When two input signals are closely aligned, the power supply noise or other uncertainties in the phase comparator circuit can generate bubbles (i.e., lone "1" in a stream of "0"s or a "0" in

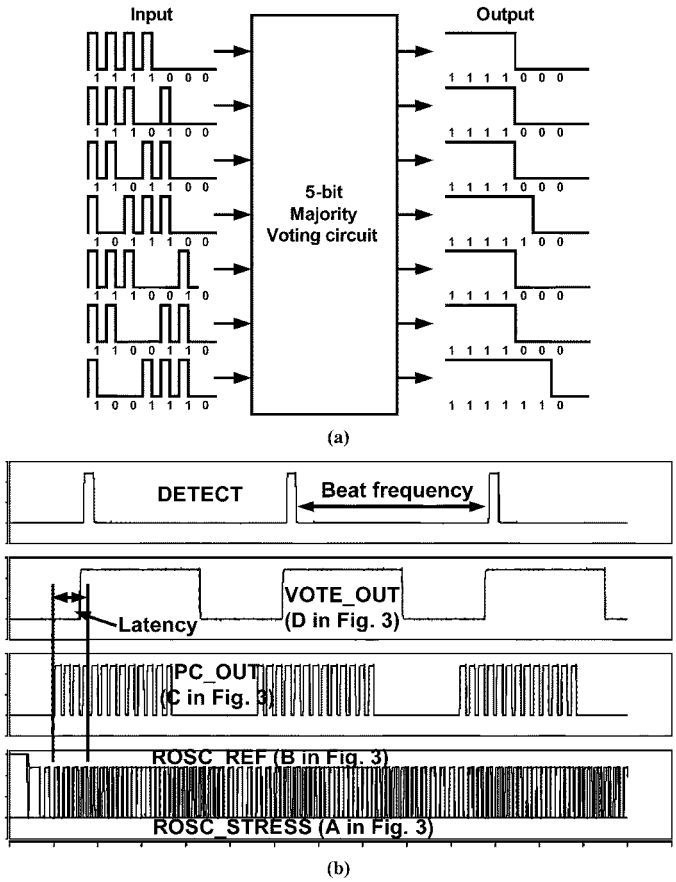


Fig. 6. (a) Operation of 5-bit majority voting circuit. (b) Simulated waveforms during measurement mode.

a stream of "1"s) in the output. A 5-bit majority voting circuit was implemented to eliminate these bubbles. The implemented majority voting circuit can filter out two bubbles in a five bit data sequence. Fig. 6(a) shows a phase comparator outputs affected by bubbles, as well as the filtered data that are generated by the majority voting circuit.

F. Beat-Frequency Detector

The output of the majority voting circuit is a signal with the beat frequency. The beat-frequency detector generates a flag signal, DETECT, to read the counter output and reset the counter for the next measurement. The time interval between DETECT signals is the period of beat frequency. DETECT is used as a sampling clock in the register and reset signal in the counter. The rising edge of the majority voter output is detected by combinational logic using five received data points. Fig. 6(b) shows sample simulated waveforms. It can be seen that the period of PC_OUT and VOTE_OUT is identical to that of DETECT. There is a delay between VOTE_OUT and DETECT due to the data storing operation of the majority voting circuit and the latency of the beat frequency detector.

IV. Test Chip Implementation and Experimental Results

A test chip was implemented in a 1.2 V 130 nm CMOS process technology to demonstrate the proposed silicon odometer circuit. The reference and stressed ring oscillators consist of 105 inverter stages giving a period of 4 ns. The target initial counter output (i.e., N in Fig. 2) was set to be 100 based on a target sensing resolution of 0.02% (or 0.8 ps), so an 8-bit counter was used to allow for a counter output up to 256. The initial calibration was done by scanning in the capacitor trimming controls S0-S4 shown in Fig. 4(a) and reading out the counter output. Both ring oscillators contain trimming circuits allowing a wider and finer calibration range for the initial count. By setting the initial count to be 100, 20× higher measurement accuracy was achieved compared with the previous technique [9], where the sensing resolution was 3.9%. Fresh chips were used in each measurement as, once stressed, circuits will not fully recover to its initial fresh state. An input signal with a frequency of up to 1 GHz was applied to test for AC NBTI stress. The die area of the test circuit was 265 × 132 μm^2 [Fig. 7(a)]. Fig. 7(b) shows the laboratory setup for the test chip measurements.

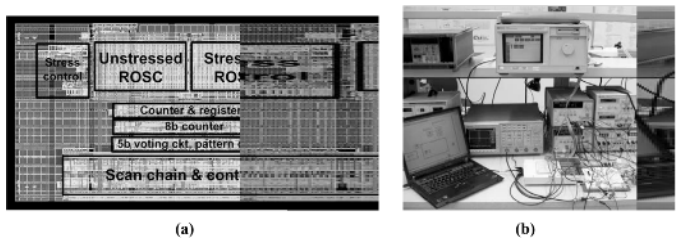


Fig. 7. (a) Layout of 130 nm test chip occupying 265 × 132 μm^2. (b) Laboratory setup for test chip NBTI measurements.

Fig. 8(a) shows the measured counter output, while the corresponding frequency degradation is plotted in Fig. 8(b) using the equation in Fig. 2. The supply voltage of the stressed ring oscillator was shut down to 0 V during the recovery periods. A nominal supply voltage of 1.2 V was applied to both ring oscillators during measurement modes. The high sensing resolution of the proposed sensor enabled aging measurements without using a higher supply voltage as the stress voltage. Such measurements done under a nonaccelerated stress condition allows us to study the circuit aging effect during normal chip operation. Three measurement samples were taken at each measurement point and the error bar indicates the variation between the data samples. The worst case error between the sampled data and the average point was only 0.022%. The ring oscillator frequency was reduced by 0.238% at the end of the first stress period of 1730 s when stressed at V_0 and 30°C. Stress voltage V_0 is not specified due to the company confidentiality. Removing the stress voltage gave a 90.5% recovery of the performance loss by the end of the first recovery period. Such a large extent of recovery is typically seen in older processes with thicker oxides where most of the hydrogen atoms, which are the consequences of the broken Si–H bonds, remain in the oxide region and quickly anneal when the stress is removed. The frequency degradation at different temperatures is illustrated in Fig. 8(c). Measurements were done at 30 °C and 130 °C for comparison. It can be seen that a higher temperature accelerates the frequency degradation. Frequency degradation under DC and AC stress conditions are shown in Fig. 8(d). DC stress shows significantly larger degradation than AC stress while the impact of AC stress frequency

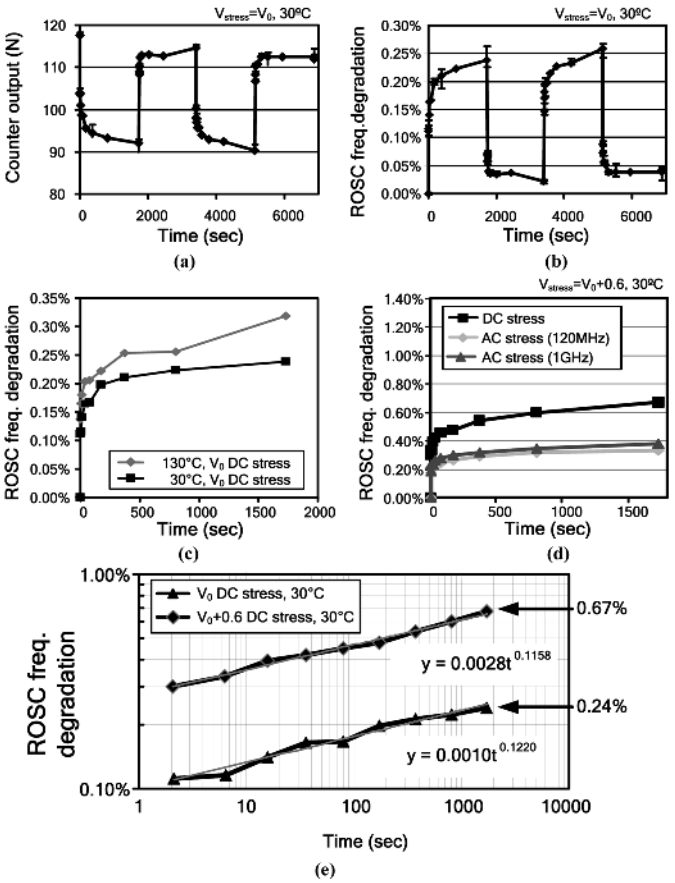


Fig. 8. Measurement results. (a) Counter output. (b) Calculated frequency degradation for alternating stress and recovery periods. Error bars show the variation between the three sampled data taken at each measurement points. (c) Frequency degradation at different temperatures. (d) Frequency degradation under DC and AC stress. (e) Frequency degradation for different stress voltages.

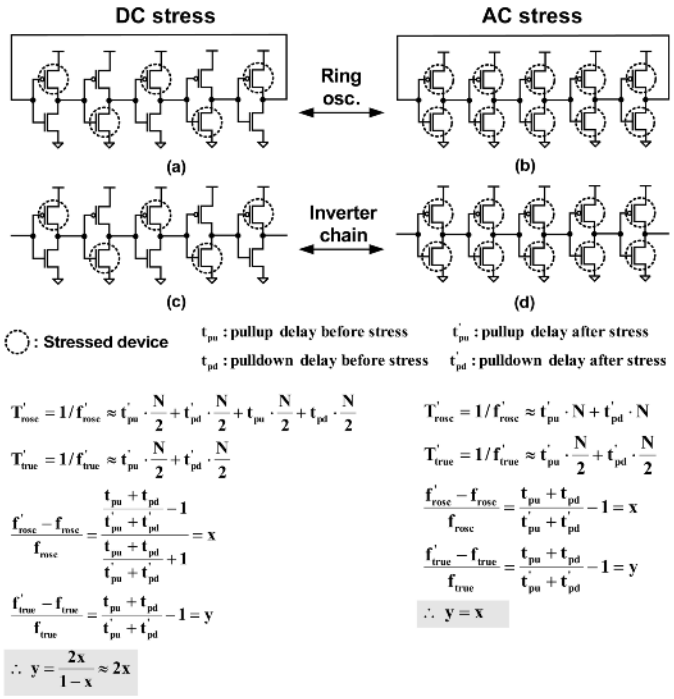


Fig. 9. Relationship between the ring oscillator frequency degradation and the worst case true inverter chain frequency degradation for DC and AC stress. Frequency degradation of a true inverter chain is twice that of the ring oscillator frequency degradation for the DC stress case. On the other hand, the two circuits observe the same amount of frequency degradation under AC stress.

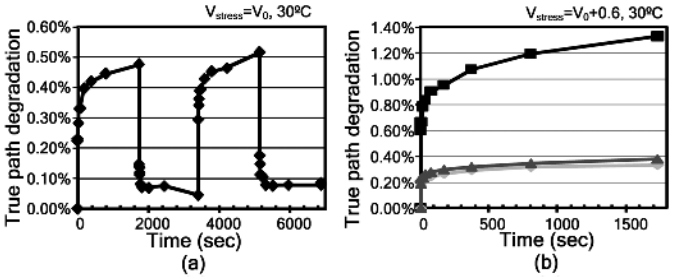


Fig. 10. True frequency degradation of an inverter chain calculated from the measurement results in Fig. 8(b). (b) True inverter chain frequency degradation calculated from the measurement results in Fig. 8(d).

on aging turned out to be small which agrees with previous observations [17]. This is due to the fact that AC stress signals with same duty cycles have the same effective stress time irrespective of the AC stress frequency. Raising the stress voltage increases electric field which in turn worsens the NBTI degradation. Fig. 8(e) shows the measured frequency degradation at different stress voltages. Similar to threshold voltage, frequency degradation also has a power-law dependency on stress time. The power-law equations obtained by curve fitting indicate time exponents of 0.1158 and 0.1220 for stress voltages of $V_0 + 0.6$ and V_0, respectively. After 1730 s of stress, a frequency degradation of 0.67% was observed when using $V_0 + 0.6$ as the stress voltage. When a stress voltage of V_0 was used, the measured frequency degradation was 0.24%.

When applying DC stress to the ring oscillator, only half of the devices are under stress, so the period of the ring oscillator is decided by the summation of the delay from stressed path and that from unstressed path as shown in Fig. 9(a). On the other hand, the worst case frequency degradation of a true inverter path is determined by the delay of the stressed path only [Fig. 9(b)]. The relationship between the frequency degradation measured from ring oscillator and that of our target, the true frequency degradation is given in Fig. 9. The true stressed inverter chain delay can be calculated by adding the stressed pull-up delay and stressed pull-down delay. By using these two expressions, the true frequency degradation can be represented as a function of ring oscillator frequency degradation. Our derivation shows that, under DC stress, the degradation of the ring oscillator frequency is almost the half that of the true inverter chain. During periods of AC stress, all pMOS devices and nMOS devices are stressed equally, so the period of the ring oscillator is simply double that of the inverter delay. As a result, the measured ring oscillator frequency degradation is equal to that experienced by the inverter chain. The true inverter chain frequency degradation from the DC stress measurement results is shown in Fig. 10(a). Note that the amount of degradation shown in Fig. 10(a) is twice as large as that in Fig. 8(b). The true inverter frequency degradation from AC stress calculated using the equations in Fig. 9 is plotted in Fig. 10(b). Note that the degradation of nMOS transistors is negligible when poly gates are used. Therefore, the measured degradations are mostly due to NBTI.

V. Conclusion

NBTI is a growing threat to circuit reliability due to its increased impact on circuit performance with each new technology node. By helping designers to monitor aging during circuit operation, on-chip NBTI monitoring structures can help them to better understand these effects and ultimately assist them in building aging-tolerant systems. In this paper, we propose a silicon odometer based on a beat-frequency detection scheme, which enabled a sensing resolution of less than 0.02% (or 0.8 ps) for a 4 ns period ring oscillator. The minimum time required for obtaining one data sample was 2 μs which was short enough to avoid any noticeable recovery effects. In addition, the differential measurement approach minimized the effect of common mode environmental variations. The silicon odometer was implemented using fully digital circuits which only require a minimum of calibration. Various operation modes have been implemented and tested. Measurement results illustrate basic characteristics of NBTI that are in line with the effects described in previous works. Finally, the relationship between true inverter chain frequency degradation and ring oscillator frequency degradation was analyzed in both the DC as well as the AC stress cases. The measured ring oscillator frequency degradation during DC stress is 50% of that of the true inverter chain, and is equal to that of the true inverter chain frequency during AC stress.

References

[1] V. Huard and M. Denais, "Hole trapping effect on methodology for DC and AC negative bias temperature instability measurements in pMOS transistors," in *Proc. IEEE Int. Reliabil. Phys. Symp.*, Apr. 2004, pp. 40–45.

[2] M. Denais *et al.*, "New perspectives on NBTI in advanced technologies: Modeling and characterization," in *Proc. IEEE Eur. Solid-State Device Res. Conf.*, Sep. 2005, pp. 399–402.

[3] R. Vattikonda, W. Wang, and Y. Cao, "Modeling and minimization of pMOS NBTI effect for robust nanometer design," in *Proc. IEEE Design Autom. Conf.*, Jul. 2006, pp. 1047–1052.

[4] M. Ershov *et al.*, "Transient effects and characterization methodology of negative bias temperature instability in pMOS transistors," in *Proc. IEEE Int. Reliabil. Phys. Symp.*, Apr. 2003, pp. 606–607.

[5] J. Keane, T. Kim, and C. H. Kim, "An on-chip NBTI sensor for measuring pMOS threshold voltage degradation," in *Proc. IEEE Int. Symp. Low Power Electron. Design*, Aug. 2007, pp. 189–194.

[6] S. Aota *et al.*, "A new method for precise evaluation of dynamic recovery of negative bias temperature instability," in *Proc. IEEE Int. Conf. Microelectron. Test Structures*, Apr. 2005, pp. 197–199.

[7] C. Schlunder *et al.*, "On the impact of the NBTI recovery phenomenon on lifetime prediction of modern p-MOSFETs," in *Proc. IEEE Int. Integr. Reliabil. Workshop*, Oct. 2006, pp. 1–4.

[8] S. Zafar, "Statistical mechanics based model for negative bias temperature instability," *J. Appl. Phys.*, vol. 97, no. 10, pp. 1–9, 2005.

[9] V. Reddy *et al.*, "Impact of negative bias temperature instability on digital circuit reliability," in *Proc. IEEE Int. Reliabil. Phys. Symp.*, 2002, pp. 248–254.

[10] S. Rangan, N. Mielke, and E. Yeh, "Universal recovery behavior of negative bias temperature instability," in *Proc. IEEE Int. Electron Devices Meet.*, 2003, pp. 14.3.1–14.3.4.

[11] T. Yang *et al.*, "Fast and slow dynamic NBTI components in p-MOSFET with SiON dielectric and their impact on device lifetime and circuit application," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2005, pp. 92–93.

[12] G. Chen *et al.*, "Dynamic NBTI of p-MOS transistors and its impact on device lifetime," *IEEE Electron Device Lett.*, vol. 23, no. 12, pp. 734–736, Dec. 2002.

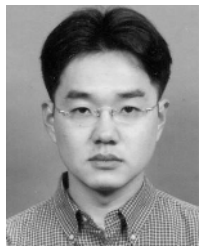
[13] M. Denais *et al.*, "On-the-fly characterization of NBTI in ultrathin gate oxide PMOSFET's," in *Proc. IEEE Int. Electron Devices Meet.*, Dec. 2004, pp. 109–112.

[14] T. Kim, J. Liu, R. Persaud, and C. H. Kim, "Silicon odometer: An on-chip reliability monitor for measuring frequency degradation of digital circuits," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2007, pp. 122–123.

[15] R. Fernández *et al.*, "AC NBTI studied in the 1 Hz—2 GHz range on dedicated on-chip circuits," in *Proc. IEEE Int. Electron Devices Meet.*, Dec. 2006, pp. 337–340.

[16] M. Denais *et al.*, "Paradigm shift for NBTI characterization in ultra-scaled CMOS technologies," in *Proc. IEEE Int. Reliabil. Phys. Symp.*, Mar. 2006, pp. 735–736.

[17] K. O. Jeppson and C. M. Svensson, "Negative bias of MOS devices at high electric fields and degradation of MNOS devices," *J. Appl. Phys.*, vol. 48, no. 5, pp. 2004–2014, 1977.



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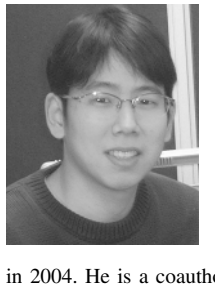

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