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Silicon photonics for telecom and data-com applications

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In recent decades, silicon photonics has attracted much attention in telecom and data-com areas. Constituted of high refractive-index contrast waveguides on silicon-on-insulator (SOI), a variety of integrated photonic passive and active devices have been implemented supported by excellent optical properties of silicon in the mid-infrared spectrum. The main advantage of the silicon photonics is the ability to use complementary metal oxide semiconductor (CMOS) process-compatible fabrication technologies, resulting in high-volume production at low cost. On the other hand, explosively growing traffic in the telecom, data center and high-performance computer demands the data flow to have high speed, wide bandwidth, low cost, and high energy-efficiency, as well as the photonics and electronics to be integrated for ultra-fast data transfer in networks. In practical applications, silicon photonics started with optical interconnect transceivers in the data-com first, and has been now extended to innovative applications such as multi-port optical switches in the telecom network node and integrated optical phased arrays (OPAs) in light detection and ranging (LiDAR). This paper overviews the progresses of silicon photonics from four points reflecting the recent advances mentioned above. CMOS-based silicon photonic platform technologies, applications to optical transceiver in the data-com network, applications to multi-port optical switches in the telecom network and applications to OPA in LiDAR system.

Keywords: silicon photonics; integration of photonics and electronics; CMOS process-compatible fabrication; optical interconnect transceiver; optical multi-port switch; optical phased array

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Introduction

Silicon photonics is a contemporary favorite in recent photonic network. Originated from the strong demand of explosively expanding network traffic, optical interconnection in the telecom/data-com now inevitably requires the silicon photonic platform to have excellent optical properties of the silicon in the mid-infrared spectrum.

To begin with, what is the network traffic like? How did the network traffic among human beings progress in its history? A newspaper article[1] (Fig. 1) provides a certain kind of answer: The ancient network traffic begins with mural painting in a cave (BC ~ 40,000) and the birth of paper (AD 105). Through the appearances of movable type printing (~1450) and telephone (1876), the article takes three historical happenings, i.e., TV broadcasting (1936), Internet (1969) and World Wide Web (WWW) (1993) as the dawn of modern traffic in the telecom era. Highlight in the article is a forecast for the vast change of the global traffic volume per year from ~ 6 Exa-byte (6×10^{18} byte) in 2000 to ~ 40 Zetta-byte (~ 4×10^{22} byte) in 2020. Additionally, a future-forecast organization, Yole Développement, also reports similar data every year. The explosive growth involves the contributions of several communication systems and technologies in the optical telecom network, as shown in Fig. 2, since 1980s[2]. Representative innovative technologies include planar light-wave circuit (PLC), arrayed waveguide grating (AWG), optical fiber amplifier (OFA), dense wavelength division multiplexing (DWDM), re-configurable optical

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add-drop multiplexing (ROADM) and digital coherent technique.

Fig. 1 | History of the traffic among human beings[1].

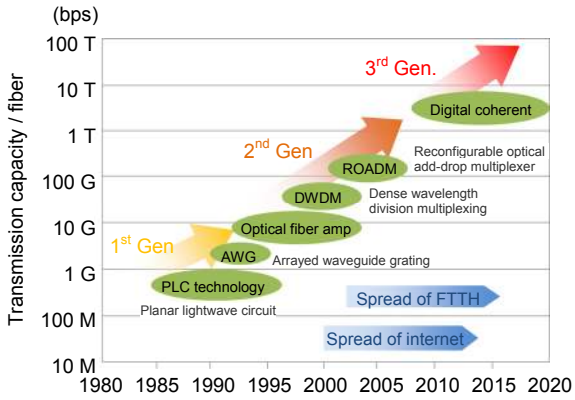


Fig. 2 | Progresses in the optical communication network[2].

For the device technologies in 1980s, III-V compound semiconductor based laser, photo-detector and other active devices have played important roles in the progress of the photonic network. III-V based optoelectronic integrated circuit (OEIC) was first developed in 1980s. However, full scale of photonic device integration has started with the pioneering work on silicon photonics (hereafter referred to simply as Si photonics) by Soref and Bennett, in the late 1980s and early 1990s[3]. Initial motivation for works on the Si photonics is the compatibility with the mature complementary metal oxide semiconductor (CMOS) manufacturing with low-cost and mass-market applications. Another important motivation is the availability of high-quality Si-on-insulator (SOI) wafers as an ideal planar waveguide platform, capable of strong optical confinement based on the high index contrast between Si (n = 3.45) and SiO_2 (n = 1.45). The latter motivation makes it possible to scale photonic devices down to hundreds of nanometer level. Such nano-scale dimensions are strongly required for true compatibility with large scale integration (LSI) processing.

Luxtera challenged pioneering integration of the photonic devices using the SOI CMOS process in 130 nm node[4–6]. Figure 3 shows the first demonstration of an optical grating connected to Si waveguides to show an efficient coupling (66 % at 1550 nm) of an optical single-mode fiber to nanoscale Si waveguides, thus mitigating the difficulty induced by the mode-size mismatch between them. This work has been widely recognized as the dawn of Si photonics, and they are now key devices for next-generation telecom and data-com interconnects for bringing the advantages of integrated photonics, i.e., high data densities and long transmission distances as well as the low manufacturing costs accompanied by CMOS compatibility.

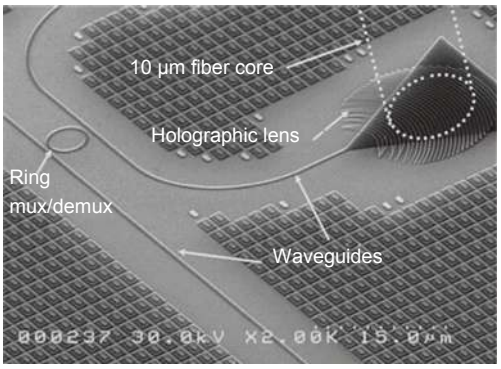


Fig. 3 | Demonstration of the first optical grating connected to silicon waveguides by Luxtera. Figure reproduced from ref.[6], under a Creative Commons Attribution License.

For about ten years from early 2000 until middle 2010s, excellent reviews and roadmap on the Si photonics technologies have been reported[5–11]. These reviews have introduced a wide range of hybrid and monolithic integration of Si photonic active/passive elements and also early applications to telecom and data-com areas. Correspondingly, this paper quickly briefs the imprints of the Si photonic devices, then lays great emphasis on the recent applications such as Si photonic interconnect transceivers in the data-com system and Si photonic multi-port switches in the telecom network.

Section 2 surveys the progress of Si photonic platform technologies including CMOS process based heterogeneous integration of passive/active photonic elements. Section 3 reviews the remarkable progresses in two-decades of Si photonic transceivers applied to the data-com interconnect. Section 4 introduces the recent innovative activities on multi-port Si photonic switches for the ROADM and optical phased arrays for light detection and ranging (LiDAR) system. Section 5 summarizes these results together with challenges and perspectives of Si photonic platforms and future applications.

Progress of Si photonic platform

CMOS process-compatible Si photonics fabrication

Integration of photonic components into a single chip has long been expected for practical integrated optics. In the conventional silica-on-Si technology, the waveguide was formed in a silica layer with doped phosphor or germanium atoms[12] or in a silicon oxy-nitride (SiON) layer[13]. On the other hand, SOI provides an excellent platform for Si/SiO_2 waveguides caused by a large refractive index contrast between Si (n = 3.45) and SiO_2 (n = 1.45), thus enabling strong optical confinement in the waveguides down-sized to approximately 0.1 μm^2.

In 2004, Vlasov et al. demonstrated the Si photonic waveguide on the SOI substrate[14]. Owing to the small sidewall surface roughness using a standard CMOS fabrication line using 200 mm wafers, minimal propagation losses of 3.6 dB/cm for the TE polarization as well as the 90° bending losses of 0.086 dB and 0.013 dB for bending radii of 1 μm and 2 μm, respectively, were reported at 1.5 μm wavelength. Figures 4(a) to 4(c) show scanning electron microscope (SEM) images of a single-mode strip waveguide with 445 × 220 nm core cross-section at different orientations. Bending loss spectra with radii of 5 μm, 2 μm and 1 μm were also measured for TE and TM modes, as shown in Figs. 4(d) and 4(e). The TM mode in a small radius bend degrades the bending loss at longer wavelengths, while the TE mode shows almost flat loss spectra in less than 1550 nm wavelength region. These results realize ultra-dense photonic integrated circuits on a single Si chip.

Heterogeneous integration of laser-on-Si platform

Integrated Si photonic platform includes on-chip active elements such as light source, modulator and detector as well as passive elements such as coupler, filter, grating and so on.

Among active Si photonic elements, Si nano-laser is difficult in principle because of inefficient radiative recombination due to its in-direct bandgap. In alternative direct bandgap III-V semi-conductors like gallium arsenide (GaAs), the bottom of the conduction band and the top of the valence band coincide in the wave vector axis, thus enabling efficient radiative recombination. Nevertheless, Si exhibits many excellent properties: (i) extremely high purity and low defect density, (ii) availability of the state-of-the-art CMOS technology, (iii) high thermal conductivity valuable for an active device substrate. These advantages allow for low-loss Si waveguides, one order of magnitude lower than the compound semiconductor waveguides. Therefore, an electrically pumped efficient Si nano-laser has become a long-term challenge for making the most of aforementioned Si advantages. For this purpose, direct mount of III-V lasers on Si is a promising solution for on-chip semiconductor laser[10]. The first method of this type is chip-/wafer-bonding of the III-V laser on Si[15,16]. The second one is direct epitaxial growth of the III-V layer on Si or SOI supported by intermediate buffer layers such as germanium layer and strained super-lattices[17,18]. The third one is a combination of these approaches. Next, the first two approaches are overviewed.

Chip-/wafer-bonded III/V-on-Si laser

A chip-bonded hybrid III-V-on-Si laser has the advantage of minimizing the area of the III-V material[15] when compared to that of wafer bonding to form the SOI based Si photonic platform that has been demonstrated so far[16,19,20]. The wafer-bonding technology has the advantages over chip-bonded III-V laser while on an SOI

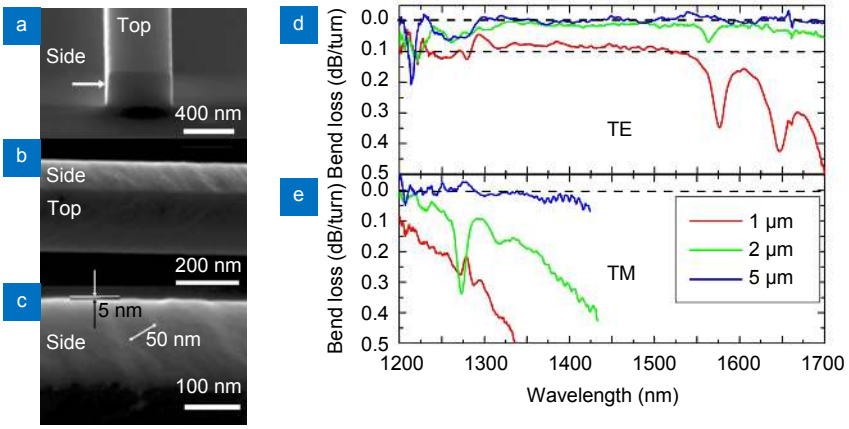


Fig. 4 | (**a–c**) SEM images of a single-mode strip waveguide cross-section at different orientations. (**d,e**) Bending loss spectra for TE and TM polarizations, respectively. Figure reprinted with permission from ref.[14], Optical Society of America.

host substrate. In the wafer-bonding, the Si passive light-wave circuits are patterned before the bonding process and the aluminum-gallium-indium arsenide (AlGaInAs) layers are processed after bonding using the standard techniques to fabricate III-V lasers[21]. After laser excitation, optical field is confined mainly in the Si waveguide with a fraction contained in the III-V quantum wells. The confinement factor can be significantly changed by altering the waveguide width. The advantage of this structure is that the optical mode can obtain electrically pumped gain from the III-V region, while being guided by the underlying Si waveguide region[22].

The vertical cavity surface emitting laser (VCSEL) is another promising light source for Si photonic circuits because of its small footprint, low manufacturing cost, low power consumption, capability of two-dimensional (2D) array and high data transmission rates[23–25]. Recently, an electrically pumped AlGaInAs-Si VCSEL with a high index-contrast grating (HCG) mirror on an SOI substrate has been reported. The HCG provides > 95% coupling efficiency between a surface-normal input and an in-plane SOI waveguide[26–27]. Figure 5(a) shows a schematic of the HCG VCSEL using an ultra-thin Si HCG optimized substrate as a bottom reflector in the laser cavity on a SOI substrate. The active layer AlGaInAs consists of compressively-strained quantum wells, and employs a proton implant defined aperture for current confinement, as illustrated in Fig. 5(b). The laser cavity, indicated by circulating red arrows in Fig. 5(a), is formed by the III-V distributed Bragg reflector (DBR) top mirror and the Si-HCG bottom mirror. The VCSEL operates at near infrared (IR) wavelengths with > 1 mW continuous wave (CW) power. The VCSEL is also capable of > 2.5 GHz 3-dB direct modulation bandwidth. These results present a promising approach for scalable and low cost integrated photonic circuits including active components.

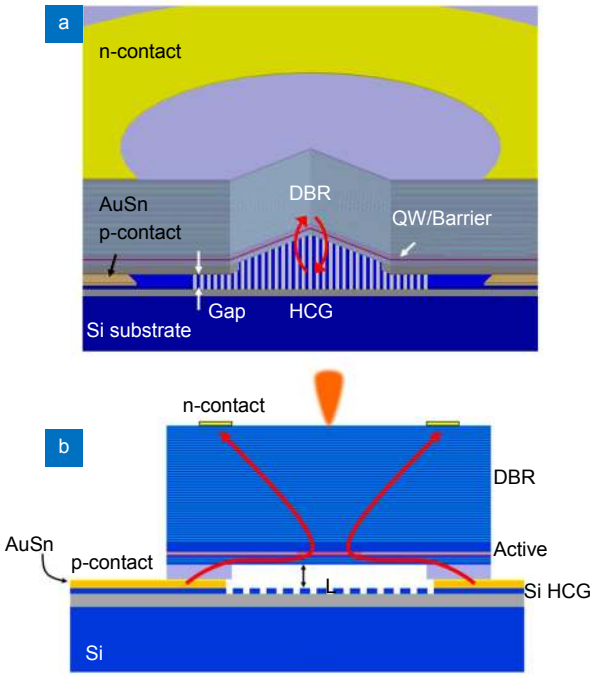


Fig. 5 | Schematic of VCSEL with Si HCG as bottom mirror. (**a**) Tilted-view of VCSEL cross-section with circulating red arrows indicating optical cavity. (**b**) The VCSEL employs a proton implant-defined aperture for current confinement, indicated by red curved lines between contacts. Figure reprinted with permission from ref.[27], Optical Society of America.

Epitaxial-grown III-V on-Ge/Si laser

In general, direct epitaxial growth of III-V compounds on Si substrates has considerable difficulty due to large lattice mismatch and different thermal expansion between III-V and Si. In contrast, Ge-on-Si (Ge/Si) has become a favorable technology for mitigating the lattice mismatch between GaAs and Si[28].

Recently, InAs/GaAs quantum dots (QDs) have been grown successfully on Ge/Si substrates[29]. Using this technology, the first CW operation of on-Si InAs/GaAs QD laser at room-temperature (RT) has been reported, as shown in Fig. 6. A Ge layer was grown on a GaAs buffer layer, resulting in the high-performance III-V QD laser monolithically grown on the Ge substrate[30,31]. Characteristics of the first RT CW operation of Si-based QD laser were J_{th} of 163 A/cm^2 at a wavelength of 1.28 μm using 20 μm-wide, 3~3.5 mm-long cavities.

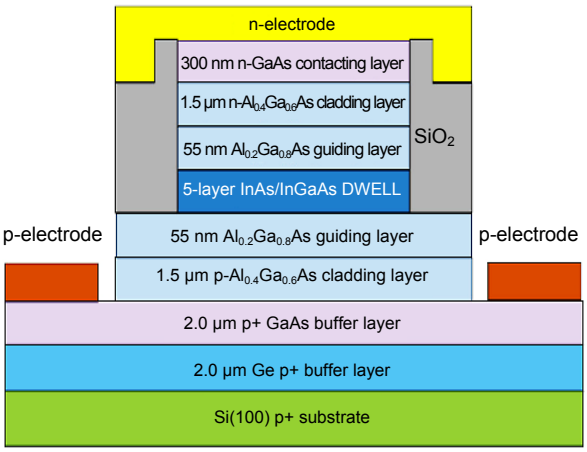


Fig. 6 | Schematic layer structure of an InAs/GaAs QD laser on a Ge-on-Si substrate. Figure reprinted with permission from ref.[31], Optical Society of America.

Heterogeneously integrated narrow-linewidth laser

Recent progress of optical communications with high speed and wide band-width requires narrow linewidth lasers for more complex modulation methods. For example, a tunable laser with a linewidth < 300 kHz is needed for a 16-quadrature amplitude modulation (QAM) format[32]. Komljenovic et al. have demonstrated a widely tunable narrow-linewidth semiconductor laser with monolithically integrated on-chip cavity using a Si photonics platform on an SOI substrate[33]. The gain section is sandwiched by loop-mirrors, constituting a 2 mm long cavity. The lasing wavelength is determined in the tuning section comprised of two ring resonators and a cavity phase section, all of which are controlled by thermal phase tuners. The external cavity is ~ 4 cm long and has its own phase adjustment and gain section. The external cavity is coupled on the side with the tuning section so that the tuning rings filter out any spontaneously emitted light from the extended cavity. The lasers are tunable over a 54 nm range from 1237.7 to 1292.4 nm. The measured linewidth in full tuning range is below 100 kHz and even ~ 50 kHz, a new record for narrow linewidth in a monolithically integrated widely-tunable laser design.

Integration of passive Si photonic platform

So far, on-Si passive photonic elements such as waveguides, couplers, multiplexers, polarization controllers, filters, resonators, etc. have been implemented[14,34]. Figures 7 show several SEM photographs of compact Si/SiO_2 waveguides. Figures 7(a) and 7(b) show multiply coupled micro-rings and their magnified ones with radii of only 1 μm, while Fig. 7(c) shows sharp-tapered waveguide. Their bending and propagation losses are less than 0.09 dB and 1 dB/cm, respectively[10,35,36]. Reference[37] also reports schematic design of multi-octave spectral beam combiner with integrated lasers utilizing Si and Si_3N_4 waveguides.

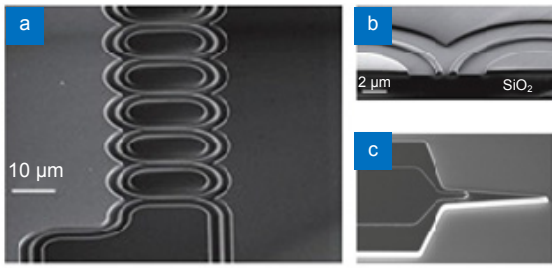


Fig. 7 | SEM photographs of nano-scale Si/SiO_2 waveguides. (**a**,**b**) Multiply coupled micro-rings and their magnified ones. (**c**) Sharp taper. Figure reprinted with permission from ref.[10], SPIE.

In the WDM system, an AWG is an essential optical component for multiplexing channels of several wavelengths into a single optical waveguide at the transmission end or de-multiplexing individual channels of different wavelengths at the receiving end. Figure 8(a) shows a schematic for the operating principle of the AWG. An optical signal consisting of multiple wavelengths in the input waveguide is diverged in an expanding free-propagation region (FPR) as an input star coupler. An array of waveguides (designed as a phased array) captures this diverging light, which then propagates and is focused at the end, i.e., at the input aperture of the output focusing FPR. This is because the length of array waveguides is selected so that the optical path length difference between adjacent waveguides equals an integer multiple of the central wavelength of the de-multiplexing. As a result, the field distribution at the beginning of the phased array is reproduced at the end and, in the focusing FPR, the light beam interferes constructively and converges at one single focal point on the focal line, as shown in the Fig. 8(a). If the wavelength is shifted from the central wavelength, the light beam is focused on a different position of the focal line in the image plane. Thus the field for each wavelength can be coupled into the respective output waveguide. As an extremely compact AWG chip demonstrated by Yaegashi's group[38], Fig. 8(b) shows a photomicrograph of the AWG with about 1.4 mm square, separating up to eight wavelengths at an optical frequency interval of 100 GHz. Figure 8(c) shows the filter spectral characteristics, indicating a low 1.2 dB loss and -16 dB crosstalk between wavelengths.

Another important optical component for the WDM system includes an optical-cavity based micro-ring resonator (MRR) filter with periodical Lorentzian spectral responses to select a series of resonance wavelengths. In general, the cavity should have a large free spectral range (FSR) to cover all the multiplexed channels. Many cascaded MRRs are convenient for an array with $N \times N$ elements to deal with N channels[39]. In general, a large wavelength window might be required for course WDM (CWDM) on-chip optical interconnects, and thus it is preferable to use MRR filters with an ultra-large FSR and a large tunable range of wavelength. Dai et al demonstrated the SOI-nanowire based MRR, in which the FSR increases from 17 nm to 58 nm for the bending radius reduced from R = 5 μm to R = 1.5 μm. When MRRs are used as tunable optical filters, modulators, switches, etc, the size reduction is effective for reducing the power consumption[40].

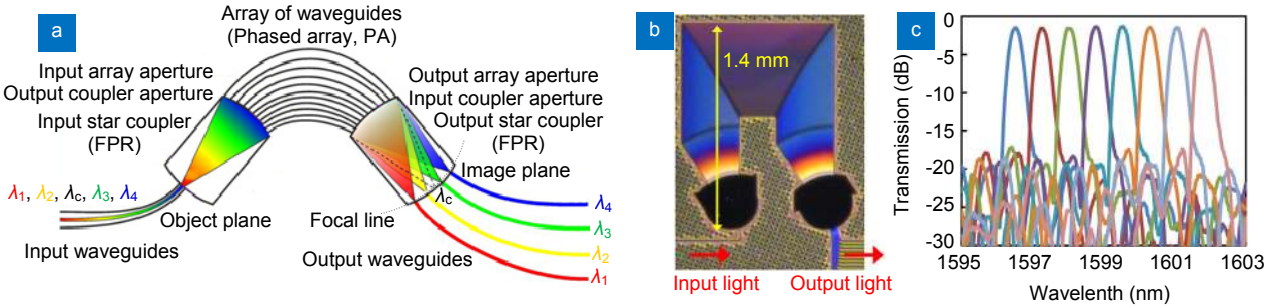


Fig. 8 | (**a**) Schematic showing the operating principle of the AWG. (**b**) Photomicrograph of the AWG with about 1.4 mm square and eight wavelength channels. (**c**) Filter spectral characteristics. Figure reprinted with permission from: (b,c) ref.[38], OKI Corporate.

Growing Si photonic foundries

Integrated Si photonic devices are produced by several manufacturing steps such as design, CMOS-process fabrication, packaging and testing by each special company (supply-chain). Table 1 shows the 2019 world ranking of semiconductor companies reported by marketing company Yole Développement[41]. In the table, a fabless company is the one that designs and sells hardware and semiconductor chips but outsources the fabrication of such chips and hardware, while a (pure-play) foundry (or just fab) is a factory that only manufactures devices such as integrated circuits without designing them. In late 2000s through early 2010s, the main Si photonics manufacturing foundries were represented by Luxtera, Intel, Cisco, etc. In *"Zero change" monolithic CMOS-processed Si photonic transceiver* Section, the new foundry, GlobalFoundry (GF), will be introduced as a typical foundry that manufactured "Zero change" monolithic CMOS-processed Si photonic transceivers. GF is the world's second-largest pure-play foundry with 2017 revenues estimated at $5.86 billion by market research company IC Insights, as shown in Table 2[42]. Since the function and scale of Si photonic platform have become more complicated and expanded year by year, the system of this production division and the role of the foundry will become more indispensable, as suggested in Table 2[42].

Table 1 | Silicon photonics supply chain for optical transceivers[41]**.** (Source: Silicon Photonics report, Yole Développement, 2020)

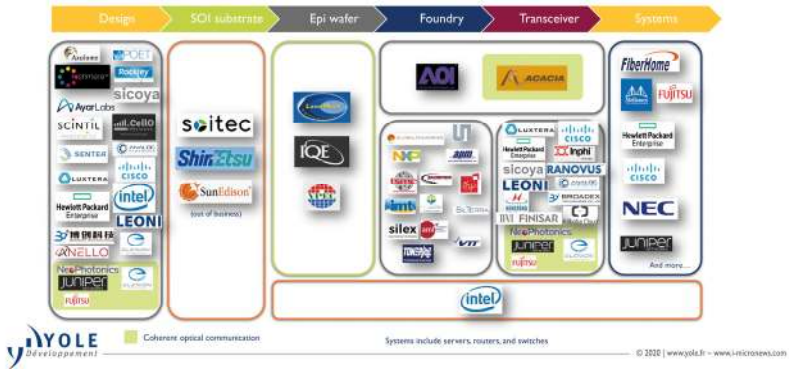


Table 2 | Major 2017 foundries (Pure-Play and IDM (integrated device manufacturer)). Table reprinted with permission from ref.[42].

2017 rank	2016 rank	Company	Foundry type	Location	2015 sales ($M)	2016 sales ($M)	2016/2015 change (%)	2017 sales ($M)	2017/2016 change (%)
1	1	TSMC	Pure-Play	Taiwan, China	26,574	29,488	11	32,163	9
2	2	GlobalFoundries	Pure-Play	U.S.	5,019	5,495	9	6,060	10
3	3	UMC	Pure-Play	Taiwan, China	4,464	4,582	3	4,898	7
4	4	Samsung	IDM	South Korea	2,670	4,410	65	4,600	4
5	5	SMIC	Pure-Play	China	2,236	2,914	30	3,101	6
6	6	Powerchip	Pure-Play	Taiwan, China	1,268	1,275	1	1,498	17
7	8	Huahong Group*	Pure-Play	China	971	1,184	22	1,395	18
8	7	Tower Jazz	Pure-Play	Israel	961	1,250	30	1,388	11
—	—	Top & Total	—	—	44,163	50,598	15	55,103	9
—	—	Top & Share	—	—	87%	88%	—	88%	—
—	—	Other Foundry	—	—	6,597	7,112	8	7,207	1
—	—	Total Foundry	—	—	50,760	57,710	14	62,310	8

*Includes Huahong Grace and Shanghai Huali.
Source: IC Insights company reports

Si photonic interconnect in data center and HPC

Pioneering Si photonic transceiver

Si photonics includes integrated optical and electronic components on single chip fabricated with a standard CMOS process. In the current interconnect in the data center and high-performance computer (HPC), the considerable amount of copper wires which connect different electronic components degrade the signal intensity due to the electrical resistance in the wire and have a limited maximum length. One possible solution for higher data rates over long distances is to replace electrical interconnection with an optical link, i.e., optical interconnection based on Si photonic transceivers. Figure 9 shows a general architecture of the Si photonic transceiver composed of a transmitter and a receiver as key elements of an optical link. The transmitter is constituted of an on-chip laser source, optical modulators and Si waveguides, while the receiver is constituted of on-chip photodetectors and electronics converting the data into electronic signals. Since the figure shows a four-channel WDM optical link, the transmitter output involves a multiplexer which combines four different-wavelength light beams and send them into a single interconnect waveguide, while the receiver input involves a de-multiplexer which separates and sends them into four different detectors.

A pioneering Si photonic transceiver with optical fibers was demonstrated in 2007 by Intel group, as shown in Fig. 10[7,43]. The figure explains a 50 Gb/s optical link module. In Fig. 10(a), a transmitter chip with four hybrid InP/Si lasers emits four different wavelength CW laser beams, which propagate into 12.5 Gb/s-encoded optical modulators. These four beams are combined in a multiplexer and sent into a single optical fiber for a total data rate of 50 Gb/s. At a receiver, as shown in Fig. 10(b), the chip separates four light beams in the de-multiplexer and sends them into photodetectors. Development of the chip achieving data rate of 100 Gb/s or further is going on.

Luxtera, as shown in Fig. 3 as a pioneering Si photonic platform company, reported a 10 Gb/s transceiver with a four-channel WDM transmitter/ receiver in 2010[4]. It was fabricated with a 90 nm SOI CMOS process. The chip includes monolithically integrated wavelength filters, photodetectors, electronic amplifiers and drivers except for four InP lasers which are flip-chip bonded onto the Si substrate. As shown later, these kinds of on-chip Si photonic transceiver have been most widely developed by several companies and foundries,

Progress of Si photonic transceiver

Si photonic interconnect forecast

Si photonics is now widely accepted as a key technology in the next-generation telecom and data-com systems. A. Zilkie overviews[9] that the potential of integrated Si photonics was recognized in the first studies of SOI waveguides in 1985[44,45], and their commercialization started in

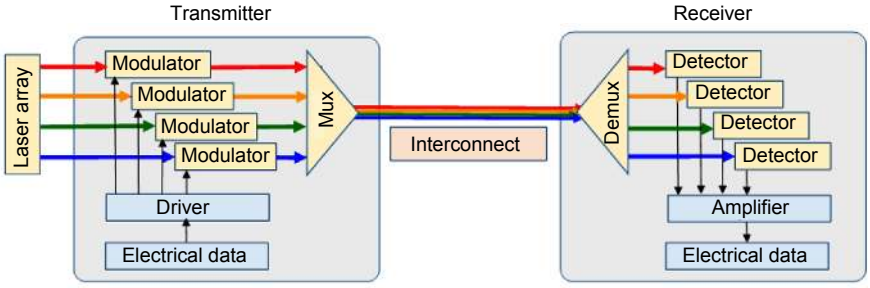


Fig. 9 | Basic block diagram of an optical link including a transmitter and receiver.

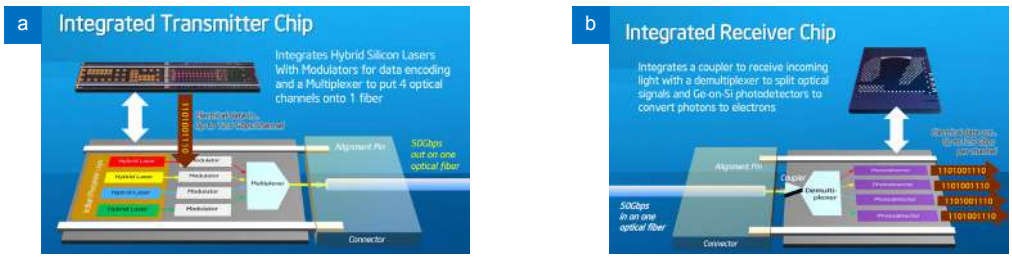


Fig.10 | 50 Gb/s Si photonics transmit module. (**a**) and (**b**) are transmitter and receiver, respectively, with wavelength division multiplexing. Figure reproduced from ref.[43], Intel.

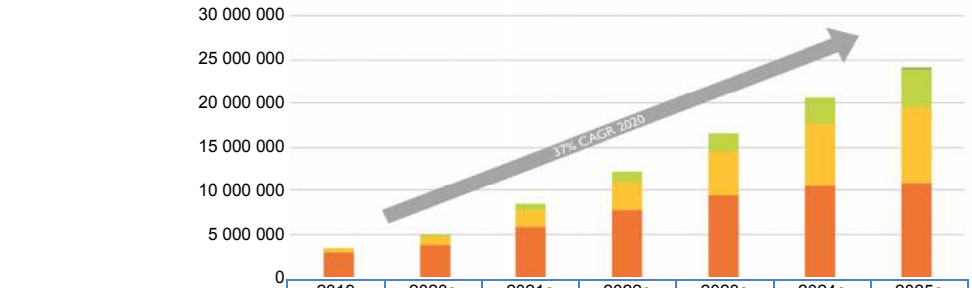
1989 by Bookham Technology Ltd[46]. Practical applications of Si photonics first started in sensor areas in the 1990s and afterwards their commercialization changed to WDM telecomm products. The practicality for data-com market was recognized further with the realization of SOI-waveguide p-i-n junction modulators[45] and Ge- and SiGe-based photodetectors and modulators[47,48]. Pioneering Si photonics companies such as Luxtera[49], Kotura (now Mellanox)[48] and Acacia Communications[50] are producing Si photonic 100 Gb/s transceivers for data center/HPC interconnects and telecom optical transport markets. Figure 11 shows Si photonics 2019–2025e forecast in the optical data center market, where the mega data center/HPC companies are planning for large-scale deployment of Si photonics based interconnects in the hardware replacement cycles starting in ~2019[51]. Metrics in ref.[51] indicated that the increase of the adoption in the data center and other data-com markets results in low cost per data lane (~$1/Gb/s), low power consumption per data lane (few pJ/bit), and good manufacturability and reliability.

Taking note to the process integration and its future evolution, Boeuf reviews in ref.[9] that the evolution of Si photonics in the next decade will require the implementation of several new process steps. He mentions that an efficient device optimization can be first achieved from a front-end perspective by mixing several types of waveguides like strip and rib waveguides with various SOI thicknesses. New material layers are integrated for mitigating the intrinsic weaknesses of Si such as thermal sensitivity of the refractive index and indirect-band-gap originated inefficient radiation. "Midex" materials having refractive index between ~1.6 to 2.5 and able to mitigate Si thermal properties issues will be developed. Regarding the integrated light source, the III–V/Si hybrid laser has already been reviewed in *Chip-/wafer-bonded III/V-on-Si laser* Section. Nevertheless, the monolithic integration of the hybrid laser into the Si photonics transceiver will require further innovative developments. From the interconnect perspective, on the other hand, development of through-Si-via (TSV) will enable the Si photonics interposer technology which allows for the integration of complex electronics together with the driving electronics of the photonics.

In the next part, advanced approaches of IBM toward Si photonic multi-chip-module are reviewed.

IBM roadmap on Si photonic multi-chip-module

Initially, Si photonic transceivers have mainly progressed in the data center and HPC areas. Within the data center, transceivers are located at the edge of the packaging board in each server, resulting in large distances between the optical component and the processor chip. IBM has been developing packaging designs to solve the issue for fifteen years under the strategy of Si photonic die to be integrated directly into the processor module. Patterson et al. have reviewed the IBM strategy of Si photonic multi-chip-module (MCM) and the first CMOS integrated Si photonics chip demonstrated in 2015[52]. Figure 12(a) shows a Si photonic die designed to arrange a waveguide array for efficient coupling between light wave and electronic components via an array of flip-chip bumps to support electrical signals. Laser dies are attached to the Si photonic chip through flip-chip bumps. Figure 12(b) shows a ball grid array (BGA) substrate with a central logic die, two hybrid memory cubes (HMCs) and associated CMOS devices. Alternative designs are illustrated in Figs. 12(c) and 12(d). In these cases, the logic die and high-bandwidth memory (HBM) stacks are mounted directly onto a high-density interposer to link the logic,



	2019	2020e	2021e	2022e	2023e	2024e	2025e
Co-packaged photonic engines	0	0	0	0	0	0	120 937
200G/400G and beyond	0	247 982	677 909	1 227 094	1 983 963	3 100 987	4 353 730
100G CWDM4	514 312	942 333	1 948 988	3 313 155	5 092 171	7 028 904	8 707 459
100G PSM4	2 937 837	3 791 554	5 846 963	7 730 695	9 456 890	10 543 356	10 884 324

Fig. 11 | Silicon photonics shipments, for datacenter (in units) 2019-2025e. (Source: Silicon Photonics report, Yole Développement, 2020)

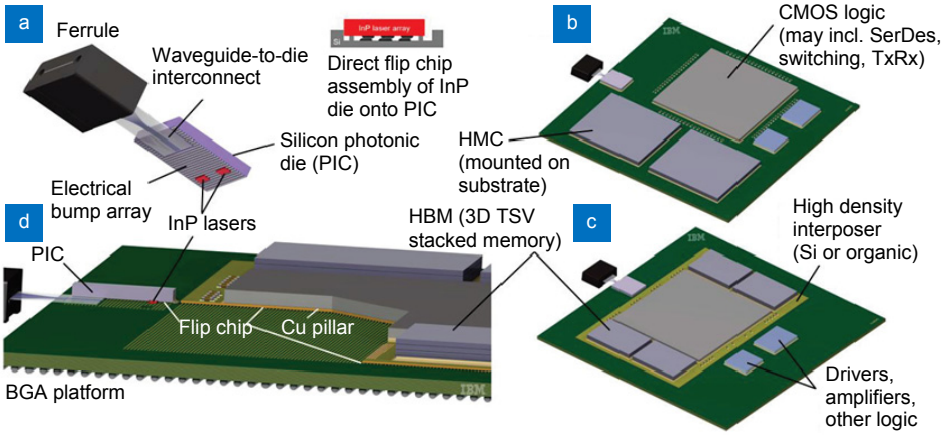


Fig. 12 | Si photonic MCM. (**a**) Photonic integrated circuit (PIC) with flip-chip mounted laser die and edge-coupled waveguide. (**b**) Logic, HMC and PIC mounted directly to a BGA substrate. (**c**) Logic and HBM mounted on a high-density interposer with micro-bumps. (**d**) Cut-away revealing copper pillar, flip-chip, BGA and optoelectronic interconnections. Figure reprinted with permission from ref.[52], IBM.

memory and photonic integrated circuit closely.

Figure 13(a) shows a photograph of the first CMOS integrated CWDM Si photonics chip demonstrated in 2015. The chip is capable of transmitting and receiving four-wavelength channels, each operating at 25 Gb/s on a single die. The die was manufactured by 90 nm CMOS process technology, containing modulators, Ge photodetectors, and ultra-compact WDMs. Figure 13(b) shows a die with an array of 100 μm lead (Pb)-free flip-chip bumps on a 200 μm pitch. Figure 13(c) shows transmitter and receiver elements along with their eye diagrams, indicating a clean and high quality response. The lasers are connected off-chip with the optical signals. Four wavelength signals are multiplexed into 100 Gb/s fiber ports. The updated chip design allows for up to twelve such fiber ports, thus enabling 600 Gb/s bi-directional data rates from a single optical transceiver. The demonstration was to push 100 Gb/s data speeds over a range of up to 2 km as required by large data center environments[53].

In recent years, two innovative progresses on the new types of Si photonic transceiver technologies have been reported: One is a “Zero change” monolithic CMOS processed Si photonic transceiver and the other is a fingertip-size Si photonic interconnect for ultra-short optical links. Their characteristics are reviewed in the following.

“Zero change” monolithic CMOS-processed Si photonic transceiver

In 2018, Stojanov et al. reported the most advanced monolithic Si photonic platforms in the state-of-the-art SOI CMOS processes as the world’s first micro-processor with photonic I/O[11]. They realized record high energy-efficiency/speed in transmitters as well as the highest level electronic-photonic integration. It is called the “Zero-change" Si photonic platform implemented using an unchanged commercial 45 nm CMOS SOI process[54]. As

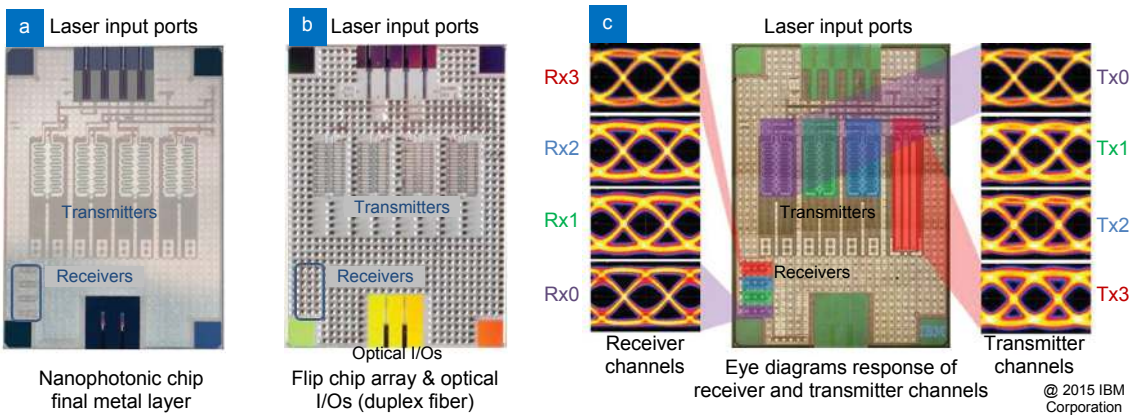


Fig. 13 | IBM Si CWDM 4 × 25 Gb/s die. (**a**) Photograph of CMOS integrated Si photonics chip. (**b**) Die with an array of 100 μm Pb-free flip-chip bumps on a 200 μm pitch. Two optical I/Os are seen at the bottom of the die. (**c**) Transmitter and receiver elements along with their eye diagrams Figure reprinted with permission from ref.[52], IBM.

shown in Fig. 14, all photonic devices are designed to follow the purely-electrical foundry design flow without any modifications to the native process[11,55,56]. Optical devices are implemented in the sub 100 nm thick high-index crystalline Si (c-Si) layer. The first six metal layers on top of photonics structures have been eliminated to prevent metallic optical losses. Since the buried oxide (BOX) layer is thin, the Si substrate is removed also to reduce the waveguide optical loss to approximately 3 dB/cm in it[55]. Light is coupled to the chip via vertical grating couplers. Active devices including micro-ring modulators and photodiodes are implemented using existing source/drain and well-implanted doping levels as well as the available SiGe in this process.

Figure 15 presents the demonstrated processor with photonic I/O using the 45 nm "Zero-change" platform. Ultra-power-efficient ring resonator (RR) based Si photonic links, with millions of transistors and hundreds of photonic devices fabricated on the same chip, are aimed to improve processor-memory link bandwidth[11,56]. The system-on-chip (SoC) in Fig. 15(a) has a dual-core reduced instruction set computer-V (RISC-V) processor[11,57], 1 MB static random access memory (SRAM) based cache memory, and DWDM optical I/Os, as illustrated in Fig. 15(b). Figure 15(c) shows the key photonic devices of an optical link implemented by this technology.

For passive optical elements, waveguides are built in the sub-100 nm thick c-Si body layer by blocking all transistor body dopants to lower the optical loss. In the 45 nm platform, the measured loss is 3.7 dB at 1280 nm and 4.6 dB at 1550 nm[55]. For coupling between the on-chip waveguide and optical fiber, vertical grating couplers have been developed using two layers of c-Si and transistor gate poly-Si for designing uni-directional grating

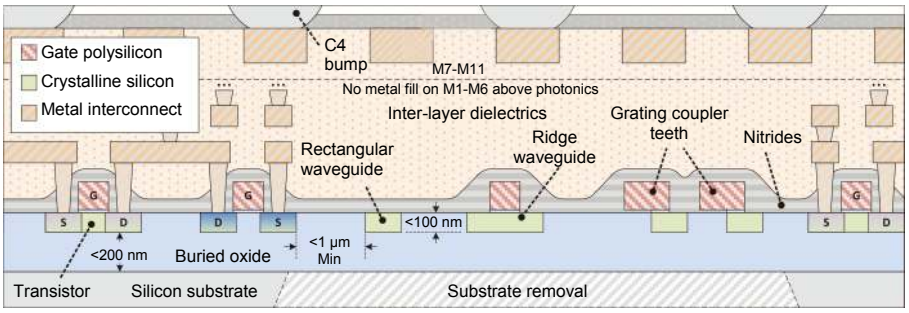


Fig. 14 | Schematic cross-section of 45 nm SOI CMOS process based Si photonic platform with photonic as well as electronic devices at the front end and bump at the back end. Figure reprinted with permission from ref.[56], IEEE.

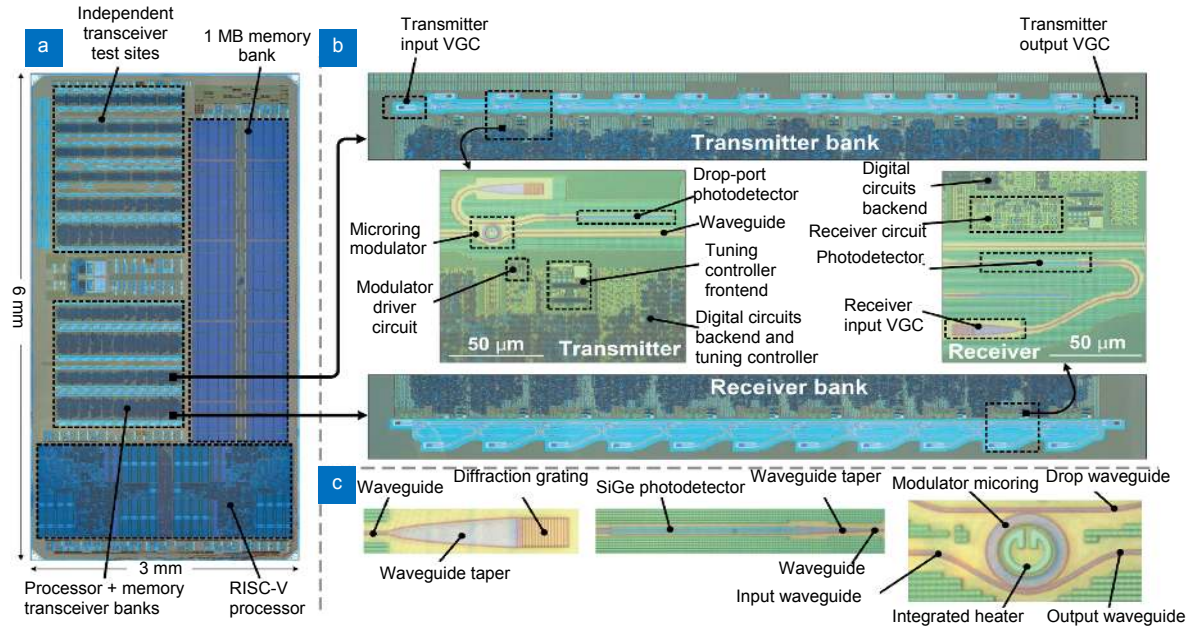


Fig. 15 | Photograph of "Zero-change" SOI platform die. (**a**) SoC including a RISC-V processor, SRAM based cache memory and DWDM optical I/Os. (**b**) WDM transceivers. (**c**) Key photonic devices of an optical link. Figure reprinted with permission from ref.[11], Optical Society of America. Development timeline in Fig. 3, ref.[11] has been omitted here.

couplers. 1.5 dB optical loss has been achieved[58].

For active optical elements, micro-ring modulators (MRM) have been fabricated by placing interleaved p and n junctions along the ring cavity, as shown right in Fig. 15(c). Resonance wavelength can be modulated by changing the carrier density in the depletion regions of interdigitated junctions via carrier-plasma effect in silicon[3]. 5 μm-radius active micro-rings achieved intrinsic Q-factors of 18 k and up to 10 k loaded Q-factors with 3.2 THz FSR in telecom O-band[11]. For photodetectors fabricated in the die, refer to ref.[11] for details.

As compared with the well-known Mach-Zehnder modulator (MZM) with mm size, the MRM with compact footprints fits for high-speed and energy-efficient optical transmitters, so that it enables DWDM for large-scale integrated systems with high bandwidth densities in the Tb/(s·mm^2) range. Experimental results using the MRM-based transmitters show two orders of magnitude improvement in energy efficiency as compared with currently popular MZM based transmitters. Figure 16(a) shows a photograph of a 40 Gb/s non-return-to-zero (NRZ) transmitter die in the 45 nm SOI CMOS. The modulator and driver stage consume only 40 fJ/b and the total energy consumption and area are 0.7 pJ/b and 0.03 mm^2, respectively[11]. Figure 16(b) shows the measured NRZ eye diagrams at 40 Gb/s with the extinction ratio of 3 dB and insertion loss of 4.7 dB. For data-rates higher than the modulator bandwidth, 40 Gb/s pulse amplitude modulation (PAM)-4 transmitter has been demonstrated[11,59]. MR based optical transceivers can be used to build DWDM links to achieve Tb/s aggregate bandwidths over a single fiber. The latest performance and results of the "Zero-change" Si photonics platforms presented above indicate that the 45-32 nm SOI CMOS processes provide a "sweet-spot" for adding photonic capability and enhancing integrated system applications beyond the Moore-scaling[11,59].

Fingertip-size Si photonic interconnect for ultra-short optical links

Recently, field-programmable gate arrays (FPGAs), having a large input/output (I/O) bandwidth over 1 Tb/s, are attracting much attention, in particular, in the data center and HPC for supplementing the deficient processing speed of current central processing units (CPUs) and/or graphic processing units (GPUs). To satisfy these bandwidth requirements, a small footprint optical module with high bandwidth density, low power consumption and high temperature durability is required to be mounted around the FPGA. To solve this problem, a Si photonics based fingertip-size optical module named "optical I/O core" has been developed recently by the PETRA project. They demonstrated 300 m transmission at 25 Gb/s per channel with the FPGA board mounted by the optical I/O cores[60,61].

Figure 17(a) shows a whole part of the optical I/O core chip and layout of optical and electrical I/O's as well as integrated circuit mounting areas, respectively[61]. It has a small footprint of 5 mm × 5 mm and a maximum capacity of 300 Gb/s (25 Gb/s × 12 channels).

Figures 17(b) and 17(c) show cross-sectional pictures of a receiver and a transmitter, respectively. The transmitter includes optical waveguides, MOS-capacitor type Si optical Mach-Zehnder interferometer (MZI) modulator and grating coupler (GC), while the receiver includes a Ge-photodetector (PD) as well as waveguides. Si photonics constituting the core is fabricated using a 300 mm SOI wafer process. ArF-immersion lithography enables low-loss (1.28 dB/cm for the O-band) and high-uniformity optical waveguide[62].

After completing the Si photonics integrated circuit, a Fabry-Perot laser diode (FP-LD) and optical pins were assembled into the optical I/O core. Figure 18 shows a cross-sectional view of the Si photonics platform in part on which the FP-LD is assembled[60]. By means of

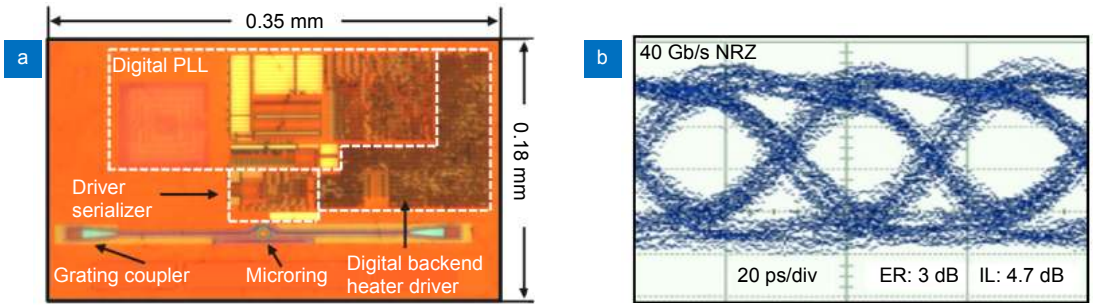


Fig. 16 | 40 Gb/s transmitters. (**a**) Micrograph of the 40 Gb/s NRZ transmitter. (**b**) NRZ transmission eye-diagram. Figure reprinted with permission from ref.[11], Optical Society of America. Figs. 7(b) and 7(d) in ref.[11] have been omitted here.

designing alignment marks on the LD and Si platform, horizontal and vertical misalignments between the LD and the Si platform remained ± 0.5 μm and ±0.1 μm, respectively. For selecting the LD on Si photonics, InAs/GaAs quantum dot (QD) FP-LDs were evaluated to be superior to InGaAsP quantum well FP-LDs in high temperature operation and high optical feedback tolerance.

Another important optical component in the optical I/O core is a newly developed optical pin, as shown in Figs. 17(c) and 17(d). The optical pin is a 3D resin polymer waveguide used in place of an optical lens for connecting the grating coupler or the Ge-PD with multimode fiber (MMF). Since the FP-LD is not temperature-controlled, the output wavelength from the core is seriously temperature-dependent (0.6 nm/°C) and the radiation angle from the grating coupler is also fluctuated at 0.083 degree/nm. Nevertheless, the optical pin has a high refractive index contrast between the core and cladding, so that the varied radiated light from the grating coupler can be enclosed within the core[63]. This means that the calculated optical pin-GI50 MMF misalignment tolerance with 1 dB excess loss is larger than 10 μm in a temperature range from -45 °C to +85 °C. The result significantly contributes to the excellent overall characteristics of the optical I/O core, as shown later. It also provides an easy connection between the optical I/O core and the MMF.

Before mounting the optical I/O cores around the FPGAs, temperature dependence of eye patterns and bit error rates (BERs) at 25 Gb/s of the optical I/O core were evaluated. Clear eye patterns from 25 °C up to 85 °C and BERs less than 10^{-12} at 20 °C and 85 °C were demonstrated[64]. These results were achieved owing to the QD LD and optical pin technologies. The transmission characteristics of the optical I/O core were also evaluated using two types of MMFs, as shown in Fig. 19. One is a corning clear curve LX MMF[65] specialized for the O-bands. The other is a conventional OM3 fiber used in 850 nm wavelength. The former MMF enables transmission up to 300 m at 25 Gb/s sufficient for applications in the data center system, while the latter OM3 fiber enables 30 m transmission without an equalizer or 60 m transmission with an equalizer at 25 Gb/s sufficient for applications in the HPC system. Finally, the performance of the optical I/O core module mounted around the FPGA board was evaluated. On the board, maximum 24 transceiver and receiver channels of optical I/O cores with a capacity of 1.2

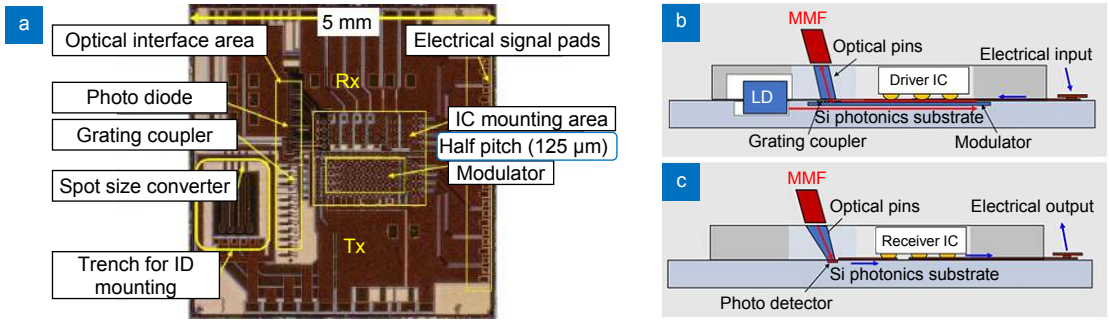


Fig. 17 | (**a**) Whole part of optical I/O core chip. (**b, c**) Cross-sectional views of receiver and transmitter, respectively. Figure reprinted with permission from ref.[61]. AIOCORE.

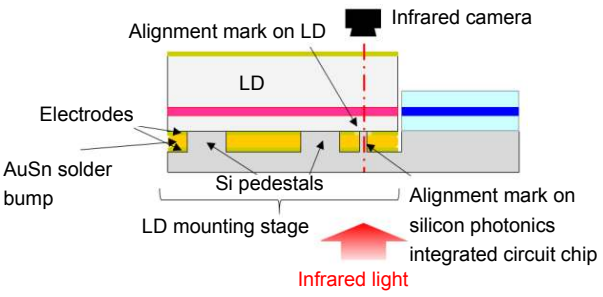


Fig. 18 | Cross-sectional view of Si photonics integrated circuit with FP-LD. Figure reprinted with permission from ref.[60], The Institute of Electronics, Information and Communication Engineers.

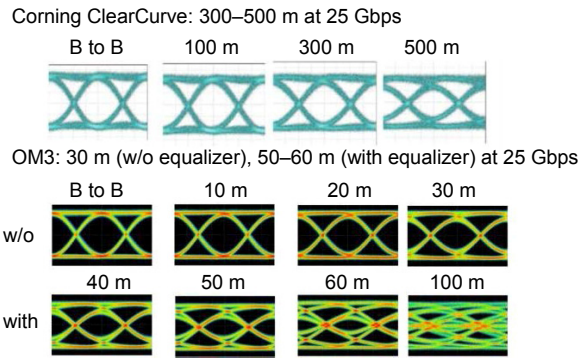


Fig. 19 | Transmission characteristics of the optical I/O core with two kinds of MMFs. Figure reprinted with permission from ref.[60], The Institute of Electronics, Information and Communication Engineers.

Tb/s were mounted around FPGA. The FPGA boards were connected to the 300 m MMF and 25 Gb/s signals per channel were transmitted. BERs less than 10^{-12} with good eye patterns were successfully obtained. The result shows that almost no degradation occurs in BERs at the simultaneous many-channel operation in the optical I/O core.

In conclusion, the Si photonics based fingertip-size optical I/O core with features of high bandwidth density, low power consumption and high temperature durability allows for 300 m transmission at 25 Gb/s per channel with the modules mounted around FPGA. These results will contribute to high bandwidth density and low power consumption interconnects among FPGAs in data center and HPC systems[60].

Si photonic switch for innovative applications

Architecture of photonic switches

Optical switches are essential elements for constructing integrated Si photonic circuits in the photonic network. For designing integrated multi-port optical switches, physical mechanisms of the switch and topologies of the switch fabrics should be considered. Typical switching mechanisms include thermally and electrically operated phase modulation in inter-ferometric structures like Mach-Zehnder interferometer (MZI) and micro-ring resonator (MRR), and signal amplification or absorption in semiconductor optical amplifiers (SOAs)[66]. They will be discussed later and here, typical switch fabric topologies (with $N \times N$ port counts) are introduced. Metrics of the performance in each topology are blocking characteristics, crosstalk suppression, number of cascading stages and total number of switch cells. Commonly used topologies include crossbar, path-independent-loss (PILOSS), Beneš and switch-and-select (S&S), as shown in Fig. 20, all of which support non-blocking connections[67]. The crossbar topology has the most cascading stage number, resulting in a large path-dependent loss. The PILOSS is preferred when uniform performances across all paths are necessary. While the first-order crosstalk is inevitable, although not all the switch cells carry two signals at once[68]. The Beneš architecture has the smallest number of cascading stages as well as switching cells, while it suffers from situation of two traversing signals, resulting in the first-order crosstalk. The S&S topology blocks first-order crosstalk, but it requires the largest number of switch cells. Moreover, the central shuffle network becomes complex. The selection of topology depends on the switching performance.

Si photonic switch in telecom network

Architecture of CDC-ROADM system

In the recent photonic network, re-configurable optical add-drop multiplexing (ROADM) has brought new flexibility and scalability to the conventional static photonic transport networks[69]. Multi-degree ROADM was developed after the introduction of the basic 2-degree ROADM in order to realize mesh-based network topologies[70].

Figures 21(a) and 21(b) show examples of multi-ring network and 4-degree ROADM node configurations connecting two ring networks, respectively. Incoming WDM signals from the degree-1 input fiber are delivered to the drop-side optical switch. In Fig. 21(b), the optical switch selects the optical path to degree 2 (red), degree 3 (orange), or degree 4 (green) for each wavelength signal. When transponders (upon receiving signals, emitting different signals in response) at this node receive these signals, the optical switch selects the drop path (purple) to deliver the signals to another optical switch, namely a transponder aggregator (TPA). Then, the TPA allocates the input signals to each desired transponder for each wavelength channel. On the add-side, an output signal from the transponder is routed to an add-side optical switch via an add-side TPA. The add-side optical switch collects add signals and the signals that pass through this

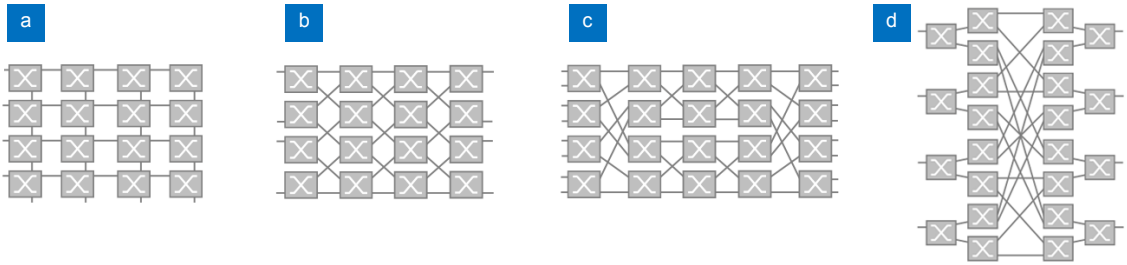


Fig. 20 | Schematic of typical optical switch topologies. (**a**) Crossbar. (**b**) PILOSS. (**c**) Beneš. (**d**) Switch-and-select. Figure reprinted with permission from ref.[66], Optical Society of America.

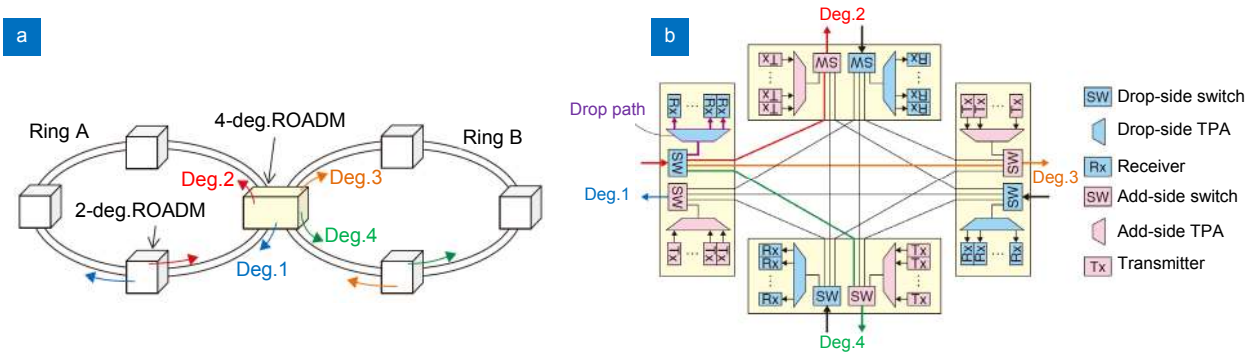


Fig. 21 | (**a**) Example of multi-ring network. (**b**) 4-degree ROADM node configuration connecting two ring networks. Figure reprinted with permission from ref.[69], NTT Technical Review.

node are then launches them into the output fiber. Today, in addition to the multi-degree function, colorless, directionless, and contention-less (CDC) functions are expected to play important roles in achieving more flexibility in terms of wavelength routing and wavelength assignment[71]. Today, CDC-ROADM is considered to construct cost-effective photonics transport networks in long-haul and metro area transmission systems. Each function in the CDC-ROADM is shown next.

Colorless function

A colorless function provides the system the ability for optical signal wavelength to be not fixed by the physical input/output port of the TPA but instead be set using software control. A conventional TPA consists of an AWG where the output port is assigned by the wavelength of the optical signal. When the AWG is replaced by a wavelength selective switch (WSS) for the colorless function, the WSS can deliver the input WDM signals to any output port for each wavelength channel by means of software control and not by manual task at the node-equipped site.

Directionless function

A directionless function provides the system the ability for the signal path from the transponder to be connected to any input/output fiber by connecting the TPA to every degree of the ROADM node. To this end, two WSSs, namely WSS1 and WSS2, are introduced. WSS1 aggregates signals from the transmitters (or to the receivers), and then WSS2 connects them to the desired input/output fiber for each wavelength channel. In this way, a colorless and directionless ROADM allows spare transponders to be shared among all the wavelength channels and degrees in the node.

Contention-less function

A contention-less function allows multiple wavelength channels of the same wavelength to be at a single TPA, thus, enabling a transponder to be assigned to any wavelength. The switch of the TPA with CDC function is an $M \times N$ WSS, as shown in Fig. 22. For the CD function, multiple wavelength channels with the same wavelength cannot be input because a single fiber connects two WSSs (WSS1 and WSS2). The contention-less function removes this wavelength restriction by using the $M \times N$ WSS. Recently Nakamura et al. developed the Si photonics based CDC TPA for the ROADM, as shown in the next section.

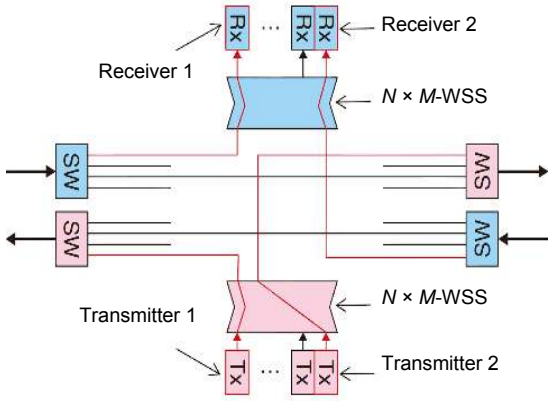


Fig. 22 | Configurations of colorless, directionless and contention-less TPA's for ROADM. Figure reprinted with permission from ref.[69], NTT Technical Review.

Multi-cast Si photonic switch

Explosively growing network traffic of the recent time accelerates the improvement of flexibilities[72] and the evolution of the CDC-ROADM technologies[70,73] along with the adaptive digital coherent technologies[74]. In 2010's, Nakamura et al. have developed multi-cast Si photonic switches for ROADM applications[75]. Figure 23(a) shows two cases for reconfiguring optical paths in CDC-ROADM networks. When an optical path originally set between the nodes A and B is cut accidentally, the CDC-ROADM function smoothly offers an alternative

optical path as an efficient failure recovery. Or, if an optical path originally set between the nodes C and D is forced to change into the path between the nodes C and E due to a rapid traffic accidental change, the CDC-ROADM function offers an optical path change as a prompt optical path reallocation. Nakamura et al. proposed optical switching in the CDC-ROADM both in the wavelength cross-connect and the TPA parts, as shown in Fig. 23(b). Compact and port count extendable TPA improves the flexibility of photonic networks. A cost-effective way for obtaining such TPA is by the combination of multi-cast optical switches and optical amplifiers[73,76–78]. In the multi-cast switches, splitters enable optical paths with different wavelengths between one transmission line and multiple transponders, while filters, or local oscillators for digital coherent receiver enable selection of a wavelength channel on the receiver side. Here, a compact 8 × 8 multi-cast switch as a unit has been used, as shown in Fig. 23(c). The port count on the transponder side can be extended by adding these switch modules and external splitters. As shown in Fig. 23(d), eight 1 × 8 splitters and eight 1 × 8 selectors are connected in a full mesh manner. As shown in Fig. 20 previously, there are various configurations for point-to-point or unicast connection between multiple input and output ports such as PILOSS, cross-point type and Beneš type. These configurations need additional complicated control on elements when the multi-cast connection is introduced. However, the configuration in Fig. 23(d) can provide strictly non-blocking and multicast capabilities. In general, these structures should solve several problems for minimizing the excess loss of the optical switch module, achieving low polarization-dependent loss (PDL) characteristic and faster switching time (e.g., ~ 1 ms). Nakamura et al solved these problems by using Si integrated small-chip based 152 thermo-optic (TO) MZ optical switch elements, as follows.

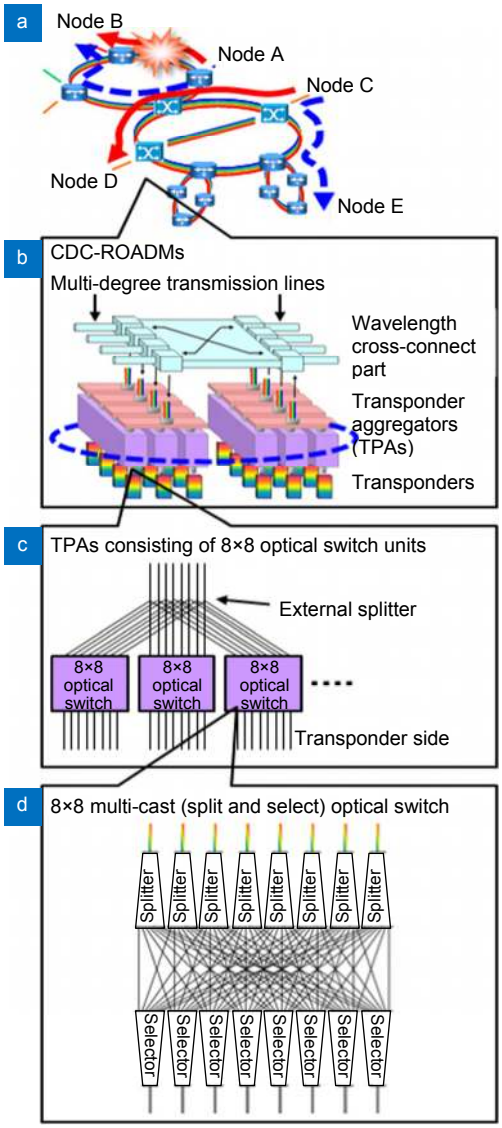


Fig. 23 | (**a**) Two cases of reconfiguring optical paths in photonic networks with CDC-ROADMs. (**b**) Schematic of CDC-ROADM. (**c**) TPA consisting of multiple optical switch modules. (**d**) Configuration of 8 × 8 multi-cast optical switch. Figure reprinted with permission from ref.[75], IEEE.

Polarization-independent Si photonic platform

The Si photonic MZ switch is composed of Si rib waveguides on a SOI wafer. For low loss and polarization insensitivity, Si thickness was designed as 1.5 μm, much thicker than that of 0.22 μm in the widely used Si photonics. A newly designed spot size convertor (SSC) at both facets of the rib waveguide was introduced for minimizing the polarization-insensitive coupling loss between the Si rib waveguide and an external optical fiber. The SSC was designed by stacking a two-layer tapered structure made of Si on the rib waveguide layer. Measured optical loss resulted in less than 2 dB at both TE and TM polarizations over a wavelength range of 80 nm[75].

Figure 24 shows a polarization-independent Si photonic MZ switch and 8×1 selector. The Si TO MZ switch is composed of two multi-mode interference (MMI) couplers and a TO phase shifter, as shown in Fig. 24 (a). For operating the TO phase shifter, a refractive index on one MZ arm is changed by applying a current to the heater placed on it. Typical switching characteristics include switching contrast of about 25 dB and switch on/off response time of 15 μs, both sufficient for failure recovery

applications. Figure 24 (b) shows a configuration of the 8 port (left) × 1 port (right) selector. The selector is composed of a gate part with 12 1×1 switch elements labeled as A1 ~ B4 and a selector part with 7 1×1 switch elements labeled as C1 ~ E1. The 8×1 selector involves totally 19 TO-MZ switch elements. The 8×1 selector sets up one optical path while blocking the other 7 optical paths. Elements A1 and B1 are used when light through these two elements is blocked, and elements A2 and C1 are used when light through these two elements is blocked. This light-blocking scheme is capable of providing high on-off contrast independent of ambient temperature[79]. For the 8 × 8 multi-cast switch, eight 8×1 selectors are placed, resulting in 152 TO MZ switch elements in total.

Evaluation of module performance

For constructing all TO MZ switch elements on chip, optical switch circuit, input and output SSCs, and electrical pads have been integrated within a chip of 12 mm × 14 mm in size, as shown in Fig. 25(a). After a Si optical switch chip was wire-bonded on a sub-mount, an array of 16 narrow-core SMF fibers was attached on the other end. The assembled 8 × 8 switch module had a compact size of 2 cm × 5 cm. Figure 25(b) shows measured optical transmission spectra corresponding to on- and off-states of an optical path. Two color lines were results with two orthogonal polarizations. Figures 25(c) and 25(d) show measured optical loss and cross-talk, respectively, for all 64 (= 8 × 8) paths at the wavelength of 1570 nm. From the average optical loss of 15 dB, the module excess loss was 6 dB after subtracting 9 dB with 1 × 8 splitting. Besides the optical coupling loss, on-chip loss of about 4 dB and the cross-talk of less than -35 dB were obtained.

TPA sub-system and performance

The chip and module were deployed into the TPA sub-system, where two sets of 8 × 48 TPAs for the add and drop sides were constituted on the main board with a 19-inch rack size and a two slot height (~5 cm). The switch drive card with a size of 8 cm× 18.5 cm includes

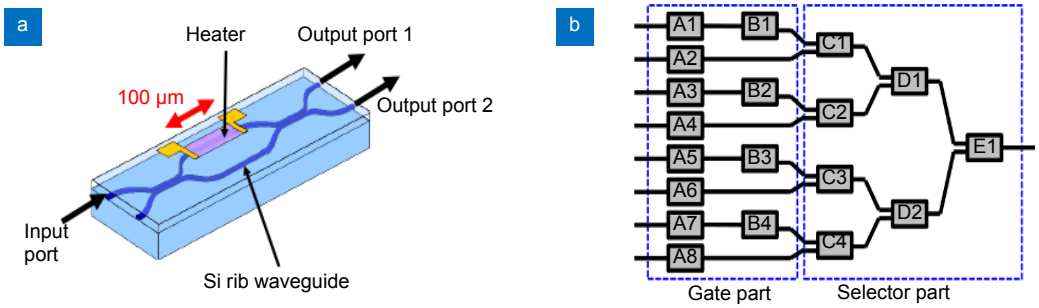


Fig. 24 | Polarization-independent Si photonic MZ switch and 8×1 selector. (**a**) Rib waveguide based Si TO MZ switch element. (**b**) Schematic of 8×1 selector composed of gate and selector parts. Figure reprinted with permission from ref.[75], IEEE.

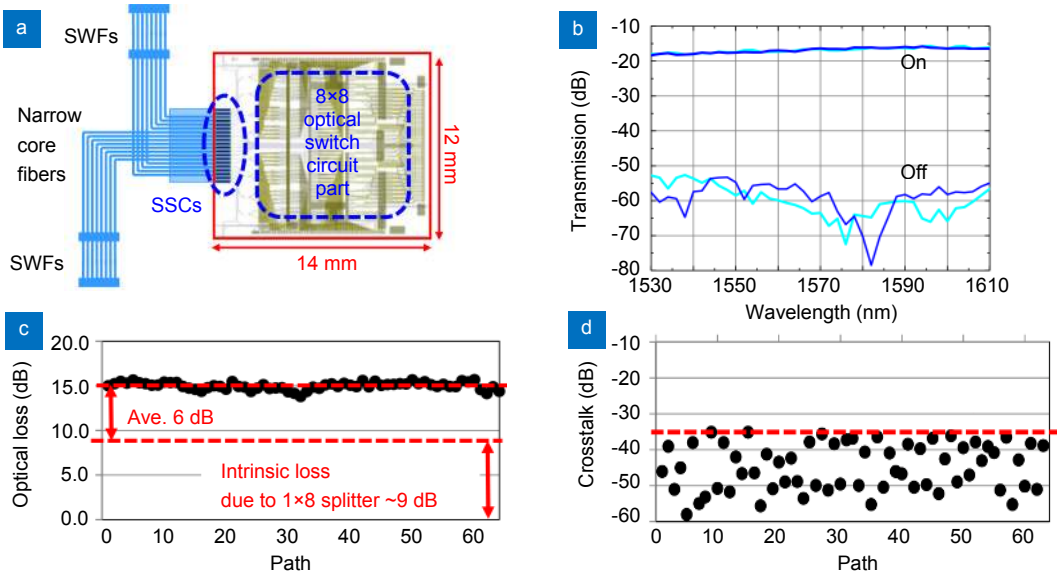


Fig. 25 | (**a**) Schematic of optical switch module consisting of Si chip and fiber array. (**b**) Measured optical transmission spectra showing on and off levels. (**c**) Measured optical loss of all 64 paths. (**d**) Measured cross-talk. Figure reprinted with permission from ref.[75], IEEE.

three optical switch modules together with current drivers for supplying heater currents to TO MZ switch elements. The main board includes four switch drive cards together with a control circuit using an FPGA. Since both of the add and drop sides of the TPA have 48 ports on the transponder side and 8 ports on the transmission line side, the entire subsystem having 112 ports has been constructed densely on one board. The average optical loss, average PDL and switching time of the developed 8 × 48 TPA subsystem were 25.1 dB, 0.32 dB and 0.15 ms, respectively. These results are useful for future faster ROADM networks.

Si photonic switch in the data center network

In the data-com networks, dynamic optical path switching is a promising method to reduce the power consumption similar to the telecom networks[80]. The key device is a low cost, high port-count and strictly non-blocking optical switch with high-density photonic integration using a CMOS-compatible process on large wafers[81–83]. Cheng et al. have recently discussed photonic switching in high performance data centers. They addressed thermo-optics (TO) and electro-optics (EO) from the view-point of switching effect, as well as MZI and MRR from the view-point device structure[66]. Here recent demonstration on the TO based multi-port MZI Si photonic switch by Tanizawa et al[84] and a wide range of reviews on the EO based multi-port MZI and MRR photonic switches by Cheng et al[66] are shown.

TO based multi-port MZI Si photonic switch

Recently Suzuki et al. reported a compact 8 × 8 strictly non-blocking TO switch based on Si-wire waveguides[83], while Tanizawa et al. reported an ultra-compact 32 × 32 strictly non-blocking Si wire optical switch with the fan-out land grid array (LGA) interposer[84]. The switch employs a PILOSS topology[85] and ensures port-count scalability in terms of power consumption since only N element switches should be active in an $N \times N$ switch. Figure 26 shows a top view of the 32 × 32 switch chip. It involves integrated 1024 2 × 2 MZ element switches, 961 intersections, 11 mm × 25 mm footprint die and electrode pads for flip-chip connections. The switch is 46 times as small as the 115 mm × 110 mm silica-based 32 × 32 PILOSS switch[86]. The two technical challenges of high intra-die uniformity and high-density electronic packaging have been solved.

The MZ switch consists of two 3 dB directional couplers for the TM mode and TO phase shifters with a TiN heater on both arms. Si waveguides are 430 nm wide and 220 nm high, and buried by 1.5 μm-thick SiO_2 cladding. The MZ element switch is designed to be in the cross state without heating. The 32 × 32 switch was fabricated using facilities for prototyping 45 nm CMOS transistors on 300 mm wafers. The footprint of the switch including the LGA interposer is 36 mm × 25 mm. Transmission

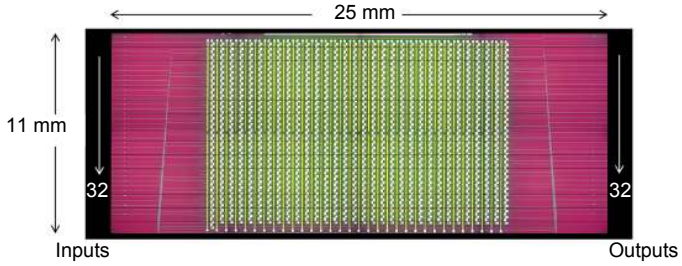


Fig. 26 | 32 × 32 Si TO MZI-based PILOSS switch. Figure reprinted with permission from ref.[84], Optical Society of America.

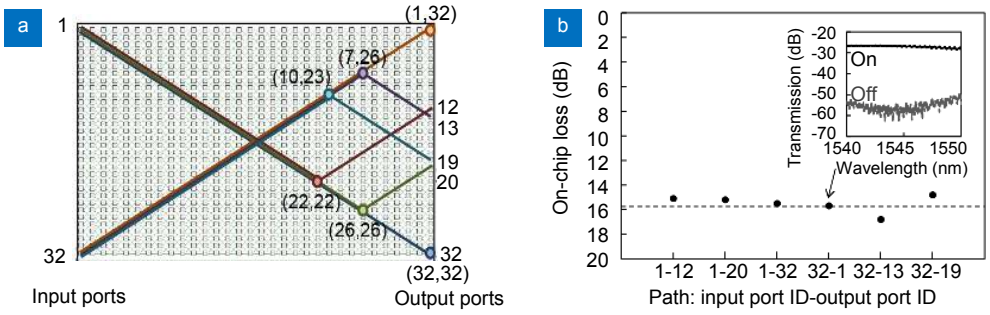


Fig. 27 | Transmission characteristics of the six sampled optical paths 1-12, 1-20, 1-32, 32-1, 32-13, and 32-19. (**a**) Path on the PILOSS switch matrix. (**b**) On-chip loss. Inset in (b) shows the spectral passband of the path 32-1. Figure reprinted with permission from ref.[84], Optical Society of America.

characteristics of the 32 × 32 switch with LGA interposer were measured. Any path contains 32 MZ element switches and 31 intersections in the PILOSS topology. Six paths 1-12, 1-20, 1-32, 32-1, 32-13, and 32-19 were selected to show typical performances, in which 96 MZ element switches in total operate. The selected paths are shown in Fig. 27(a). Figure 27(b) shows on-chip loss of paths at 1545 nm excluding loss of fiber-to-chip coupling. The resultant loss was 15.8 dB including 2.1 dB propagation loss of the access waveguides for the input and output, and 13.7 dB loss of the switch part. The propagation loss of the switch part is estimated to be 5.5 dB. The total power consumption for 32 bar-state and 992 cross-state MZ element switches for the full connections was estimated to be 2.93 W. The worst crosstalk was also estimated to be −20 dB at a bandwidth of 1.8 nm. Finally, 32 × 32 optical switch was successfully demonstrated with a 43 Gb/s digital-coherent quadrature phase-shift keying (QPSK) signal at 1544.93 nm wavelength. The current challenge of this work includes taking full advantages of the 32 × 32 switch with the LGA interposer by developing the printed circuit board (PCB) capable of controlling all the 2048 heaters. Broadening the bandwidth, improving the efficiency of optical coupling, and avoiding the input polarization sensitivity are further challenges to enable the practical use of the optical switch.

EO based multi-port MZI photonic switch

Si has a large TO coefficient (1.8×10^{-4} K^{-1}) and is used for its TO effect for μs-scale switching[87]. For ns-scale switching, on the other hand, the plasma dispersion induced EO effects by carrier injection or depletion are widely used because Si has no linear EO effects (Pockels effect). For the fast EO phase shifting, carrier-injection based PIN junctions are more widely applied than their carrier-depletion type PN junction counterparts. However, the EO MZI configuration causes electro-absorption-induced power intensity imbalance in the two parallel arms, thus deteriorating both crosstalk and insertion loss. In 2016, 16 × 16 port-count MZI based Si EO switches were reported[88–89]. Lu et al. integrated a pair of TiN micro-heaters in both arms and a PIN diode in one arm to optimize device performance[88]. However, the introduction of a single EO phase shifter only in one arm induced loss and crosstalk imbalances between the cross and bar states due to the free carrier absorption. Qiao et al. implemented PIN junctions in both arms but in an opposite set for push-pull switching operation for mitigating the imbalance of power intensity in two arms[89].

Very recently, connectivity of Si EO MZI based switch has been scaled to 32 × 32 by Qiao et al., as shown in Fig. 28[90]. The switch adopted the Beneš topology using 144 MZI elements. An optical phase bias of π/2 was intentionally introduced to one phase-shifter arm to equalize the phase change of the two arms during push-pull operation. Therefore, operation for the bar and cross states could be balanced and thus optimized. On-chip insertion losses and crosstalk ratios, all in the cross configurations, were measured to be 12.9 ~ 16.5 dB and −17.9 ~ −24.8 dB, respectively, while they were 14.4 ~ 18.5 dB and −15.1 ~ −19.0 dB, all in the bar configurations, respectively. Uniformity of the switch units can be improved by using a more precise process such as 90 ~ 45 nm CMOS technology. Nevertheless, a monitoring method is still needed since several-nm variation in the waveguide width might cause a phase change of π/2 in a 200 μm-long phase shifter. Further optimization is achieved by adding TO heaters to provide an additional control method that succeeds in optimization of both TO and EO phase elements for correcting phase-error and power-imbalance simultaneously[91].

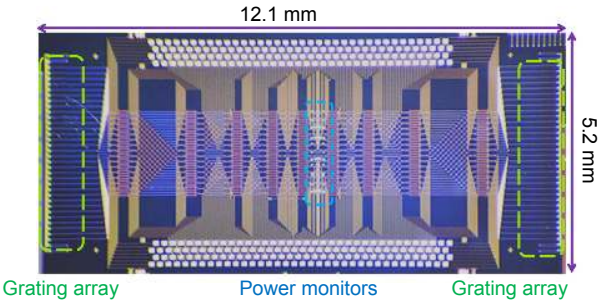


Fig. 28 | 32 × 32 Si EO MZI-based Beneš switch. Figure reprinted with permission from ref.[90], under a Creative Commons Attribution 4.0 International License.

Current performances evaluated on loss and crosstalk in these EO switch circuits are not enough for real applications from the practical point of view[66]. Improvement of such performances in single MZI switch cells has been carried out so far by several methods: introduction of optical phase bias and push-pull control[90], application of broadband coupler[92] and nested MZI structure[93]. Some of them succeeded in excellent crosstalk suppression, although insertion loss is more challenging to manage for large-scale switch fabrics. Semiconductor optical amplifiers (SOAs) are reasonable solutions to provide on-chip gain. The recent report on the lossless SOA-integrated 4 × 4 PILOSS Si switch using a flip-chip bonding technique

was a notable demonstration[94]. For the future studies, built-in amplifiers would be needed to build larger Si EO switches for reducing the insertion loss. Polarization-insensitive Si optical switch with the introduction of polarization control elements and polarization-independent Si waveguides would also be another challenge for practical optical communication[66].

Multi-port MRR photonic switch

Early research work on MRR based switching circuits was conducted jointly by the teams in Columbia and Cornell, USA[95–97]. A representative of the hitless router is shown in ref.[90,95]. The wavelength-selective nature of the MRR unit requires wavelength alignment across the switching circuit, adding extra overhead. Various schemes for fast and efficient wavelength locking have been demonstrated[98–100]. The largest port-count of the crossbar type of switch matrix reported to date is 8 × 7 based thermally tuned fifth-order (five-ring series-coupled) Si MRRs[90,101]. Single MRR switch element was designed to give a 100 GHz passband and an FSR of 350 GHz. The MRR switch element had an average through-loss of 0.9 dB and drop loss of 2.0 dB. Recently, a modular S&S topology by assembling 1 × N/N × 1 ring-based spatial (de-) multiplexers with low loss fibers or 2D optical interposer were proposed[90,102]. An early-stage demonstration of an 8 × 8 S&S MRR switch was performed with excellent results[102].

Si photonic multi-port switches are now innovative key devices in the data center as well as in the telecom network. A wide range of Si photonic switches were overviewed in terms of both TO/EO switching effects and MZI/MRR device architectures. Current performance parameters including port count, switching time, power consumption, and optical power penalty are far from being able to implemented in real applications at the moment. Nevertheless, considering the ever-growing interconnect demand of the data center and also remarkable intrinsic feature of the Si photonic platform, several promising answers to the challenges based on the large-scale SOI CMOS integration technologies will be provided in the near future.

Si photonics phased array for LiDAR

In recent years, continuously growing attention toward Si photonic technologies is also extending to unique applications such as light beam manipulating (steering and shaping) in the free space. The currently remarkable challenge in light detection and ranging (LiDAR) is also one of them[103]. LiDAR is a surveying method for measuring distance to a target by illuminating the target with laser light and detecting the reflected light with a sensor. Differences in laser return times and wavelengths can then be used to make digital 3D representations of the target. LiDAR provides images at higher resolution than that is possible with radar, and has terrestrial, airborne, mobile applications and even applications in point-to-point free-space communication links. In this section, an optical phased array (OPA) developed by Doylend et al is introduced first as an essential element for LiDAR[104]. Then its application to the LiDAR is reviewed from the first demonstration by Poulton et al[105].

OPA

An OPA can be used to steer a beam in free space without mechanical motion[106], and has been demonstrated for LiDAR and free-space communication links[107,108]. Previous bulk optical components needed to be assembled, aligned and co-packaged. However, new integrated optical components offer several advantages such as small size, free of optical alignment, high tolerance against mechanical vibration and low packaging cost. OPAs can also be realized using Si photonic technologies.

In a standard OPA for 2D beam steering, emitter elements or antennae are arranged in a 2D array and a phase is adjusted to shape/steer the beam. Here, integrated waveguides with surface gratings for free-space emission have the advantage of functioning as 1D phased arrays. Each grating tooth scatters light with a phase delay determined by the effective index of the optical mode. Emission angle is determined by the grating pitch, waveguide effective index and wavelength. For example, a schematic configuration of hybrid Si free-space source with integrated beam steering is shown in Fig. 29(a). Figure 29(b) shows its layout of the overall device demonstrated by Doylend et al[104]. Here a tunable laser is followed by an SOA pre-amplifier, after which the beam is split into multiple channels (1 × 8 in this case). Each channel is separately amplified and phase tuned before routed to an array of surface gratings. Emission angle of the beam from the surface grating is determined by the wavelength (here symbolized by color) in the θ (longitudinal) axis and by the relative phase in the ψ axis. They demonstrated a Si 16-channel waveguide surface grating OPA for 2D beam steering. Resultant total field of view, beam width and full-window background peak suppression were 20° × 14°, 0.6° × 1.6° and 10 dB, respectively. Figure 30(a) shows measured beam profiles in the ψ axis

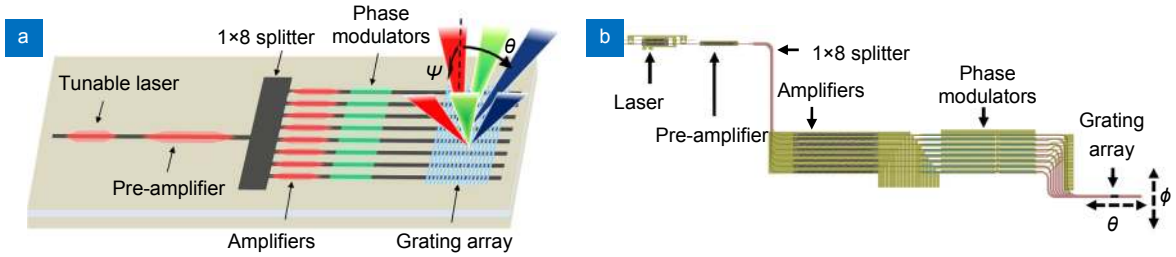


Fig. 29 | (**a**) Schematic configuration of hybrid Si free-space source with integrated beam steering. (**b**) Layout of the overall devices. Figure reprinted with permission from ref.[104], SPIE.

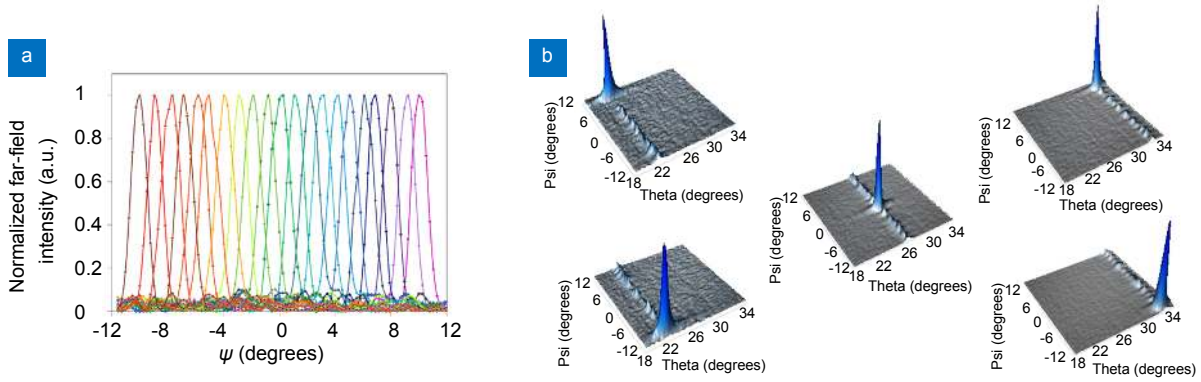


Fig. 30 | (**a**) Measured beam profiles at 1555 nm wavelength as the beam was swept across the field of view in the ψ axis at 1° increments. (**b**) Plots of the 2D beam profiles at the corners and center of the field of view. Figure reprinted with permission from ref.[109], Optical Society of America.

for alignment at 1° increments across the field of view, while Fig. 30(b) shows the 3D plots of the beam measured at the corners and center of the field of view[109]. Afterwards, the Si free-space beam steering chip was first fully integrated using the hybrid Si platform by the same group (Hulme et al)[110]. Demonstrated photonic integrated circuit (PIC) consists of 164 optical components including lasers, amplifiers, photodiodes, phase tuners, grating couplers, splitters, and a photonic crystal lens. The PIC exhibited steering over 23° × 3.6° with beam widths of 1° × 0.6°.

LiDAR

LiDAR has been used extensively in autonomous vehicles[111], robotics[112], aerial mapping[113], and atmospheric measurements[114]. Autonomous systems are key markets for LiDAR devices and, in order to map surrounding environment, solid-state beam steering systems[115] have recently been emphasized to increase system durability as compared with the conventional mechanical system such as gimbal. The solid state system has advantages of high scan rate, high reliability and low system cost. In particular, integrated photonics provides a path for low-cost chip-scale LiDAR systems.

In 2017, coherent LiDAR with integrated optical phased arrays for solid-state beam steering was first demonstrated using frequency-modulated continuous-wave (FMCW) LiDAR with a compact laser diode[105]. FMCW LiDAR allows for simultaneous Doppler-based velocity measurements at no additional cost or complexity. The concept of the FMCW LiDAR is described in detail in ref.[116,117]. According to this technique, triangular modulation is used to increase the resolution of the distance/velocity ambiguity caused by the Doppler shift induced from a moving target. Using coherent detection, a time delay between a received frequency-modulated optical signal and a local oscillator (LO) produces an electrical beat frequency. For a stationary target, a single beat frequency proportional to the target distance is observed, while for a moving target, two distinct beat frequencies occur due to the Doppler shift on the received signal. These two beat frequencies occur in different time regions depending on the direction of the laser frequency sweep. Therefore, the difference of the two beat frequencies is twice the induced Doppler shift including the velocity of the target, while the average of the two beat frequencies is proportional to the time-of-flight distance to the target. In this way, by detecting both beat frequencies, distance and velocity can be measured simultaneously. This is the essence of the FMCW LiDAR system.

Figure 31(a) shows a schematic of the solid-state LiDAR system with transmitting (Tx) and receiving (Rx) optical phased arrays (OPAs). In the figure, all the components Tx OPA, Rx OPA and LO are monolithically

integrated on the Si chip. Figure 31(b) shows a 3D picture of the optical phased array designed for a solid-state LiDAR system, while Figs. 31(c) to 31(e) show SEM photographs of the fabricated phase shifter, magnified one and antenna. Figure 31(f) shows an optical micrograph of the on-chip Si LiDAR system. The total LiDAR chip let was 6 mm×0.5 mm. Here, the tap from the input waveguide to realize the LO was achieved with a 10% directional coupler. The system was controlled using nine copper electrical pads: three for the Tx array, three for the Rx array, two for the signal and bias of the balanced photodetector, and one for ground. The chip let was packaged in a chip-on-board configuration with an epoxied fiber. The phased array consists of 50 grating-based antennae placed at a 2 μm pitch. The antenna emits a main beam with full-width at half maximum (FWHM) intensity spot size of 0.80° in the array dimension. The antenna length is 500 μm and is designed to have a uniform emission pattern by apodized periodic perturbations on the side of a silicon waveguide. A grouped cascaded phase shifter method was used to apply phase shifts to antenna elements. The light to each antenna is evanescently coupled from a common bus waveguide. The cascaded evanescent couplers have a constant 120 nm coupling gap and coupling lengths that increase by 1.89 μm to create a uniform amplitude distribution. A waveguide embedded thermal phase shifter is placed between each coupler. For beam steering applications, thermal tuning steers in the array dimension, ϕ, while wavelength tuning primarily steers in the antenna dimension, θ. A total steering range of 46° × 36° was achieved with thermal steering under electrical power consumption up to 1.2 W and wavelength tuning from 1454 to 1641 nm.

For evaluating the steered LIDAR operation of the device, three targets were placed at different incident angles and different distances, 0.23, 0.32 and 0.45 m apart from the chip. By steering the transmitting and receiving phased arrays simultaneously, each of the targets was measured separately. Although the maximum range and target diffusivity were limited by the aperture size of the phased array performed here, the demonstration conducted here paves the way for on-chip LiDAR systems based on optical phased arrays.

Si photonics for further innovative applications

In *Fingertip-size Si photonic interconnect for ultra-short optical links* Sections, Si photonic interconnect transceivers and multi-port switches in the telecom/data-com networks, and OPA in LiDAR system have been reviewed as currently attractive applications. Now, novel next-generation applications of Si photonics have been proposed: Ultra-compact optical transceivers for IoTs (internet-of-things) and 5G (fifth generation) networks have already been demonstrated[38,118], while deep learning with coherent nano-photonic circuits[119] and neuromorphic photonic integrated circuits[120] based on the Si photonics have been intensively discussed in related community. For more details, refer to each reference indicated above.

Recently a new concept of sub-wavelength grating (SWG) constituted of a periodic waveguide with sub-wavelength pitch nanostructure has attracted much attention for its peculiar anisotropic and dispersive be-

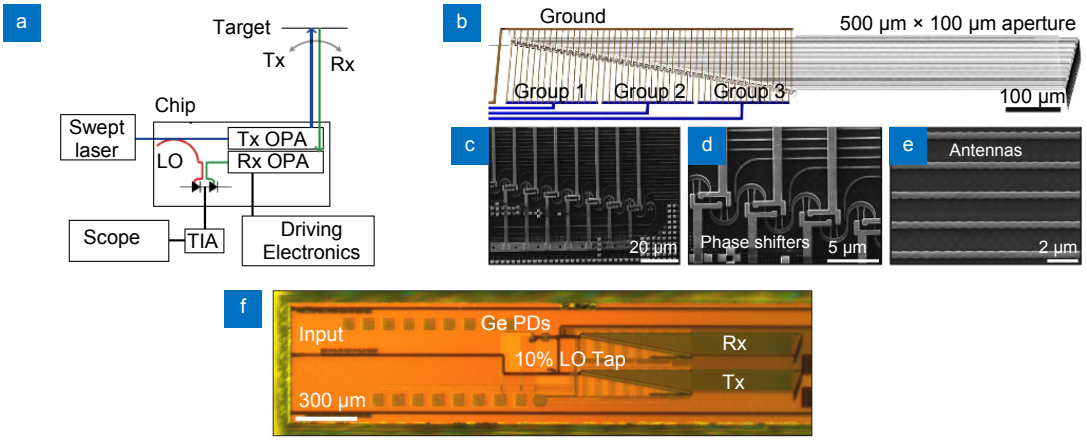


Fig. 31 | (**a**) Schematic of the solid-state LiDAR system with transmitting and receiving optical phased arrays. (**b**) 3D picture of the optical phased array. (**c–e**) SEM images of phase shifter, magnified one and antenna, respectively. (**f**) Optical micrograph of the device. Figure reprinted with permission from ref.[117], Optical Society of America.

haviors like meta-materials[121]. It provides possibilities for novel devices such as highly efficient fiber-to-chip couplers, extremely compact beam splitter, polarization management and spectral filtering, contra-directional couplers, etc., all of which are essential building blocks for advanced integrated optical systems. Along with further innovations in process and material technologies as well as device architectures discussed in this paper, silicon photonics will be a promising solution to meet the energy efficiency, sensitivity and cost requirements even in these new applications.

Summary: challenges and perspectives

Si photonics has remarkably progressed owing to its specific features, small footprint, low cost, high energy efficiency and scalability based on the CMOS-process compatibility. They contributed to implementation of a wide range of heterogeneous passive/active optical elements. Among them, indirect-bandgap induced intrinsic difficulty in Si nano-laser has been considerably overcome by III-V/Si hybrid lasers with chip-/wafer-bonding and III-V hetero-epitaxial direct growth on the Ge/Si substrate. Nevertheless, considering more advanced integration of these components, further innovative technologies will be required. A through-Si-via (TSV) technology capable of a Si photonic interposer allows for integration of high-performance electronic cores like FPGA together with the driving electronics for the photonics. For material integration for diversification of Si-photonics, Ge-based photonics is also a promising technique allowing for SiGe quantum-well based modulators and detectors.

In application worlds, Si photonic interconnect transducers have advanced far urged by the explosively expanding network traffic in data-com markets. A monolithically integrated “Zero-change” Si photonic transmitter was developed in a 0.03 mm^2-sized die by 45 nm SOI CMOS processes and showed 40 Gb/s NRZ transmission characteristics. A fingertip-size optical I/O core with high bandwidth density, low power consumption and high temperature durability was also developed using a 300 mm SOI wafer process and demonstrated 300 m transmission at 25 Gb/s per channel, mounted on the FPGA board. The results are adaptable in the current data-com market.

Si photonics has also been applied to a high-speed and multi-port optical switch with low loss, low cross-talk and polarization-insensitivity in the CDC ROADM telecom network. A multi-cast Si photonic TPA switch with a TO modulator, operating at ~10 μs speed, showed 25 dB average optical loss and 0.15 ms switching time in a 8 × 48 TPA subsystem. The results are useful for future faster ROADM networks. In the data-com network also, dynamic optical path switching using several kinds of multi-port switch topologies have been demonstrated. Ultra-compact 32 × 32 strictly non-blocking Si PILOSS optical switch fabricated using 45 nm CMOS process on the 300 mm wafer demonstrated switching with 43 Gb/s digital-coherent QPSK signal at 1544.93 nm wavelength. Challenges include broader bandwidth, improved optical coupling efficiency and polarization-insensitivity. The switching speed of Si photonics, relying on the TO modulator for μs-scale speed, and EO modulators for ns-scale switching, has been investigated. The EO device depends on plasma effects induced by carrier injection or depletion. Reduction of transmission loss due to the electronic absorption and crosstalk is a main challenge for future demands at ~ns EO switching.

Si photonics applications are extending to novel next-generation systems: optical phased arrays in LiDAR for autonomous systems, ultra-compact optical transceivers in the IoT and 5G networks, deep learning with coherent nano-photonic circuits, neuromorphic photonic integrated circuits, etc. These applications require more advanced Si photonic integration technologies based on new principles and architectures as well as CMOS-compatible processes. Recent novel Si photonic technologies will definitely contribute to the implementation of innovative next-generation Si photonic applications with the support of the intrinsic excellent optical properties of the Si materials.

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Competing interests

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