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SILICON SOLAR CELLS WITH FRONT HETERO-CONTACT AND ALUMINUM ALLOY BACK JUNCTION

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ABSTRACT

We prototype an alternative n-type monocrystalline silicon (c-Si) solar cell structure that utilizes an n/i-type hydrogenated amorphous silicon (a-Si:H) front hetero-contact and a back p-n junction formed by alloying aluminum (Al) with the n-type Si wafer. Such a structure combines a conventional high-throughput Al-Si alloying process with excellent front surface passivation provided by a-Si:H. A key process consideration is to preserve the clean c-Si front surface through the high-temperature alloying, so there will be effective a-Si:H passivation. From cell simulations, we estimate a front SRV of 10-50 cm/sec has been achieved in our process. The best prototype 1×1 cm^2 cell with planar front surface and single anti-reflection (AR) coating layer has demonstrated a confirmed conversion efficiency of 13.5%, V_{oc} of 604.7 mV, and fill factor (FF) of 79.9%. Processes for further efficiency improvements are described.

INTRODUCTION

Silicon solar cells with a heterojunction front emitter made of thin layers of hydrogenated amorphous silicon (a-Si:H) and an a-Si:H back hetero-contact have demonstrated efficiency higher than 22% [1] and 19% [2] on high-quality n- and p-type monocrystalline silicon (c-Si), respectively. The a-Si:H has been deposited by various chemical vapor deposition (CVD) techniques and here in NREL we have focused mostly on developing and optimizing a-Si:H thin film deposited by hot-wire chemical vapor deposition (HWCVD). One of the key advantages of the a-Si:H/c-Si hetero-interface is the low surface recombination velocity (SRV) and high V_{oc} resulting from the low interface state density. SRV below 20 cm/sec [3] and V_{oc} above 710 and 675 mV [2, 4, 5] have been consistently produced at NREL by HWCVD of double-sided Si hetero-junction (SHJ) cells on n- and p-type c-Si, respectively. NREL's cells use HWCVD instead of plasma-enhanced CVD to eliminate the potential ion damage to the high-quality c-Si wafer surface during deposition.

In this paper we report an alternative cell structure on n-type c-Si that combines (n/i)-a-Si as the front surface passivation and electrical contact, with alloyed aluminum (Al) back junction and contacting. The cell is illustrated schematically in Fig. 1. The back p-n junction emitter is formed by depositing Al, followed by high-temperature alloying. The Al-alloyed back junction has a far higher back SRV compared with the double-sided a-Si heterojunction emitter used in the SHJ cell, but it is a simple structure and can be manufactured cost effectively. Cell efficiency higher than 18% has been reported with Al alloy back junction and diffused front surface field [6]. In this study we discuss our first attempts to incorporating the excellent front surface passivation by thin (n/i)-a-Si hetero-contact with an Al-Si back junction. The combination of high-temperature alloying followed by low-temperature a-Si deposition presents a unique challenge: it is essential to preserve the clean c-Si front surface until a-Si:H passivation in order to achieve the desired low front SRV. We will discuss in the paper the effect of different surface preparations on front SRV. We will also analyze our current process to understand the possible limiting factors for V_{oc} and cell efficiency.

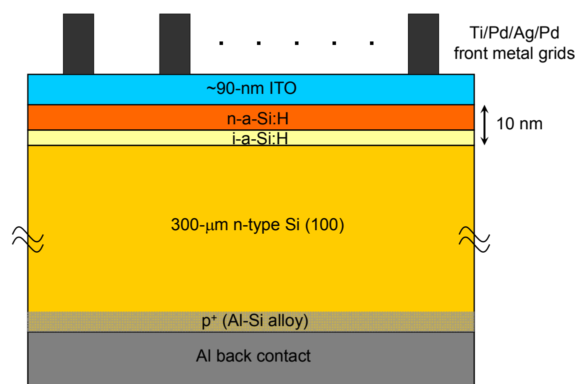

Fig. 1: Schematic cross section of a cell with a-Si:H front hetero-contact and Al-Si alloy back junction.

DEVICE FABRICATION

Phosphorus-doped, n-type double-side polished Si (100) float zone substrates with resistivity of 1.2 Ω-cm and thickness of 300 μm were cleaned by the RCA-1, dilute HF dip, and RCA-2 cleaning processes, in sequence. Samples in this study were not texture etched. One of the essential tasks is to preserve a clean c-Si surface throughout the high-temperature alloying process. We tested three different surface preparations made immediately after the chemical cleaning. These approaches were (1) remove the chemical oxide left by the RCA-2 cleaning and then grow a layer of thermal oxide (~76 nm) at 1000°C in O_2 ambient; (2) leave the surface covered with the chemical oxide; and (3) cover the front surface with spin-on-glass (SOG) (Filmtronics 700B) and densify the SOG layer at 425°C for 60 min to produce a glass layer of ~200 nm. After soaking the back side of the samples with dilute HF to remove the oxide and ensure a good Al-to-Si contact, we then deposited the back side with 3-μm of Al by e-beam evaporation. Al-Si alloying was performed in conventional tube furnace at 900°C for 30 min. A Al-doped back surface field (p^+ layer) of about half of the deposited Al thickness will be formed at this alloying temperature [7].

Thin layers of intrinsic and n-type doped a-Si:H were subsequently deposited on the front surface by HWCVD after a front-surface-only dilute HF soaking removes the front oxide or glass. The intrinsic and n-type a-Si layers were deposited at a substrate temperature of 100°C with SiH_4 feedstock gas and at 160°C from a mixture of SiH_4, H_2, and PH_3 gases, respectively. Conditions for NREL HWCVD hetero-contact formation are described elsewhere [8]. The combined thickness of the i- and n-layers of a-Si:H is 10 nm. A 93-nm ITO was then evaporated on the front to provide good electrical contact to the front grid and serve as an anti-reflection (AR) coating. The front metal grid consists of 50/60/4000/60-nm-thick Ti/Pd/Ag/Pd stack was evaporated through a shadow mask. Shadowing by the front grid is approximately 5%. Finally, cells were isolated by saw dicing into 1×1 cm^2 areas.

TABLE I: Summary of Suns-V_{oc} and IQE on cells with different surface preparation before a-Si:H deposition.

Front surface preparation	Thermal oxide	Chemical oxide	SOG
Suns-Voc (mV)	617	611	548
IQE at 700 nm (%)	83.4	77.7	----

RESULTS

Table I summarizes the Suns-V_{oc} measurement prediction of 1 Sun voltage (before dicing) [9] and the 700-nm internal quantum efficiency (IQE) on completed cells with different front surface preparations. The cell protected by a thermal oxide on front side until the a-Si deposition shows the highest Suns-V_{oc} whereas the cell with SOG shows the lowest. This suggests that the thermal oxide works best to preserve the cleanliness of the c-Si front surface through the high-temperature Al-Si alloying. The application of SOG is even worse than the case of simply having the thin chemical oxide on the surface. We suspect that SOG might have introduced impurities on the front surface which were driven into the c-Si during the high-temperature alloying. Impurity contamination can result in higher defect state density, lower carrier lifetime, and lower Suns-V_{oc}, as observed.

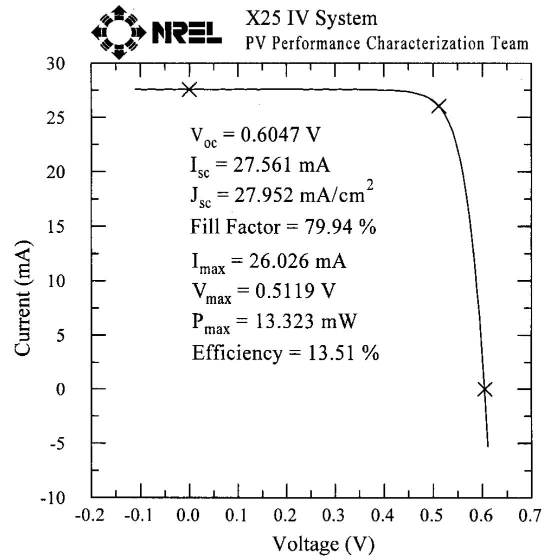

Fig. 2: Certified lighted I-V on n-type c-Si cell with an a-Si:H front hetero-contact and Al-Si back junction.

Figure 2 presents the light current-voltage (I-V) curve, as measured by the independent Device Performance Section at NREL, on our 1×1-cm^2 cell with thermal oxide protection of the front side until a-Si:H deposition. This untextured cell has a V_{oc} of 604.7 mV, J_{sc} of 27.95 mA/cm^2, FF of 79.94%, and efficiency of 13.51%. A roughly 10-mV V_{oc} drop compared with the Suns-Voc in Table I is likely due to recombination centers at the saw-

damaged edges. Reflectance (R), external QE (EQE), and IQE results from the same cell are shown in Fig. 3. The positive slope of the IQE between the 600 and 1000-nm wavelength clearly indicates a back p-n junction structure. The fall of IQE below 600-nm indicates excessive absorption by the front a-Si:H and ITO layers.

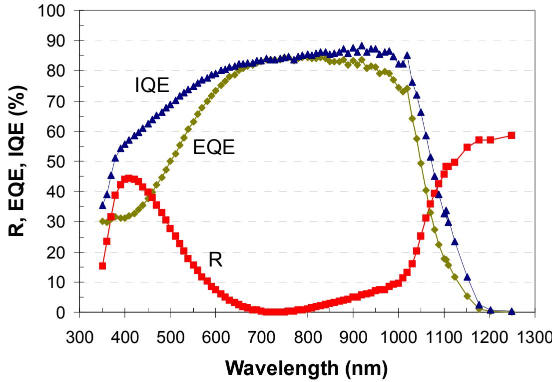

Fig. 3: R, EQE, and IQE results on cell with thermal oxide on front surface before a-Si deposition.

DISCUSSION

Simulations using PC1D were performed to estimate the front SRV and the effective base wafer minority carrier diffusion length (L) on our cells. SRV on the Al-Si back surface is believed to be very high and was set to 10^7 cm/sec [10]. Figure 4 shows the relationships between IQE at 700-nm wavelength and the front SRV for a family of curves representing different values of L ranging from 300 (bottom curve) to 700 µm (top curve), in 50-µm intervals. The measured IQE from cells covered by thermal oxide and chemical oxide until front a-Si deposition are indicated by the horizontal lines. The simulation suggests that the finished cells have L better than 450 µm. Although a definitive front SRV cannot be determined, it appears that front SRV is between 10 and 50 cm/sec on the cell with high-quality thermal oxide coverage until a-Si deposition. Thermal oxide has effectively preserved the clean c-Si surface throughout the high-temperature Al-Si alloying process: the front SRV on the finished cell is close to what we have obtained on low-temperature processed double-sided SHJ cells (< 20 cm/sec [3]). Assuming that L is comparable, the cell with chemical oxide coverage must have a front SRV more than twice as high as the cell with the thermal oxide. From this analysis, we can conclude that chemical oxide falls short on preserving the clean surface for a-Si passivation

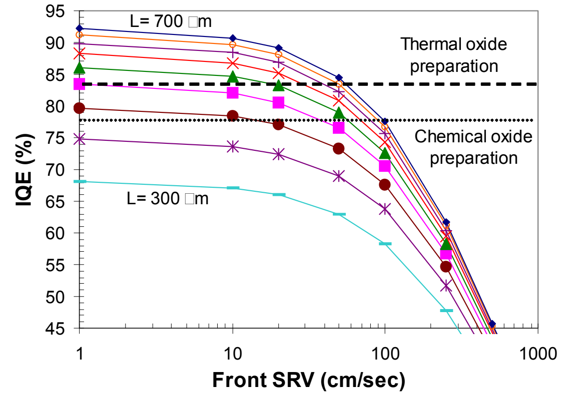

Fig. 4: Simulated IQE at 700 nm. Curves from bottom to top have base diffusion lengths from 300 to 700 µm in 50-µm intervals. Dashed and dotted lines indicate the IQE from cells with thermal oxide and chemical oxide protected front sides before a-Si:H deposition.

and a thermal oxidation process is preferred for the best cell performance.

Several improvements could be implemented to improve the cell performance. First, a textured surface may further increase the effectiveness of light trapping. Second, a better cell isolation technique or larger cell area may alleviate the impact on V_{oc} from the damaged cell edges. Finally, a highly non-uniform appearance of the back surface after Al-Si alloying is often observed in our cells. It has been reported that non-uniformity and poor back-surface fields are obtain when a slow temperature ramp rate in a conventional tube furnace is used for Al-Si alloying [11]. This problem likely extends to our Al back-junction processing. A widely implemented rapid thermal process or beltline furnace with a fast temperature ramp rate can likely achieve a more uniform Al-Si alloy region and improve the junction quality.

CONCLUSION

We have demonstrated an alternative c-Si solar cell structure with front a-Si:H hetero-contact and an Al-Si alloy back junction. We have found that a protective layer of quality thermal oxide can provide a clean Si surface for a-Si:H passivation. By comparing the IQE from measurement results and simulation from PC1D, the corresponding front SRV is estimated to be between 10 and 50 cm/sec, close to what we have obtained on double-sided SHJ cells. The best of these prototype cells has a V_{oc} of 604.7 mV and efficiency of 13.5%, with an excellent FF of 79.9%. This cell structure can potentially

be manufactured cost-effectively and further process improvements should lead to better performance than what is reported here.

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