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Silicon Vertically Integrated Nanowire Field Effect Transistors

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ABSTRACT

Silicon nanowires have received considerable attention as transistor components because they represent a facile route toward sub-100-nm single-crystalline Si features. Herein we demonstrate the direct vertical integration of Si nanowire arrays into surrounding gate field effect transistors without the need for postgrowth nanowire assembly processes. The device fabrication allows Si nanowire channel diameters to be readily reduced to the 5-nm regime. These first-generation vertically integrated nanowire field effect transistors (VINFETs) exhibit electronic properties that are comparable to other horizontal nanowire field effect transistors (FETs) and may, with further optimization, compete with advanced solid-state nanoelectronic devices.

Moore's law predicts the pace at which transistor dimensions are reduced in order to increase the speed and density of transistors on an integrated circuit. Conventional planar metal-oxide-semiconductor FETs (MOSFETs), however, are increasingly facing challenging issues such as short-channel effects (SCEs), scaling of gate oxide thickness, and increasing power consumption.[1] To further miniaturize the transistor while still maintaining control over power consumption, alternative transistor geometries need to be considered.[1] Silicon nanowire based devices[2,3] and horizontal double-gate transistors, such as the Fin FET (FINFET),[4−7] have exhibited high device mobilities and significantly reduced SCEs on the sub-100-nm scale. The FINFET—a structure based on a silicon fin sandwiched between two gate electrodes—has clearly demonstrated that increasing the electrostatic efficiency of the gate electrode geometry is essential in reducing power consumption at this size scale. A surrounding gate geometry is the natural next step for advanced solid-state nanoelectronic devices, yet with conventional top-down fabrication processing, it is not easy to realize such a device architecture with nanoscale features.

Silicon nanowire[2,3,8−11] based transistors exhibit properties comparable to bulk single-crystalline devices, and with the recent demonstration of addressing high-density nanowire circuits,[11] they pose to be very promising building blocks for future nanoelectronic devices. Typically, silicon nanowire transistors have a horizontal, planar layout with either a top or back gate geometry.[2,3,10] However, the amount of energy and time required to align and integrate these nanowire components into high-density planar circuits remains a significant hurdle for widespread application. In-place growth of vertically aligned nanowires, on the other hand, would in principle significantly reduce the processing and assembly costs of nanowire-based device fabrication. Furthermore, pushing the transistor geometry into the third dimension could result in ultrahigh transistor densities. Finally the transport properties of nanowire devices strongly depend on the nature of the nanowire surface.[2,12] For example, hysteretic behavior of the threshold voltage is commonly observed due to the presence of surface and interface charge-trapping states on the nanowire surface.[3,13] This surface dependence potentially limits the transistor reliability.

To these ends, Si VINFETs in particular are promising for several reasons. First, transistors having a surrounding gate structure have been proposed and demonstrated to have excellent subthreshold behavior due to the high gate coupling efficiency and a 35% reduction of SCEs compared to double-gate (FINFET) devices.[14−17] Moreover, the transistor density per unit area can be significantly increased by fabricating multiple gate electrodes and source/drain connections along the length of an individual nanowire, taking advantage of the high aspect ratio vertical nanowire conduction channel. The ability to synthesize longitudinal and coaxial heterostructure nanowires will allow additional design flexibility, such as on-chip incorporation of vertical SiGe heterostructures for on-chip thermoelectric cooling.[9] Furthermore, embedding the nanowires in low charge trap density SiO_2 would eliminate hysteresis and makes the transistor properties much more consistent and reproducible. Although ZnO and CuSCN vertical nanowire transistors have previously been demonstrated,[18,19] Si VINFETs would be more technologic-

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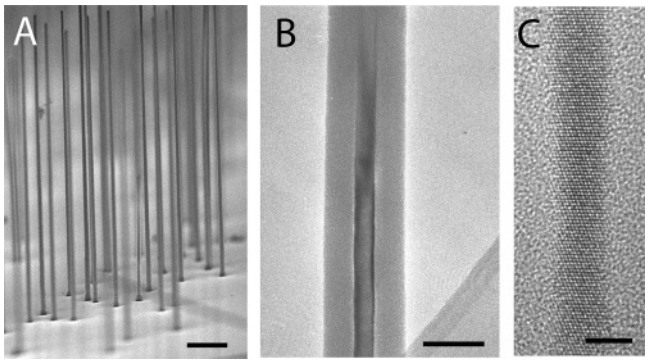

Figure 1. Si nanowires: (A) cross-sectional SEM image of vertically grown Si nanowires off of a Si(111) substrate, scale bar is 1 μm; (B) TEM image of Si nanowire surrounded in a conformal SiO_2 coating after dry oxidation at 850 °C to form the gate dielectric, scale bar is 75 nm; (C) high-resolution TEM image of a Si nanowire with an inner diameter that has been reduced to ~4.5 nm, scale bar is 4 nm.

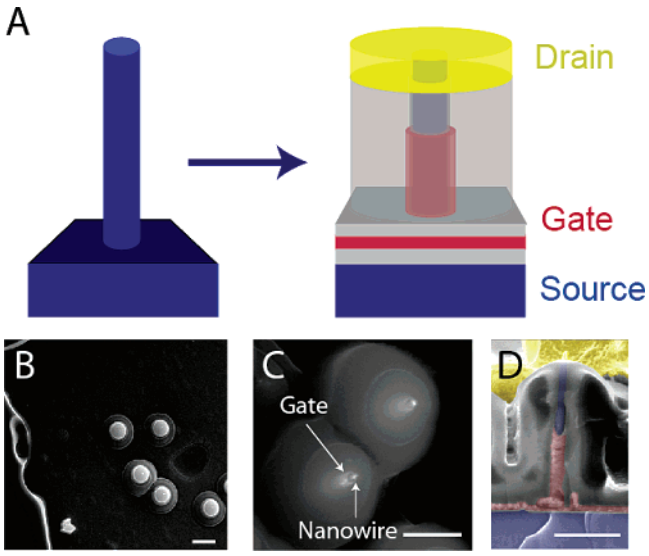

Figure 2. VINFET device configuration: (A) cartoon schematic of VINFET device (right) fabricated from vertical silicon nanowires (left). (B) top-view SEM image of a completed VINFET device, scale bar is 2 μm; (C) top-view SEM image of the midsection of VINFET device, highlighting the conformal gate surrounding the nanowire channel, scale bar is 1 μm. SEM images (B) and (C) are obtained with a 30° tilt. (D) Cross-sectional SEM image of a VINFET device. Scale bar is 500 nm. False color is added to image D, for clarity. In (A) and (D), blue corresponds to the Si source and nanowire, gray corresponds to SiO_2 dielectric, red corresponds to the gate material, and yellow corresponds to the drain metal.

ally relevant, and more easily integrated using existing fabrication techniques.

Vertically grown Si nanowires can be used as active components in a FET design featuring a surrounding gate geometry. To fabricate Si VINFETs, vertically oriented Si nanowires were grown on degenerately boron-doped p-type (ρ < 0.005 Ω cm) Si(111) substrates as previously described.[20] The wires were synthesized via the vapor−liquid−solid (VLS) growth mechanism in a chemical vapor deposition (CVD) reactor using a $SiCl_4$ precursor, a BBr_3 dopant source, and metal nanoparticle growth-directing catalysts. Figure 1A is a scanning electron microscopy (SEM) image of Si nanowires grown from 50 nm Au colloids. Transmission electron microscopy (TEM) analysis confirmed that these nanowires are single crystalline and grow along the (111) direction. Si nanowire arrays grown by the above method exhibit narrow diameter distributions with standard deviations (typically ≤9%) equal to those of the colloid catalysts.[20] Although the nanowires shown in Figure 1a were grown with Au colloids, similar results have been achieved using industry-friendly catalyst compositions such as Pt[21] and Ti.[22] Nanowire length is controlled by the reaction time. Finally, spatial registration of these nanowires can be achieved by controlling the position of the nanoparticles (Figure S1, Supporting Information), as well as using other methods including nanoimprint lithography[23−25] and e-beam lithography.[26] As a result, the dimensions and positioning of the vertical nanowires can be accurately controlled to create suitable substrates for VINFET fabrication.

Figure 2A is a schematic of the VINFET design. Devices were fabricated using conventional very-large-scale integration (VLSI) processing. Vertical silicon nanowire arrays were thermally oxidized to create uniform SiO_2 layers as dielectrics. A typical device has a ~20−30 nm diameter Si nanowire surrounded by ~30−40 nm of high-temperature gate oxide, a Cr metal gate length of ~500−600 nm, and nanowire channel lengths that range from ~1.0 to 1.5 μm. The gate−oxide thickness and channel diameter were obtained from TEM imaging (Figure 1B). Significantly, the channel diameter can be readily reduced below 5 nm via conventional high-temperature thermal oxidation. Such high aspect ratio thin body features are not readily achievable with conventional lithography. Figure 1C shows a high-resolution TEM image of a 4.5 nm ultrathin Si channel created in this manner. Further reduction of the gate oxide thickness could be accomplished by seeding the nanowires with smaller-sized nanoparticles, as well as combining thermal oxidation with SiO_2 etching chemistry. Initial VINFET devices were made from nanowire arrays catalyzed by low-density nanoparticle dispersions. Details of the VINFET fabrication process are described in the Supporting Information. The devices contained anywhere from 8 to 269 nanowires per drain contact pad. Figures 2B−D are SEM images of a typical device.

Typical drain-source current (I_{ds}) vs drain-source voltage (V_{ds}) measurements at various gate voltages (V_{gs}) indicated that B-doped VINFETs behave as accumulation-mode p-type transistors (Figure 3A). The application of a negative (positive) V_{gs} results in an increase (decrease) of I_{ds}, due to the increase (decrease) of majority hole carriers. The V_{gs} value at which the I_{ds} is effectively turned on and accumulation begins is defined as the threshold voltage (V_t). V_t is more clearly seen in the plot of I_{ds} vs V_{gs} at different V_{ds} values for the same device (Figure 3B). The average threshold voltage for 11 different devices was -0.39 ± 0.19 V (1σ). This value is consistent with the expected values for nanowires with dopant densities around 3×10^{16} cm^{-3} (Supporting Information).[27] Additionally, no dependence of the scan rate or direction of V_{gs} on the V_t was observed in any of our devices. This is illustrated by the lack of hysteresis in the I_{ds} vs V_{gs} curves when the V_{gs} is varied from negative to positive to negative values (Figure 3C) at rates varying

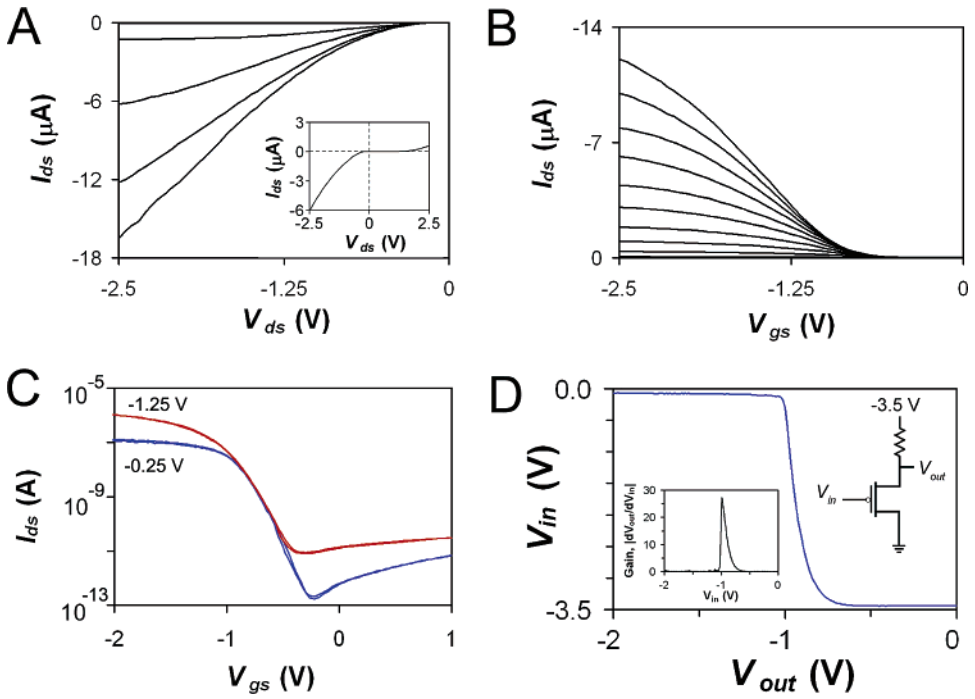

Figure 3. VINFET device characteristics. (A) I_{ds} vs V_{ds} at $V_{gs} = -2.5$, -2.0, -1.5, -1.0, and -0.5 V from bottom to top. Inset shows the full I_{ds} vs V_{ds} spectrum at $V_{gs} = -1.5$ V. (B) I_{ds} vs V_{gs} with V_{ds} ranging from -2.5 to -0.25 V in 0.25-V steps, from top to bottom, respectively. The curves collected in (A) and (B) are from a device having 131 nanowires connected in parallel. (C) I_{ds} vs V_{gs} at $-1.25V_{ds}$ (red) and $-0.25V_{ds}$ (blue), for a device having 20 nanowires collected in parallel, and measured with V_{gs} varying negative to positive to negative V_{gs} values at a 10 mV/s rate. This device has minimal hysteresis, a subthreshold slope of ~120 mV/decade, and an I_{on}/I_{off} ratio $>10^5$. (D) Output characteristics of an inverter circuit (right) fabricated with a p-type VINFET device with 20 nanowires connected in parallel and an external 200 MΩ resistor. An inverter gain of ~28 is determined from the first derivative of this plot with respect to V_{in} (left).

from 0.01 to 3 V s^{-1}. This behavior is indicative of a small number of charge-trapping states in or near the Si/SiO_2 gate oxide interface and illustrates that consistent, reproducible transistor performance can be achieved with minimal outside ambient dependence by embedding these devices in SiO_2.

The significant figures of merit for transistor performance include the transconductance (g_m), the device mobility (μ), on−off current ratio (I_{on}/I_{off}), subthreshold slope (S), and the drain induced barrier lowering (DIBL). The transconductance is obtained from the slope of the linear region in the I_{ds} vs V_{gs} plot at $V_{ds} = -1$ V. The g_m for all 11 devices ranged from 0.2 to 8.2 μS. Accurate comparison with other transistor devices requires normalizing the transconductance with the effective channel width (W_{eff}). Assuming W_{eff} is given by the number of nanowires in each pad multiplied by the diameter of each nanowire, the normalized transconductance of our devices ranged from 0.65 to 7.4 μS μm^{-1}. These are comparable to reported values for high-performance silicon-on-insulator (SOI) MOSFET (5−12 μS μm^{-1})[28] and p-type Si nanowire (0.045−11 μS μm^{-1})[2,3] devices.

The effective hole mobility of an individual nanowire can be extrapolated from its transconductance via the equation $\mu = g_m L^2/(CNV_{ds})$, where L is the gate length, N is the number of nanowires, and C is the gate capacitance for an individual nanowire. The gate capacitance is described by the equation $C = 2\pi\epsilon_0\epsilon_{SiO_2}L/\ln(r_g/r_{nw})$, where ϵ_0 is the vacuum permittivity, ϵ_{SiO_2} is the dielectric constant of the gate SiO_2, r_g is the inner radius of the gate electrode, and r_{NW} is the nanowire radius, assuming a cylindrical channel. However, these simplified expressions neglect the influence of the top portion of the nanowire channel which lacks a conformal gate electrode. In our calculation, we have taken this into account through numerical integration of the capacitance in the gated and nongated portions of our device geometry. The hole mobilities obtained at $-2.5V_{ds}$, range from 7.5 to 102 cm^2 V^{-1} s^{-1} with an average mobility of 52 cm^2 V^{-1} s^{-1}. These hole mobility values are also comparable to those reported for unfunctionalized p-type silicon nanowires (20−325 cm^2 V^{-1} s^{-1})[2,29], and within the same order of magnitude to the best reported values of p-type SOI MOSFETs (~180 cm^2 V^{-1} s^{-1})[28]. We further note that this estimate represents a lower limit of our true device mobility, since our model assumes that every nanowire is in ohmic contact with negligible contact resistance.

The I_{on}/I_{off}, and S can be extracted by plotting the I_{ds} vs V_{gs} on a logarithmic scale (Figure 3C). The I_{on}/I_{off} ratio is the ratio of I_{ds} at current saturation (I_{on}) to I_{ds} at depletion (I_{off}). I_{on}/I_{off} ranges from 10^4 to 10^6 for all devices. The minimization of the subthreshold slope is necessary for low power switching applications in digital electronics. The S value for a typical device having a 300 Å gate oxide shell is 120 mV/decade. Although this is approximately double the theoretical room temperature limit of 60 mV/decade, it is already much smaller than typical values obtained for nanowire devices with back-gate or top-gate geometries (typically >300 mV/decade, with the minimum reported

value to be 140 mV/decade).[2,12,13,30] Further reduction of S can be accomplished by using thinner gate oxides and high-k materials as the gate dielectric, as S values down to 70 mV/decade have been experimentally shown in lithographically defined vertical transistors.[31]

Finally, we have been able to successfully fabricate Si VINFETs with 6.5 nm Si nanowire channel diameters and gate lengths that range from 300 to 350 nm (Figure S5, Supporting Information). These ultrathin channel transistor devices clearly demonstrate the ability to further scale down the device dimensions. Interestingly, with reduced dopant density, these 6.5 nm VINFETs exhibit ambipolar behavior. Such ambipolar behavior has been previously observed for low-boron-doped silicon nanowires ($n_h = 2 \times 10^{15}$ cm^{-3}) created via a lithographic etching process.[32]

The full I_{ds} vs V_{ds} curves for all devices have a small nonlinearity at negative V_{ds} and are rectifying with an order of magnitude decrease in current at positive V_{ds} (inset in Figure 3a). Such nonlinearity in the positive and negative V_{ds} is expected as there are two different contacts to the silicon nanowire: a degenerately doped p^+ Si contact to the base of the nanowire and a NiSi contact to the medium-doped Si nanowire drain. This nonlinearity is partly due to the large resistance of a Schottky barrier at the p-type nanowire drain. Decreasing the contact resistance will result in better transistor performance by effectively increasing g_m, I_{on}/I_{off}, and μ. This could be achieved by tuning the doping gradient profile along the length of the nanowire, through the creation of more highly doped silicon in the contact regions.[33] Nevertheless, the minimization of series contact resistance at the sub-20-nm scale still remains a significant challenge for the semiconductor industry.[34]

To demonstrate the feasibility of using these devices for digital logic applications, we have also fabricated an inverter circuit using resistor−transistor logic. This structure (Figure 3D) was fabricated by connecting a 200 MΩ resistor to one of our p-type VINFET devices in series. When the input voltage is ca. −0.9 V, the output voltage switches between the source (0 V) and the drain voltages (−3.5 V). A large voltage gain of ∼28, which is extracted through differentiating the input and output voltage (left inset in Figure 3D), indicates that these are high-performance devices and are suitable for use in microelectronic applications. The ideal inverter resistor should have a resistance between the on and off state transistor resistances.[35] Therefore, future on-chip logic integration is possible by using properly gated VINFETs as resistors can be easily fabricated via source patterning SOI substrates.

Our prototype Si VINFET devices represent a novel platform for silicon nanowire electronics that combines the epitaxial growth of silicon nanowires with top-down fabrication. These first-generation, unoptimized devices already show transport properties that are within the same order of magnitude as standard planar MOSFETs and other nanowire based devices. Previous device modeling has also suggested that this device structure is competitive with advanced nanoelectronic devices, yet the difficulty in lithographically defining high-aspect ratio vertical Si channels at the sub-100-nm size scale has hindered the research and implementation of this architecture. The in-place, vertical growth of silicon nanowires represents a promising solution to this problem. The three-dimensional device architecture could further increase the transistor density through the additional ability to integrate multiple gates and source/drain connections along the length of these high aspect ratio channels. Future optimization of the processing, device geometry, and dopant concentration, the use of high-k dielectrics, as well as reduction of the gate length can make these devices competitive with FINFETs and other current advanced solid-state devices in the sub-10-nm regime.

Note Added in Proof: During the review of this paper, a conceptually similar nanowire device was reported (Schmidt, V.; Riel, H.; Senz, S.; Karg, S.; Riess, W.; Gösele, U. *Small* **2006**, *2*, 85−88).

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Supporting Information Available: Descriptions of nonlithographic positional control of silicon nanowires, VINFET fabrication procedures, and threshold voltage analysis. This material is available free of charge via the Internet at http://pubs.acs.org.

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