# Simple Analytical Bulk Current Model for Long-Channel Double-Gate Junctionless Transistors

Juan P. Duarte, Sung-Jin Choi, Dong-Il Moon, and Yang-Kyu Choi

***Abstract*—A bulk current model is formulated for long-channel double-gate junctionless (DGJL) transistors. Using a depletion approximation, an analytical expression is derived from the Poisson equation to find channel potential, which expresses the dependence of depletion width under an applied gate voltage. The depletion width equation is further simplified by the unique characteristic of junctionless transistors, i.e., a high channel doping concentration. From the depletion width formula, the bulk current model is constructed using Ohm's law. In addition, an analytical expression for subthreshold current is derived. The proposed model is compared with simulation data, revealing good agreement. The simplicity of the model gives a fast and easy way to understand, analyze, and design DGJL transistors comprehensively.**

***Index Terms*—Bulk current, double gate (DG), junctionless (JL) transistor, semiconductor device modeling.**

## I. Introduction

As a RESPONSE to several problems resulting from the scaling of gate length in metal–oxide–semiconductor field-effect transistors (MOSFETs), junctionless (JL) transistors have recently been reported [1], [2] as an alternative device. Indeed, it can be fabricated more simply [3] than regular MOSFETs by virtue of its junction-free nature. In addition, short-channel effects are more effectively suppressed [1]–[6] in comparison with their counterpart enclosing conventional junctions. Double-gate (DG) JLFETs have basically the same structure as standard DGFETs [7]. However, in the proposed JL transistor, its channel, its source, and its drain have a homogeneous doping polarity and a uniform doping concentration. Therefore, as shown in Fig. 1(a), the formation of junctions is not needed.

The operational principle of an n-channel DGJLFET is different from that of a standard n-channel DGFET. In the subthreshold region [see Fig. 1(b)], a highly doped channel is fully depleted; hence, it can hold a large electric field. By increasing gate voltage, the electric field in the channel reduces until a neutral region is created in the center of the channel. At this point, it is possible to define threshold voltage because bulk current starts to flow through the center of the channel [see Fig. 1(c)]. Then, by further increasing the gate voltage, depletion width reduces until a completely neutral channel is created [see Fig. 1(d)]. This occurs when the gate voltage equals flatband voltage. At the onset of this condition, the bulk current reaches its maximum value. Thereafter, by increasing the gate voltage further, negative charges accumulate on the surfaces of the channel [see Fig. 1(e)]. These charges result in surface current, which is similar to the current in a standard n-channel DGFET. However, the surface current flows at a gate voltage that is much higher than the threshold voltage for the bulk current [8]. Hence, the bulk current drives the total current in the JL transistors. In this letter, simple analytical expressions to describe the bulk current in DGJLFETs are proposed. The model is verified by a numerical simulation with the aid of Silvaco Inc. [9]. It provides a simple way to understand, analyze, and design DGJLFETs comprehensively.

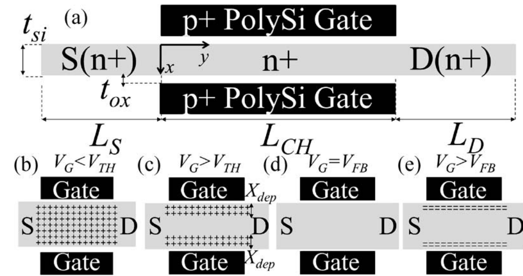


Fig. 1. (a) Cross section of the DGJL transistor. (b) Fully depleted channel in subthreshold mode. (c) Semidepleted channel in bulk current mode. (d) Flatband mode. (e) Accumulation mode.

## II. Bulk Current Model

In order to model the bulk current characteristics of DGJLFETs, a depletion approximation is used to solve the Poisson equation in the channel in a similar manner performed in accumulation-mode transistors [10]. From this solution, it is possible to determine the depletion width $X_{\text{dep}}$ in the bulk current regime, which is given by

$$X_{\text{dep}}\left(V_G,\, V(y)\right) = \left(\varepsilon_{\text{si}}/C_{\text{ox}}\right) \times \left[-1+\sqrt{1-\frac{2C_{\text{ox}}^2}{\varepsilon_{\text{si}} q N_{\text{si}}}\left(V_G - V_{\text{FB}} - V(y)\right)}\right] \quad (1)$$

Manuscript received February 10, 2011; revised February 27, 2011; accepted February 28, 2011. Date of publication April 28, 2011; date of current version May 25, 2011. This work was supported in part by the Ministry of Knowledge Economy/Korea Evaluation Institute of Industrial Technology under Grant 10035320 "Development of Novel 3D Stacked Devices and Core Materials for the Next Generation Flash Memory" and Grant 10029953 "Terabit Nonvolatile Memory Development" through the Information Technology R&D Program and in part by the Ministry of Education, Science and Technology National Research Foundation of Korea under Grant 2009-0082583 through the Nano R&D Program. The review of this letter was arranged by Editor X. Zhou.

The authors are with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Daejeon 305-701, Korea (e-mail: jpduarte@nobelab.kaist.ac.kr; sjchoi@nobelab.kaist.ac.kr; dimun@nobelab.kaist.ac.kr; ykchoi@ee.kaist.ac.kr).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.
Digital Object Identifier 10.1109/LED.2011.2127441

0741-3106/$26.00 © 2011 IEEE

where $\varepsilon_{\rm si}$ is the silicon permittivity, $N_{\rm si}$ is the channel doping concentration, $V_G$ is the gate voltage, $V_{\rm FB}$ is the flatband voltage, and $V(y)$ is the channel potential at location $y$ in the channel. In expression $C_{\rm ox} = \varepsilon_{\rm ox}/t_{\rm ox}$, $\varepsilon_{\rm ox}$ is the oxide permittivity, and $t_{\rm ox}$ is the gate oxide thickness. In a conventional accumulation-mode transistor, the doping concentration at the channel is approximately $10^{16}$ cm$^{-3}$ [10]. However, the channel is much more heavily doped ($\sim 10^{19}$ cm$^{-3}$) in a junctionless transistor [2]. Therefore, for the DGJLFETs, (1) can be simplified using a Taylor expansion at the threshold voltage point $V_{\rm TH}$ that can be found in (1) by setting $X_{\rm dep} = t_{\rm si}/2$, where $t_{\rm si}$ is the channel thickness. Neglecting higher order terms, it gives rise to the following equation for $X_{\rm dep}$:

$$X_{\rm dep}(V_G, V(y)) \cong -(C_{\rm eq}/qN_{\rm si}) \times (V_G - V_{\rm FB} - V(y)) + (t_{\rm si}/2) \times (1 - (C_{\rm ox}/2 + C_{\rm dep})/(C_{\rm ox} + C_{\rm dep})) \quad (2)$$

where $C_{\rm dep}$ is the half-channel depletion capacitance, $C_{\rm dep} = 2\varepsilon_{\rm si}/t_{\rm si}$, and $C_{\rm eq}$ is the equivalent capacitance given by the series connection between $C_{\rm ox}$ and $C_{\rm dep}$. In the DGJLFETs, channels are thin and comparable with dielectric thickness; therefore, $(C_{\rm ox}/2 + C_{\rm dep})/(C_{\rm ox} + C_{\rm dep})$ tends to be 1. This further simplifies $X_{\rm dep}$ to

$$X_{\rm dep}(V_G, V(y)) \cong -(C_{\rm eq}/qN_{\rm si}) \times (V_G - V_{\rm FB} - V(y)). \quad (3)$$

The bulk current through the channel should satisfy Ohm's law, i.e., $dV = IdR$, where $dR$ is the differential channel resistance given by

$$dR = dy/(2W\mu_b qN_{\rm si}(t_{\rm si}/2 - X_{\rm dep})). \quad (4)$$

Here, $W$ is the channel width, and $\mu_b$ is the bulk electron mobility. Using the gradual channel approximation, Ohm's law can be integrated with $dR$ given by (3), yielding the following:

$$I_{\rm BULK} = 2\mu_b qN_{\rm si}(W/L_{CH}) \times \left[\left(\frac{t_{\rm si}}{2} + \frac{C_{\rm eq}}{qN_{\rm si}}(V_G - V_{\rm FB})\right)V_{DS} - \frac{C_{\rm eq}}{qN_{\rm si}}\frac{V_{DS}^2}{2}\right] \quad (5)$$

where $L_{\rm CH}$ is the channel length, and $V_{DS}$ is the drain-to-source voltage. Although $V_{\rm TH}$ can be found in (1), it is possible to extract a simpler $V_{\rm TH}$ expression in (5), and $V_{\rm TH} = V_{\rm FB} - (qN_{\rm si}t_{\rm si}/2C_{\rm eq})$. Saturation drain voltage can be also found in (5), i.e., $V_{DS,\rm SAT} = V_G - V_{\rm TH}$, which represents the drain voltage to induce pinchoff at the center of the channel in the drain side. In the triode region, the drain-to-source voltage square term is negligible, and (5) gives rise to linear dependence on $V_G$ and $V_{DS}$. Furthermore, as $V_G$ tends to be close to $V_{\rm FB}$ [2], the bulk current is simplified and, hence, can be represented by $I_{\rm BULK}(V_G = V_{\rm FB}) \approx \mu_b qN_{\rm si}t_{\rm si}(W/L_{\rm CH})V_{DS}$.

The subthreshold current is given by [11]

$$I_{\rm BULK} = qD_n(W/L_{CH})N(0) \times [1 - \exp(-V_{DS}/V_T)] \quad (6)$$

where $V_T = kT/q$, and $N(0)$ is the areal electron density near the source as follows:

$$N(0) = N_{\rm si}\int_0^{t_{\rm si}} \exp(\phi(x)/V_T)\,dx \quad (7)$$

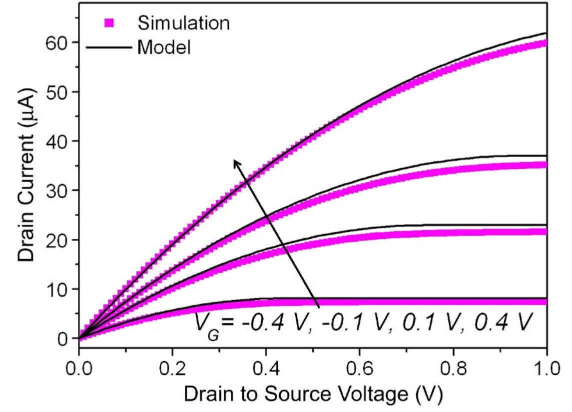


Fig. 2. Drain current versus drain voltage of the DGJL transistor for different gate voltages.

where $\phi(x)$ is the potential in the silicon channel, which is represented by $\phi(x) = -(qN_{\rm si}/2\varepsilon_{\rm si})(x - t_{\rm si}/2)^2 + (qN_{\rm si}t_{\rm si}^2/8\varepsilon_{\rm si}) + \phi_s$; and $\phi_s$ is the surface potential. When the channel is fully depleted, $\phi_s$ can be obtained from $V_G = V_{\rm FB} + \phi_s - (qN_{\rm si}t_{\rm si}/2C_{\rm ox})$. Equation (7) can be expressed as

$$N(0) = \alpha\int_0^{t_{\rm si}/2} \exp(-\beta u^2)\,du = \frac{\alpha}{2}\sqrt{\frac{\pi}{\beta}}Erf\left(\sqrt{\beta}\frac{t_{\rm si}}{2}\right) \quad (8)$$

where $\alpha = 2N_{\rm si}\exp[(qN_{\rm si}t_{\rm si}^2/8\varepsilon_{\rm si} + V_G - V_{\rm FB} + qN_{\rm si}t_{\rm si}/2C_{\rm ox})/V_T]$, and $\beta = (qN_{\rm si}/2\varepsilon_{\rm si})/V_T$. The solution of (8) is not analytic. However, in the case of a DGJLFET where $N_{\rm si}$ is high, the error function gives an approximated value of 1 because its argument is much higher than 1. This gives the following analytical expression for the subthreshold current:

$$I_{\rm BULK} = qD_n\frac{W}{L_{CH}}\frac{\alpha}{2}\sqrt{\frac{\pi}{\beta}} \times \left[1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right]. \quad (9)$$

## III. Model Verification and Discussion

A 2-D numerical simulation using ATLAS [9] is used for the verification of the proposed model. An energy balance model has been used because it is accurate for small dimensions [9]. The Lombardi mobility model has been employed, which accounts temperature, doping, and field dependence effects. Fermi–Dirac carrier statistics along with standard recombination models have been used in the simulation. The parameters used in the simulation are as follows: $V_{DS} = 0.05$ V, $W = 1$ $\mu$m, $L_{\rm CH} = 1$ $\mu$m, $L_S = L_D = 10$ nm, $t_{\rm si} = 10$ nm, $t_{\rm ox} = 7$ nm, $N_{\rm si} = 1 \times 10^{19}$ cm$^{-3}$ (i.e., phosphorus), and a p$^+$ polysilicon gate. For various sets of simulations, some parameters are appropriately modified for each set. Source length and drain length ($L_S$ and $L_D$) are assumed to be small compared with channel length in order to avoid parasitic resistance effects. Other parameters used for the model correspond with those used in the simulation. Only bulk electron mobility values were extracted from each doping concentration using (5).

Fig. 2 shows the drain current versus the drain voltage of the DGJLFETs. The model shows good agreement with the simulation results. At higher $V_{DS}$ voltages, the device is

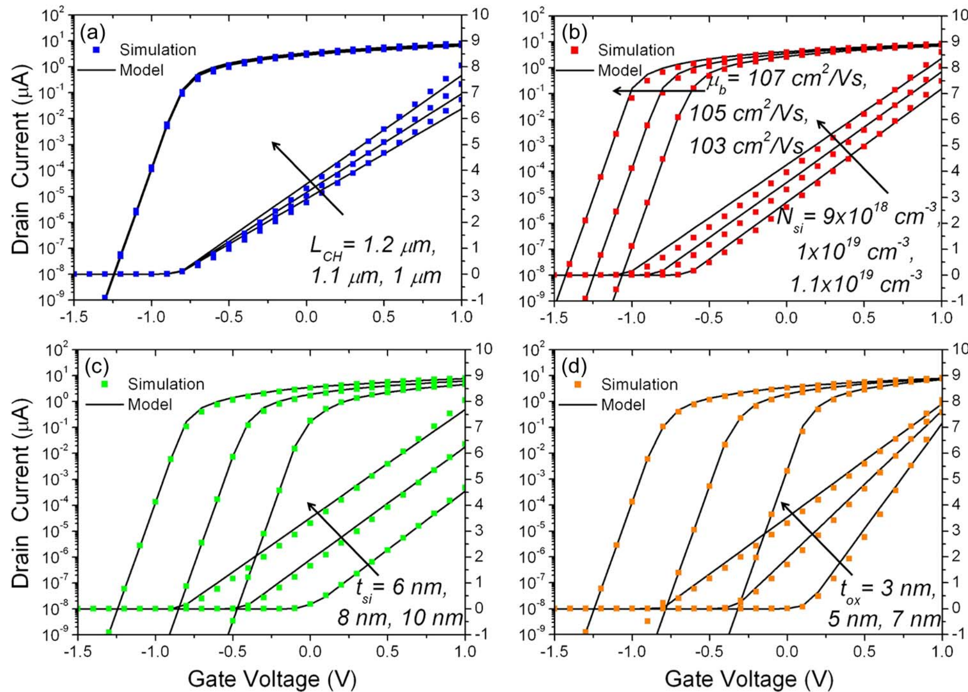


Fig. 3. Drain current versus gate voltage of the DGJL transistor for (a) different channel lengths, (b) different channel doping concentrations, (c) different channel thicknesses, and (d) different oxide thicknesses. Both linear and log scales are plotted.

saturated, as in the case of a conventional DGFET. However, the pinchoff of the bulk current is at the center of the channel in the drain side.

Fig. 3(a)–(d) shows the drain current versus the gate voltage for various $L_{\mathrm{CH}}$, $N_{\mathrm{si}}$, $t_{\mathrm{si}}$, and $t_{\mathrm{ox}}$, respectively. The bulk current expressed in (5) is valid at a gate voltage lower than the flatband voltage. For higher gate voltages, bulk current would be constant. It is found that there is a good correlation between the model and the simulation results. Therefore, (5) and (9) can be used for multifacet purposes in relation to DGJLFETs: a simple way to understand bulk current dependence on device parameters, a simple guideline for DGJLFET optimization, a means of exploiting the variability according to each device parameter, a model parameter extraction methodology, etc. For example, using the $V_{\mathrm{TH}}$ equation, it is possible to calculate threshold voltage sensitivity to the variation of $t_{\mathrm{si}}$. In the case of a doping concentration of $5 \times 10^{19}$ cm$^{-3}$, an oxide thickness of 2 nm, and a channel thickness of 6 nm, the variability derived from (6) is approximately 347 mV/nm, constituting only a 4% difference compared with the variability found previously for the same case in [12].

## IV. Conclusion

A model for the bulk current in long-channel DGJLFETs was derived from the solution of the Poisson equation in the channel using a depletion approximation. A high channel doping concentration allowed a simplification of the depletion width expression, which resulted in a simple equation for drain current, and it also gives a simplification for area electron density calculation, which results in an analytical expression for subthreshold current. The model showed that DGJLFETs were saturated at high drain bias, similar to conventional DGFETs. The results were compared with simulation data, and good agreement was found. The simplicity of the proposed bulk current equation provides an easy and fast way to understand, analyze, and design DGJLFETs comprehensively.

## References

[1] C.-W. Lee, A. Afzalian, N. Dehdashti Akhavan, R. Yan, I. Ferain, and J. P. Colinge, “Junctionless multigate field-effect transistor,” *Appl. Phys. Lett.*, vol. 94, no. 5, p. 053511, Feb. 2009.

[2] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. Dehdashti Akhavan, R. Yan, I. Ferain, P. Razavi, B. O’Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, “Nanowire transistors without junctions,” *Nat. Nanotechnol.*, vol. 5, no. 3, pp. 225–229, Feb. 2010.

[3] A. M. Ionescu, “Nanowire transistors made easy,” *Nat. Nanotechnol.*, vol. 5, no. 3, pp. 178–179, 2010.

[4] C.-W. Lee, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi, and J.-P. Colinge, “Performance estimation of junctionless multigate transistors,” *Solid State Electron.*, vol. 54, no. 2, pp. 97–103, Feb. 2010.

[5] J.-P. Colinge, C.-W. Lee, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, R. Yu, A. N. Nazarov, and R. T. Doriac, “Reduced electric field in junctionless transistors,” *Appl. Phys. Lett.*, vol. 96, no. 7, p. 073510, Feb. 2010.

[6] C.-W. Lee, A. N. Nazarov, I. Ferain, N. Dehdashti Akhavan, R. Yan, P. Razavi, R. Yu, R. T. Doria, and J.-P. Colinge, “Low subthreshold slope in junctionless multigate transistors,” *Appl. Phys. Lett.*, vol. 96, no. 10, p. 102 106, Feb. 2010.

[7] Y. Taur and T. H. Ning, *Modern VLSI Devices*, 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 2009, p. 530.

[8] A. Kranti, R. Yan, C.-W. Lee, I. Ferain, R. Yu, N. Dehdashti Akhavan, P. Razavi, and J. P. Colinge, “Junctionless nanowire transistor (JNT): Properties and design guidelines,” in *Proc. ESSDERC*, Seville, Spain, 2010, pp. 357–360.

[9] *Atlas User’s Manual: Device Simulation Software*, 2008.

[10] J. Colinge, “Conduction mechanisms in thin-film accumulation-mode SOI p-channel MOSFET’s,” *IEEE Trans. Electron Devices*, vol. 37, no. 3, pp. 718–723, Mar. 1990.

[11] Z. Zhengfan, L. Zhaoji, T. Kaizhou, and Z. Jiabin, “Investigation into sub-threshold performance of double-gate accumulation-mode SOI PMOSFET,” in *Proc. ASICON*, Guilin, China, Oct. 2007, pp. 1150–1153.

[12] S.-J. Choi, D.-I. Moon, S. Kim, J. P. Duarte, and Y.-K. Choi, “Sensitivity of threshold voltage to nanowire width variation in junctionless transistors,” *IEEE Electron Device Lett.*, vol. 32, no. 2, pp. 125–127, Feb. 2011.