Simple Digital Control Improving Dynamic Performance of Power Factor Preregulators

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Abstract - **This paper presents the practical implementation of a fully digital control for boost power factor preregulators (PFP's). The control algorithm, which is simple and fast, provides a significant improvement in the system's dynamic performances compared to usual analog control techniques. The paper discusses the design criteria and the actions taken for the implementation of the digital control, which is performed by means of a standard micro-controller (Siemens 80C166). The effectiveness of the approach is assessed by experimental tests.**

I. Introduction

As compared to conventional analog controllers, digital regulators offer several advantages such as: possibility of implementing non-linear and sophisticated control algorithms, reduction of the number of control components, high reliability, low sensitivity to components' ageing, negligible offsets and thermal drifts. On the other hand, digital regulators may imply a higher development cost and a limitation in the attainable control bandwidth due to the sampling process. These drawbacks, which in the past limited their application to dc power supplies, can now be partially overcome by modern microcontrollers, featuring a very high performance level at a relatively low cost. Therefore microcontroller applications are now feasible not only in the area of ac drives and three phase converters, where they are indeed extremely popular, but also in the field of dc/dc converters.

For instance, digital control has been applied to dc/dc converters in [1,2], mainly to implement sophisticated and non-linear control laws. This paper, instead, discusses the implementation of a simple and effective digital control of a boost power factor preregulator, using a standard micro-controller (Siemens 80C166). The control strategy is defined according to what is normally done in conventional analog controllers and widely discussed in literature [3,4]. Nevertheless, by exploiting the potentialities of the digital implementation it is possible not only to get the aforementioned general advantages, but also, more specifically, to significantly improve the system dynamics. On the other hand, the well known drawback of the digital approach, represented by the limited bandwidth of the current control loop, is shown to produce a phase leading current absorption from the grid which, anyway, can be fully compensated.

The first part of the paper gives a detailed explanation of the adopted control technique. In the following part, a theoretical explanation of the input current phase displacement is provided. Finally, in the last part of the paper, all the details concerning the practical implementation with the 80C166 μC (control timing, hardware requirements, prototype ratings) are discussed and the results coming from laboratory tests are presented.

II. Power Factor Preregulators

Fig. 1 shows the basic scheme of a boost PFP. As it is known, this topology is particularly suited for

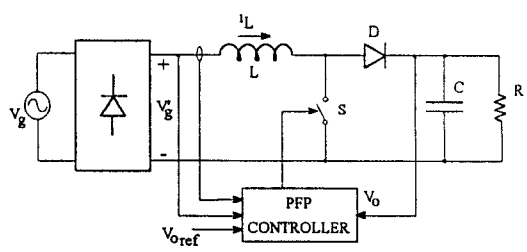

Fig. 1 - Basic scheme of a boost PFP

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average current control [3]. The PFP's current controller operates the switch so as to draw from the grid an average current whose waveform is proportional to the line voltage V_g, as implied by (1).

$$i_L(t) = g_{V_0}(t) \cdot V'_g(t) \qquad (1)$$

A key point in PFP's control is that, due to the low frequency power unbalance, the output capacitor always presents a voltage ripple at twice the line frequency. The voltage ripple, assuming unity power factor and neglecting the input inductor energy, is given by (2), where ω_f is the line angular frequency and P_o is the output power.

$$|\Delta V_o(t)| = \frac{P_o}{2\omega_f C V_o} \cdot \sin(2\omega_f t) \qquad (2)$$

This cannot be compensated by the voltage control loop without causing the input current distortion, which, therefore, usually limits the achievable bandwidth to a fraction of the line frequency (10÷20Hz). Among the different possible solutions to this problem [5,6,7,8], this paper takes into account the output voltage ripple notch-filtering, which, thanks to the digital approach, can be easily and efficiently implemented [5].

III. Digital Control Strategy

The scheme of a boost PFP with digital control is shown in Fig. 2. The inner loop controls the average current by means of a PI regulator (K_I). The reference for this loop is provided by multiplying the sampled input voltage signal by the output of the voltage loop PI regulator (K_V). The control requires the sampling of three variables: input rectified voltage (V'_g), output voltage (V_O) and average input current (i_S), which is performed by means of insulated transducers with a sampling frequency equal to the modulation frequency (20kHz).

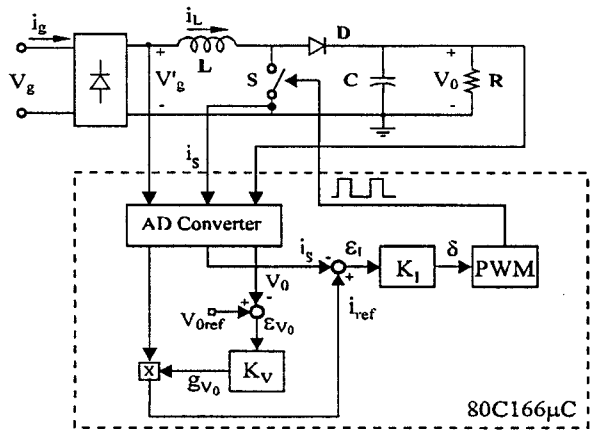

Fig. 2 - Scheme of converter and digital controller

As far as the current loop is concerned, the required calculations, implementing a digital PI regulator with anti-windup, are performed immediately after the current sampling to minimise the delay. The regulator is designed to get a 2kHz bandwidth, which was selected to ensure a satisfactory tracking of the current reference and, at the same time, to allow the direct design in the continuous time domain. A phase margin greater than 70°, necessary to cope with the delay introduced by the holder, was also set.

An important advantage of the digital approach is that the average value of the sensed current is obtained, without low-pass filters in the loop, by synchronising sampling and modulation so that the current is always sampled in the middle of the switch on-period. This allows precise regulation of the average current without introducing any delay in the loop, as long as the converter operates in the continuous conduction mode (CCM). It is worth noting that when the converter enters the discontinuous conduction mode (DCM), even if the average current is no longer equal to the sensed current and the converter's dynamics change, no stability problems arise, mainly because of the very low gain of the current loop in such conditions. However the input current is distorted until the converter enters the CCM again. Finally, this solution allows the sensing of the switch current, instead of the inductor one, by using a lossless current transformer.

As shown in Fig. 2, the reference for the current loop is provided by multiplying the sampled rectified input voltage (V'_g) and a scaling factor given by the output voltage regulator (g_{V_O}). This task is accomplished by a proper routine which starts after the input voltage conversion.

The transfer function to be compensated by the output voltage regulator is given in [3,4] and does not call for special design provisions, since the required bandwidth (typically around 20Hz) is much lower than the sampling frequency. In order to increase the voltage loop bandwidth, while limiting the input current distortion, the application of analog notch filters to the sensed voltage has been investigated [5,6]. This solution, however, introduces undesired effects on the phase of the open loop gain. Digital filters instead, allow a strong reduction of the 100Hz component in the feedback signal with very small effects on the phase. Another interrupt routine, which starts after the output voltage conversion, implements a digital notch filter and a PI regulator to get to a high bandwidth control with reduced input current distortion.

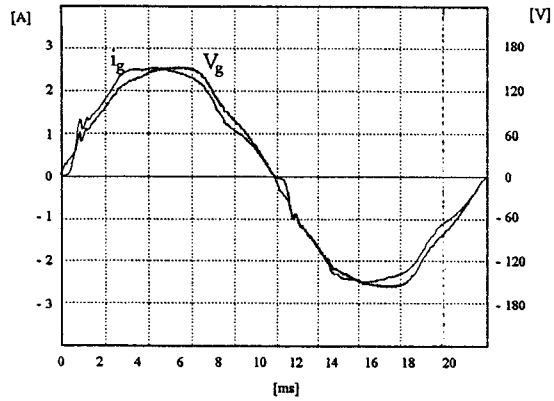

Fig. 3 - Measured input current and voltage waveforms

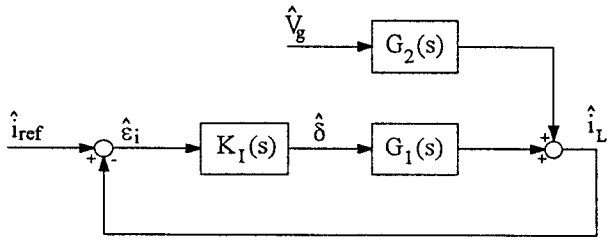

Fig. 4 - Block diagram of current control loop

IV. Input Current Phase Displacement

Fig. 3 shows the phase displacement between the measured current and voltage on the grid. As it can be seen, the current waveform appears to be about 7° leading the voltage waveform. Such an effect can be explained considering the control block diagram shown in Fig. 4, which refers to a small signal analysis of the current loop. The transfer functions G_1 and G_2 can be derived by state space averaging the converter equations in CCM. They are given in (3), where, for instance, $\bar{\delta}$ represents the steady-state value of the duty cycle δ, while $\hat{\delta}$ represents its perturbed value. K_I represents the current controller (PI regulator).

$$G_1(s)=\frac{\hat{i}_L}{\hat{\delta}}=\frac{s\bar{V}_oC+\frac{\bar{V}_o}{R}+(1-\bar{\delta})\cdot\bar{i}_L}{s^2LC+s\frac{L}{R}+(1-\bar{\delta})^2} \tag{3}$$

$$G_2(s)=\frac{\hat{i}_L}{\hat{V}_g}=\frac{sC+\frac{1}{R}}{s^2LC+s\frac{L}{R}+(1-\bar{\delta})^2}$$

By closing the loop, the transfer functions from i_{ref} to i_L (W_1), which is the current closed loop, and from V_g to i_L (W_2), can be calculated:

$$W_1(s)=\frac{\hat{i}_L}{\hat{i}_{ref}}=\frac{G_1(s)\cdot K_I(s)}{1+G_1(s)\cdot K_I(s)}$$

$$W_2(s)=\frac{\hat{i}_L}{\hat{V}_g}=\frac{G_2(s)}{1+G_1(s)\cdot K_I(s)}. \tag{4}$$

Assuming a steady state condition, with constant average output voltage, i_{ref} can then be expressed as

$$\hat{i}_{ref}=g_{V_0}\cdot\hat{V}_g, \tag{5}$$

where g_{V_0} is a constant factor depending on input voltage steady-state level. Therefore, using (4) and (5), the complete transfer function from v_g to i_L can be found to be:

$$W(s)=\frac{\hat{i}_L}{\hat{V}_g}=g_{V_0}\cdot W_1(s)+W_2(s) \tag{6}$$

Calculating the phase of W(s) at $s=j\omega_f$, the expected phase displacement between input voltage and current can be found. The results of this calculation for different current loop bandwidths and phase margins are shown in Fig. 5.

Fig. 6, instead, displays the current open loop gain $G_1(s)K_I(s)$ at the line frequency ω_f for different bandwidths and phase margins.

As it is shown by (6), the outcoming leading phase displacement between input current and voltage is totally due to the term W_2, since W_1 is practically unity at the line frequency.

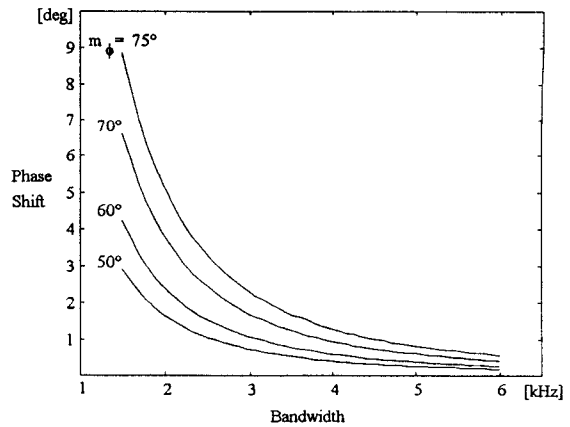

Fig. 5 - Phase displacement as a function of current control loop bandwidth and phase margin (m_ϕ)

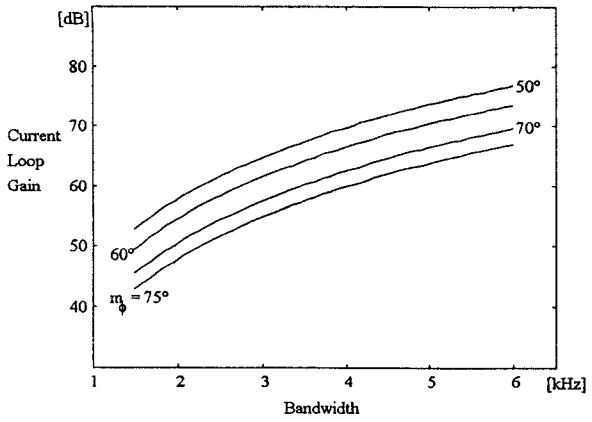

Fig. 6 - Current loop gain at $\omega=\omega_f$ as a function of current control loop bandwidth and phase margin (m_ϕ)

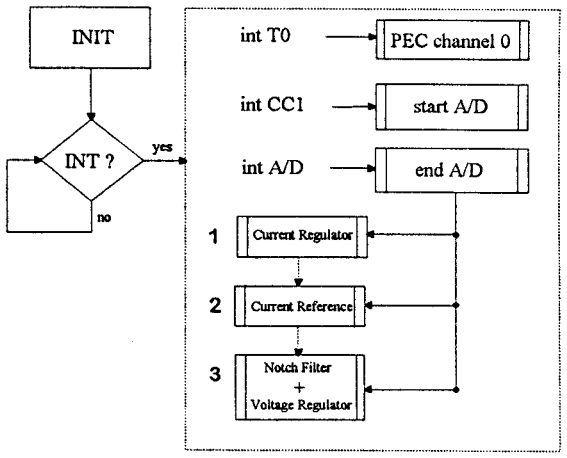

Fig. 7 - Flow chart of control algorithm

The effect of W_2 is heavier when the current loop gain is small because, as it is possible to see in (3,4), W_2 and G_IK_I are inversely proportional to each other. As Fig. 6 shows, the bigger the phase margin or the smaller the loop bandwidth, the smaller the loop gain. Therefore, with low current loop bandwidths the phase displacement tends to be higher. In standard analog implementations this effect is normally negligible, thanks to the high current loop achievable bandwidth. This is no longer true for the digital implementation of the current controller because of the bandwidth limitation imposed by the sampling process. Anyway, since the phase shift is constant, once the converter power rating and controller bandwidth are defined, the practical solution to the problem is straightforward; inserting a suitable delay line between the input voltage sampling and the elaboration of the converted data, the leading phase shift can be completely compensated, thus restoring an almost unity input power factor.

V. Digital Control Implementation

The control strategy described in section III was practically implemented by means of the 80C166 μC. Fig. 7 represents a flow chart of the control algorithm. The program starts executing the standard initialisation routines, then enters an idle mode, waiting for interrupts. There are three interrupt sources: the first (T0) is related to the PWM process and calls for the duty-cycle update at the beginning of each modulation period. This has the highest priority. The second comes from the timer CC1, which is programmed to count down from a half of the duration of the switch on-period.

When the count-down ends an interrupt is generated and, as a result, the A/D conversion of the first control variable (switch current) is started. The third interrupt is produced when the current A/D conversion is over. The sequence of the A/D conversions proceeds automatically; the second sampled variable is the input voltage and the last is the output voltage. At the end of each conversion, when the interrupt labelled INT A/D in Fig. 7 is generated, a proper service routine elaborates the result and programs the next conversion.

The sampling of the switch current is operated at the half of the switch on-period, thus allowing to acquire the average inductor current value with no need for low pass filters to eliminate the ripple. The routine handling the current conversion implements the PI current regulator. At its very end, this routine programs the next service routine, so that when the second conversion is over, the elaboration of the input voltage sample can be performed. This consists of phase shift compensation, which is done by means of a delay line, and current reference calculation. Once again, at its end this routine programs the next interrupt handling so that, when the third conversion is over, all calculations regarding output voltage can be performed. These consist of a digital notch filter to eliminate the voltage ripple from the feedback signal and of a conventional PI voltage regulator.

The digital notch filter can be directly designed in the discrete time domain by allocating two transmission zeros and a couple of poles at the ripple frequency (λ_o), as shown in Fig. 8.

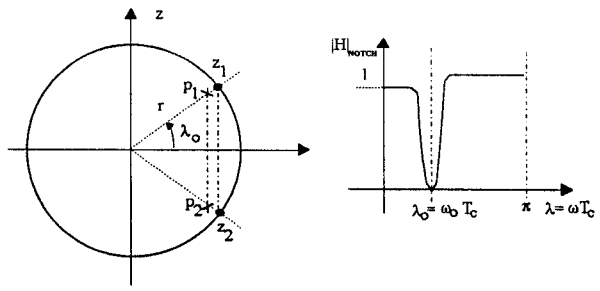

Fig. 8 - Notch filter design

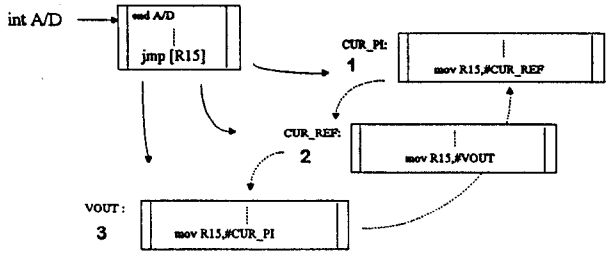

Fig. 9 Sequence of interrupt service routines

As known, the closer the poles and the zeros the more selective the filter and negligible the phase perturbation. Anyway, as a consequence of the fixed point architecture of the adopted μC, it was not possible to select the poles radium to be more than 0.95. The discretisation in the filter coefficients would otherwise have caused filter instability. An additional low pass filter was then needed to compensate for the unwanted high frequency amplification introduced by the notch filter. Its consequence is a 10° phase lag at 20 Hz, which must be considered in designing the voltage regulator.

At the end, this routine programs again the interrupt service routine for the inductor current, so that a new modulation period can begin. Fig. 9 shows the explained sequence of the interrupt service routines.

A key point of this implementation is control timing. It is important to notice that the only actual constraint for the control algorithm is to be able to determine the duty cycle for the next modulation period before the end of the current one. As shown in Fig. 10, this is always possible, since it requires about 22 μs (comprising A/D conversion, dead-times and current loop). Therefore, since in the worst case, when the duty-cycle is close to 100%, there are more than 25 μs available, this critical calculation always ends within the current modulation period. Of course the other control tasks may, instead, end in the following modulation period; this is not a problem anyway, since they operate on slowly variable signals, which are not affected by the resulting one-cycle delay in the calculations.

VI. Experimental Results

The ratings of the boost PFP used for the experimental tests are given by Table I.

Table I - Prototype Ratings

Input Voltage	$V_g = 110V_{RMS}$
Output Voltage	$V_o = 200V$
Rated Output Power	$P_o = 200W$
Switching Frequency	$f_{sw} = 20kHz$
Input Inductor	$L = 4.6mH$
Output Capacitor	$C = 470\mu F$

The experimental verification of the prototype operation was focused, at first, on testing the power factor correction's quality. As shown in Fig. 11, the input current replicates the input voltage waveform pretty well; accordingly the measured power factor is 0.994, while the total harmonic distortion of the corresponding input voltage V_g and filtered current i_g are 3.8% and 6.2% respectively.

Fig. 12 shows the effect of the digital notch filter applied to the output voltage feedback signal. It is possible to note that the current distortion is strongly reduced by the filter. The designed bandwidth for the output voltage control loop is 20 Hz both in the case of Fig. 11 and of Fig. 12. Moreover, as for any of the performed tests, the compensation of input current phase lead is active. As it can be seen, the digital notch filter effectively reduces the current distortion for a given bandwidth. To further illustrate this effect, Fig. 13 shows the measured line current spectra.

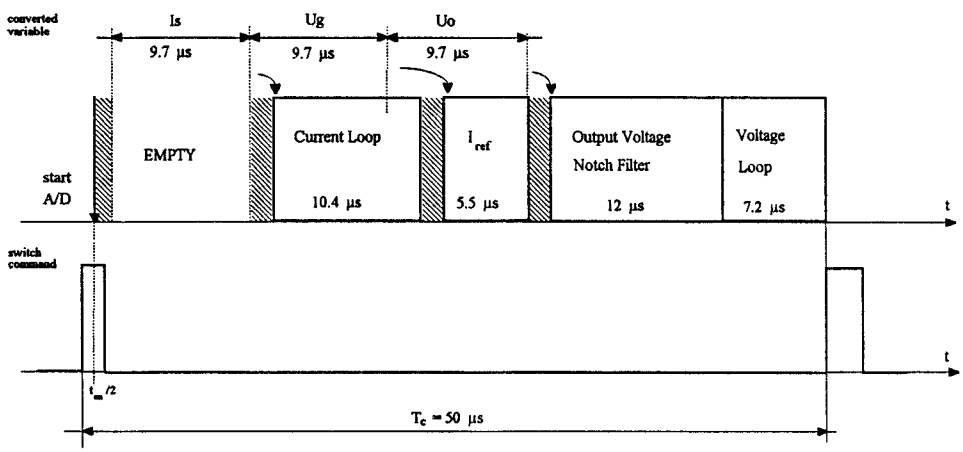

Fig. 10 Timing of the control algorithm. Shaded areas represent the dead time of interrupt service routines (≈1μs)

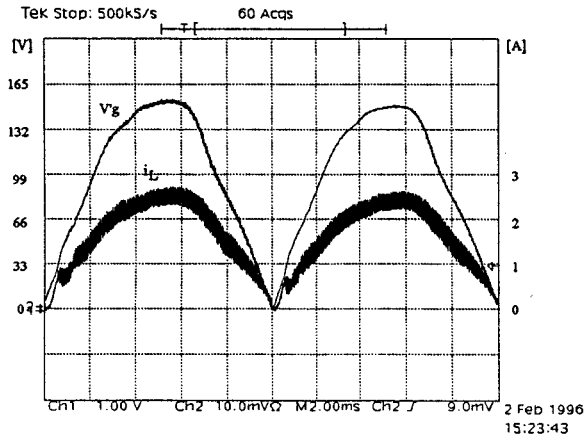

Fig. 11 - Input current and voltage waveform

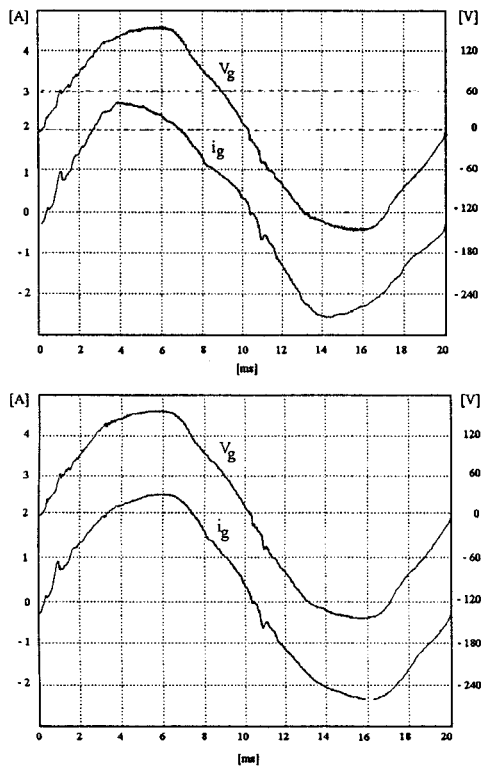

Fig. 12- Line voltage and current: without notch filter (top), with notch filter (bottom)

It is possible to notice the evident reduction of the third harmonic component of the spectrum, which accounts for the measured THD reduction from above 10% to about 6%.

Inversely, it is also possible, given a certain THD acceptable level, to push the voltage loop bandwidth far beyond the achievable limit with no filter. As a consequence of the voltage loop bandwidth's increase, it is possible improve the dynamic performances of the PFP. As a comparison, Fig. 14 shows the behaviour of the converter in case of a load step change from full to minimum load (200Ω →1500Ω) and back. The

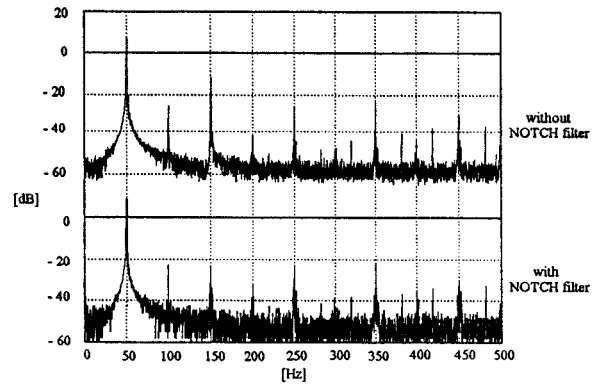

Fig. 13 - Line current spectra without (top) and with (bottom) notch filter

designed voltage loop bandwidths are 10 Hz and 40 Hz respectively, so as to ensure a similar current harmonic distortion with and without notch filter. The difference in the dynamic responses is pretty evident. The settling time at load reconnection, for instance, passes from about 80 ms to about 20 ms.

Finally, Fig. 15 shows the behaviour of the tested prototype at start-up. A soft start procedure was implemented to gradually raise the output capacitor

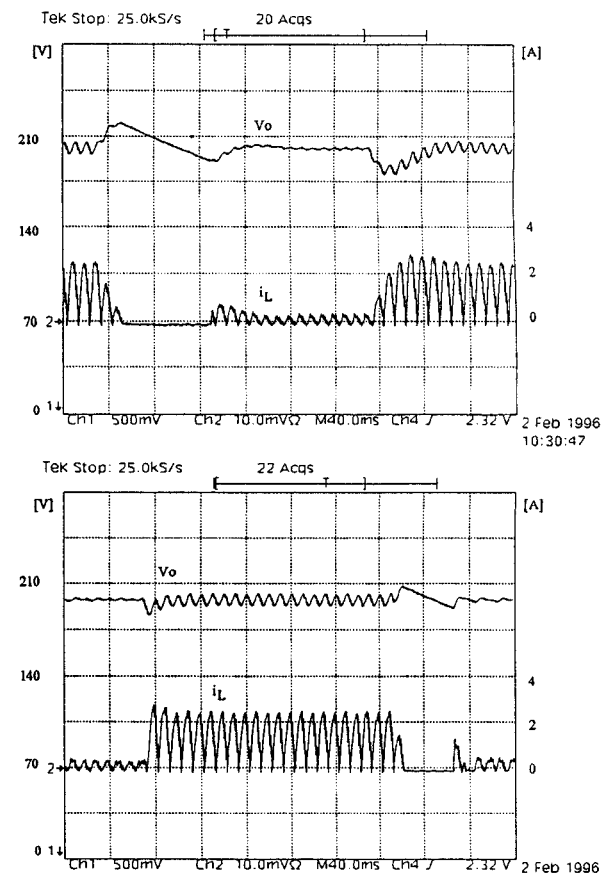

Fig. 14 - Dynamic behaviour of the tested PFP in case of load step changes: without (top) and with (bottom) notch filter

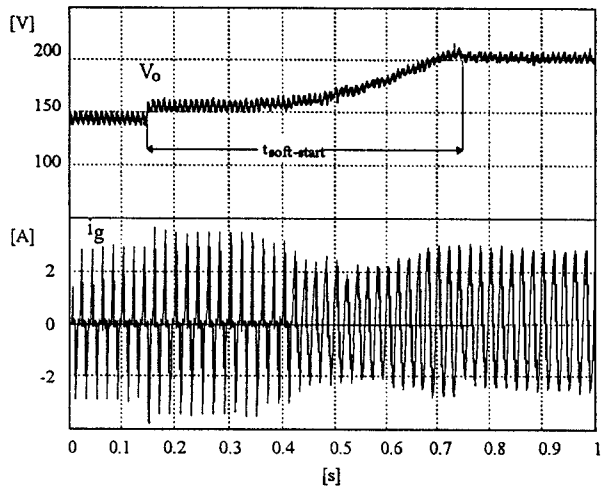

Fig. 15 - Soft start process

voltage from its pre-charged level (≈150V) to its final level of 200V. This was done by slowly increasing the saturation level of the output voltage PI regulator, thus limiting the current surge. The duration of the whole process ($t_{soft-start}$) is about 0.6s.

VII. Conclusions

The paper presents the implementation and test of a fully digital control for a boost PFP. The implementation is done by using the 80C166 micro controller. The paper shows how the higher development cost of the digital implementation is compensated by a significant improvement of the dynamic performances achievable by the converter. The digital approach, in fact, can be effectively exploited in implementing simple compensations for each of the unwanted effects deriving from the limited current and voltage loop bandwidths, which, instead, may be rather complicated in analog implementations.

In particular, the paper discusses the phase leading current absorption from the grid which is due to the current loop limited bandwidth, providing a simple theoretical explanation of it.

Finally, the results of the experimental tests assessing control performance are presented and discussed.

Acknowledgment

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