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Simple digital current control strategy for single-phase grid-connected converters

Majid Sanatkar-Chayjani, Mohammad Monfared

Department of Electrical Engineering, Faculty of Engineering, Ferdowsi University of Mashhad, Mashhad, Iran
E-mail: sanatkar.majid@gmail.com

Abstract: This study proposes a simple digital current control technique for single-phase grid-connected voltage source converters. Unlike conventional strategies, the proposed method does not require any proportional-integral or proportional-resonant controller, fictitious phase generation, reference frame transformation and decoupling network; thus, it has the advantages of simplicity and reduced computational efforts. The suggested digital technique only uses a simple proportional controller in its structure and can be directly implemented on available digital signal processors. A digital controller parameter design procedure is proposed which ensures stability and near-zero steady-state error under all circumstances. Simulation and experimental results confirm that the proposed technique provides a fast and accurate current tracking with minimum harmonic distortions.

1 Introduction

Single-phase voltage source converters (VSCs) are now widely used in grid-interfacing power conditioning applications, such as active rectifiers [1], active power filters [2, 3], power factor correction circuits [4], uninterruptable power supplies [5], photovoltaic systems [6] and fuel cells [7]. In all these applications, besides a regulated power exchange with the grid, the injection of a sinusoidal current to the grid is of major concern [8].

Various current control techniques to realise the high-quality single-phase AC power regulation for VSCs have been proposed. The current hysteresis control (CHC) [9, 10], the voltage oriented control (VOC) in the synchronous reference frame (SRF) [11, 12] and the proportional-resonant- (PR) based control in the stationary reference frame [13, 14] are some of the well-known current control methods. On the other hand, because of the recent advances in digital control techniques and the increasing use of digital signal processors (DSPs), the interest for digital control schemes, such as deadbeat [15], repetitive [16] and predictive [17] raises rapidly. In CHC, which is the easiest method, the AC current is controlled to stay within the limits of an upper and lower band around the sinusoidal reference. The infinite gain of hysteresis comparators provides a high dynamic response. Simple implementation, good stability and automatic current limiting are the advantages, and variable switching frequency is the major drawback associated to the CHC method [8]. The VOC is the most industrial accepted control strategy employed for three-phase applications. In VOC, the control is realised in the SRF through decomposing the AC current into active and reactive components. These current components in the SRF are DC quantities and, as a consequence, the zero steady-state error is ensured using a conventional proportional-integral (PI) controller. The internal current control loops of VOC guarantee high dynamic and static performance. However, the final configuration and performance of this method depends on the quality of the applied PI controllers [11, 12]. In single-phase systems, transferring electrical signals from the stationary to the SRF requires two orthogonal signals. Therefore, to adopt the VOC to single-phase converters, a fictitious phase must be generated. Different techniques to achieve a fictitious phase in single-phase systems have been proposed, such as using a 90° phase shifter [18], Hilbert's transformation [19], all-pass filter [20] and second-order generalised integrator (SOGI) [21]. Unlike the VOC, the PR-based control can track a sinusoidal reference signal in the stationary reference frame without steady-state error [13, 14]. Hence, as the CHC method, the PR is also implemented in the stationary reference frame and no coordinate transformation is required in the current control loop. Despite its simplicity, the PR-based control has several major drawbacks, such as sensitivity to system frequency variations, exponentially decaying response to step changes and great sensitivity and possibility of instability to the phase shift of current sensors [11]. Modern digital control techniques, such as sliding mode, repetitive and predictive, try to maintain the advantages of conventional control strategies, especially VOC, in accurate control with minimum distortion and harmonic noises at the expense of difficult design and implementation, more computational burden and the requirement of a good knowledge of the system parameters.

This paper presents a novel digital current control strategy for single-phase grid-connected VSCs, which is easy to

study and design, and can be simply implemented on typical digital signal controllers. It is shown that the proposed control system is stable and can achieve accurate current tracking with low output current THD without the need for any PI or PR controller, fictitious phase generator and reference frame transformation. Consequently, the proposed method offers a high dynamic performance. While the proposed technique has the benefits of a simpler structure and significant reduction of computations over the VOC, its parameter tuning is a very simple, as well as a straightforward task. The performance is compared with the VOC control strategy in various operating conditions. Comparative simulation and experimental results confirm the superior performance of the proposed method.

2 Structure of the single-phase VSC

The most commonly used structure of single-phase VSC with an AC-side inductive filter and DC-side capacitive energy storage, which is known as the full-bridge converter, is depicted in Fig. 1. It offers bidirectional power flow capability in addition to controlled power factor and low current distortion at AC side with well-regulated DC-link voltage. The current flowing through the filter at $t+\Delta t$ can be written as

$$i(t+\Delta t) = i(t) + \frac{1}{L}\int_{t}^{t+\Delta t} v_L(t')\mathrm{d}t' = i(t) + \Delta I \qquad (1)$$

where v_L is the voltage drop over the filter inductance, Δt denotes the time of each switching state and ΔI is the integral part of the current equation and is defined as the current change during Δt.

2.1 Switching states

In the circuit of Fig. 1, there are $2^4 = 16$ different switching combinations for switches S_1–S_4. To avoid either short circuit on the DC side or open circuit on the AC side of the converter, only four switching states are allowed. In terms of the converter output voltage, v, three distinct states are obvious: (I) S_1 and S_3 or S_2 and S_4 are on and $v=0$, (II) S_1 and S_4 are on and $v=V_{dc}$ and (III) S_2 and S_3 are on and $v=-V_{\mathrm{dc}}$, in which V_{dc} is the DC-link voltage. Current changes relating to the states I–III can be obtained as

$$\begin{cases} \Delta I_{\mathrm{I}} = \dfrac{1}{L}\displaystyle\int_{t}^{t+\Delta t} \big(v_s(t') - r_L i(t')\big)\mathrm{d}t' \\ \Delta I_{\mathrm{II}} = \dfrac{1}{L}\displaystyle\int_{t}^{t+\Delta t} \big(v_s(t') - r_L i(t') - V_{dc}\big)\mathrm{d}t' \\ \Delta I_{\mathrm{III}} = \dfrac{1}{L}\displaystyle\int_{t}^{t+\Delta t} \big(v_s(t') - r_L i(t') + V_{dc}\big)\mathrm{d}t' \end{cases} \qquad (2)$$

where r_L is the equivalent series resistance of the filter, and v_s is the grid voltage. Assuming Δt is a very small time interval, the grid voltage and current can be considered constant during Δt. Hence, the current changes can be simplified and discretised as shown in (3).

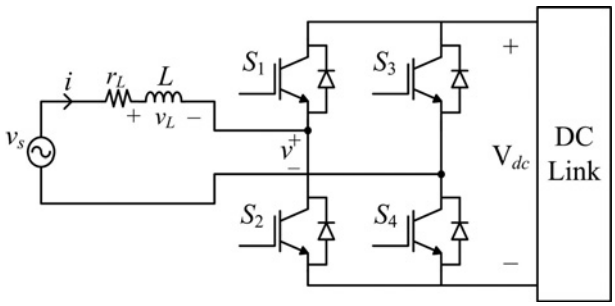

Fig. 1 *Structure of the single-phase full-bridge converter*

$$\begin{cases} \Delta I_{\mathrm{I}} = \dfrac{\Delta t_{\mathrm{I}}}{L}\big(v_s[n] - r_L i[n]\big) \\ \Delta I_{\mathrm{II}} = \dfrac{\Delta t_{\mathrm{II}}}{L}\big(v_s[n] - r_L i[n] - V_{dc}\big) \\ \Delta I_{\mathrm{III}} = \dfrac{\Delta t_{\mathrm{III}}}{L}\big(v_s[n] - r_L i[n] + V_{dc}\big) \end{cases} \qquad (3)$$

In the above equations, Δt_{I}, Δt_{II} and Δt_{III} are the times that the converter remains in states I, II and III, respectively.

2.2 Unipolar sinusoidal pulse width modulation

In single-phase systems, unipolar sinusoidal pulse width modulation has found wide industrial applications, since it offers great implementation simplicity with minimum harmonic distortions. The generation of the gating pulses in the unipolar modulation for both positive and negative reference voltages is illustrated in Fig. 2. The gating pulses are generated by comparing the reference voltage waveform with a high-frequency triangular carrier waveform. The unipolar modulator uses v_{ref} to generate the gating signals for S_1 and S_2 (v_{g1} and v_{g2}), and uses $-v_{ref}$ to generate the gating signals for S_3 and S_4 (v_{g3} and v_{g4}). In Fig. 2, it is assumed that the carrier and sampling frequencies are equal. It can be seen from Fig. 2 that for a positive reference voltage, switching states I and II, and for a negative reference voltage, switching states I and III are used. The switching times for both positive and negative reference voltages can be easily calculated as follows

$$\begin{cases} \Delta t_{\mathrm{I}} = 4t_1 = \left(1 - \dfrac{v_{ref}[n]}{\mathrm{V}_{dc}}\right)T_s \\ \Delta t_{\mathrm{II}} = 2t_2 = \dfrac{v_{ref}[n]}{V_{dc}}T_{\mathrm{s}}, \qquad v_{ref}[n] > 0 \\ \Delta t_{\mathrm{III}} = 0 \end{cases} \qquad (4)$$

$$\begin{cases} \Delta t_{\mathrm{I}} = 4t'_1 = \left(1 + \dfrac{v_{ref}[n]}{V_{dc}}\right)T_s \\ \Delta t_{\mathrm{II}} = 0, \qquad v_{ref}[n] < 0 \\ \Delta t_{\mathrm{III}} = 2t'_2 = -\dfrac{v_{ref}[n]}{V_{dc}}T_s \end{cases} \qquad (5)$$

where T_s is the sampling period. By substituting (4) and (5) into (3), the current changes during each switching state can

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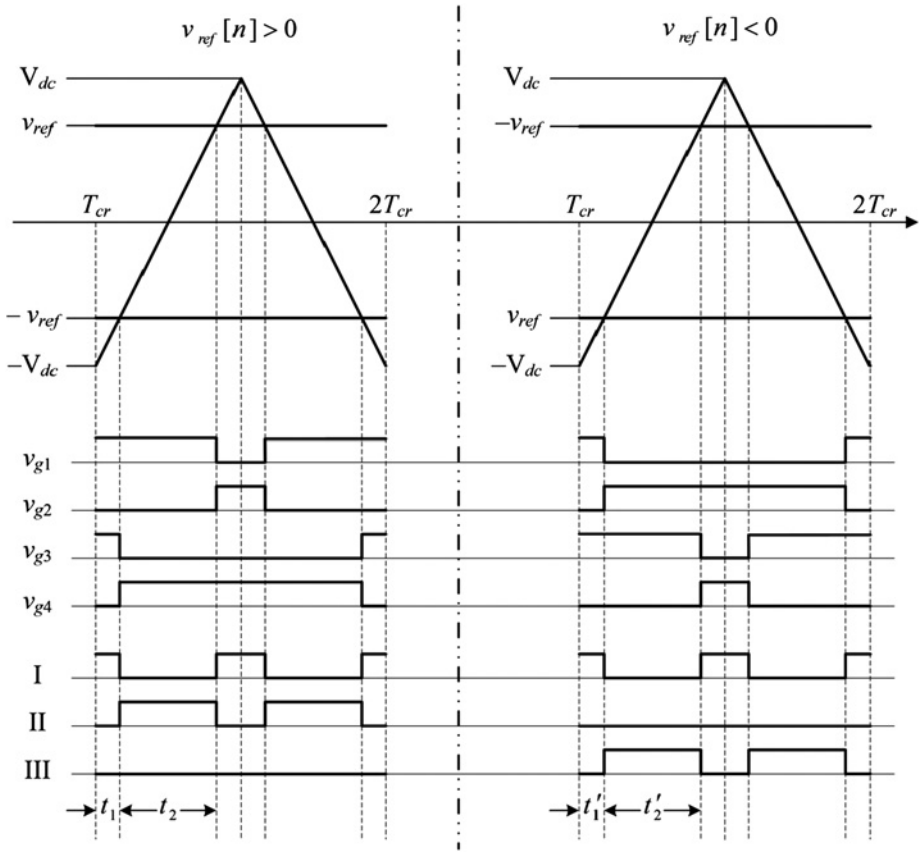

Fig. 2 *Generation of gating pulses by the unipolar modulator*

be computed as

$$\begin{cases} \Delta I_{\mathrm{I}} = \dfrac{T_s}{L}\left(1 - \dfrac{v_{ref}[n]}{V_{dc}}\right)\left(v_s[n] - r_L i[n]\right) \\ \Delta I_{\mathrm{II}} = \dfrac{T_s}{L}\dfrac{v_{ref}[n]}{V_{dc}}\left(v_s[n] - r_L i[n] - V_{dc}\right) \end{cases} \quad v_{ref}[n] > 0 \tag{6}$$

$$\begin{cases} \Delta I_{\mathrm{I}} = \dfrac{T_s}{L}\left(1 + \dfrac{v_{ref}[n]}{V_{dc}}\right)\left(v_s[n] - r_L i[n]\right) \\ \Delta I_{\mathrm{III}} = -\dfrac{T_s}{L}\dfrac{v_{ref}[n]}{V_{dc}}\left(v_s[n] - r_L i[n] + V_{dc}\right) \end{cases} \quad v_{ref}[n] < 0 \tag{7}$$

Using (6) and (7), the total current change between two successive sampling in both positive and negative reference voltages is derived as

$$\begin{aligned} \Delta I &= \Delta I_{\mathrm{I}} + \Delta I_{\mathrm{II}} = \Delta I_{\mathrm{I}} + \Delta I_{\mathrm{III}} \\ &= \frac{T_s}{L}\left(v_s[n] - r_L i[n] - v_{ref}[n]\right) \end{aligned} \tag{8}$$

It is important to note that in (4)–(8) the carrier and sampling periods are assumed to be equal. It can be demonstrated that these equations are true if the sampling of measured quantities and updating the pulse width modulation (PWM) signals are carried out at both peaks and valleys of the carrier waveform ($T_s = T_{cr}/2$, where T_{cr} is the carrier period). These results will be used as a basis for the proposed control algorithm.

3 Proposed digital current error control method

All current control techniques of VSCs, such as the VOC, need the reference current as the input of the control algorithm. Then, the reference voltage of the converter is determined so that the reference current is tracked fast and accurately. Hence, proper determination of the reference current plays an important role in achieving the desired power factor, current distortion and stability of the converter.

3.1 Calculation of reference current

Regulating the converter power exchange with the grid can be readily realised by controlling the phase and amplitude of the converter current. Assuming that $v_s = V_S \sin(\omega t)$ and $i = I \sin(\omega t - \theta_i)$ are the grid voltage and converter current, respectively, the active and reactive powers can be defined as (9). Substituting the active and reactive powers with the corresponding reference values and performing some manipulations, gives the reference current as (10), in which ωt and V_S are provided by a single-phase phase-locked loop (PLL).

$$\begin{cases} P = \dfrac{V_S I}{2}\cos(\theta_i) \\ Q = \dfrac{V_S I}{2}\sin(\theta_i) \end{cases} \tag{9}$$

$$\begin{aligned} i_{ref}(t) &= \frac{2\sqrt{P_{ref}^2 + Q_{ref}^2}}{V_S}\sin\left(\omega t - \arctan\left(Q_{ref}, P_{ref}\right)\right) \\ &= I_{ref}\sin\left(\omega t - \theta_{ref}\right) \end{aligned} \tag{10}$$

Besides its simplicity, providing a pure sinusoidal reference current (in condition that the PLL performs perfectly under non-ideal grid voltages) is another advantage of this method, which as a result the distortion of grid voltage does not appear in the reference current.

3.2 Determining the reference voltage

As mentioned before, the reference voltage for the converter must be determined such that the converter current tracks its reference waveform, as fast and accurate as possible. In the simplest form, that is, in an open-loop control system, the reference voltage can be directly calculated from the voltage equation of the filter which is shown in (11). Substituting the converter current with its reference value and neglecting the inductor resistance r_L, the reference voltage can be obtained in discrete form as (12), where the subscript '*ol*' stands for the open-loop operation.

$$v_s(t) - v(t) = r_L i(t) + L\frac{\mathrm{d}i(t)}{\mathrm{d}t} \tag{11}$$

$$v_{ref,ol}[n] = v_s[n] - L\frac{\mathrm{d}i_{ref}[n]}{\mathrm{d}t} \tag{12}$$

The derivative part of (12) can be calculated using the first-order approximation. This approximation may reduce the speed of the system, especially during transients and load changes. To deal with the problem, given that the reference current of (10) is a pure sinusoidal waveform, it is possible to directly replace the derivative of (10) in (12), and then convert it to the discrete form as

$$v_{ref,ol}[n] = v_s[n] - \omega L I_{ref}\cos(\omega n T_s - \theta_{ref}) \tag{13}$$

The open-loop current control leads to errors in the amplitude and the phase of the converter current. This error mainly arises from modelling errors and uncertainties, such as neglecting the inductor resistance, r_L, the fact that $v_s[n]$ and $v_s(t)$ are equal only at sampling instants, and delays introduced by the analogue-to-digital converters, the program execution and the PWM modulator. To achieve a zero steady-state error, a closed-loop control system is

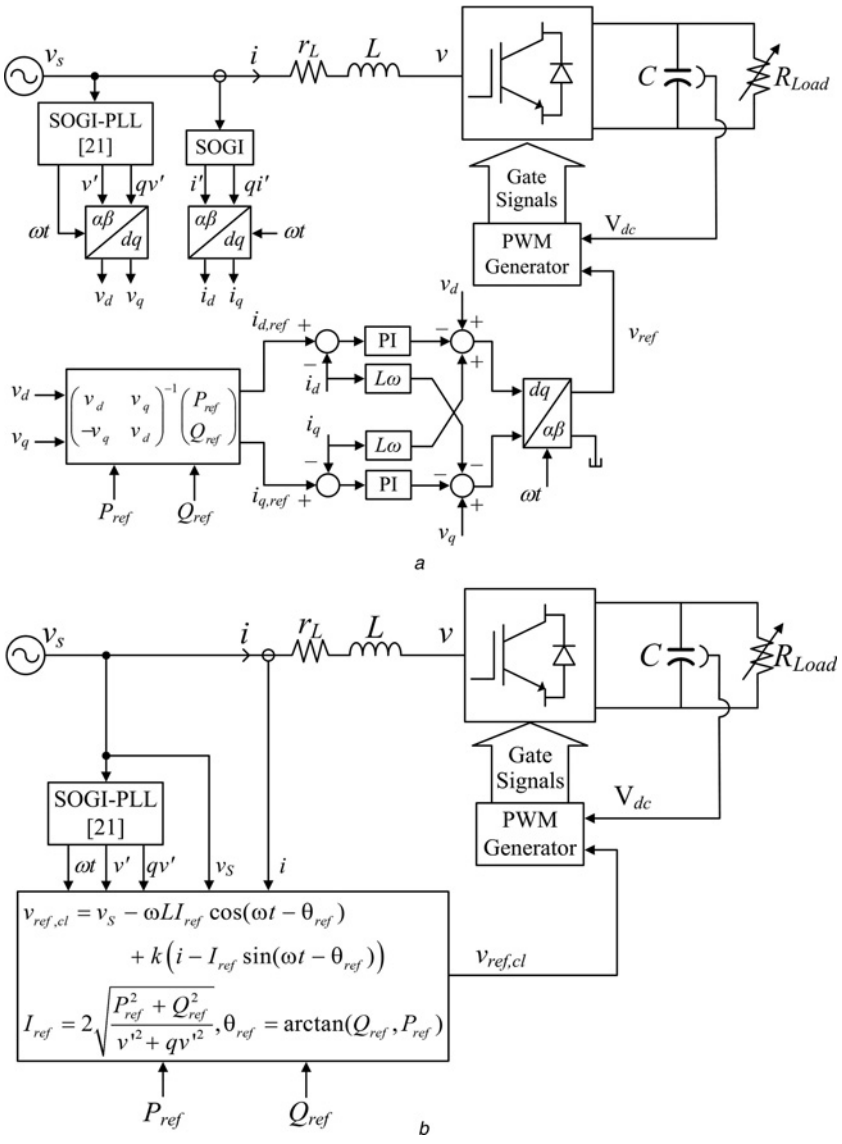

Fig. 3 *Block diagrams of*
a VOC
b DCEC

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Table 1 Comparison of computations per sampling cycle

Operation	VOC	DCEC
addition/subtraction	27	6
multiplication	28	9
division	1	1
sine	2	2
arctangent	0	1
square root	0	1

Table 2 System parameters

Parameter	Symbol	Unit	Value
filter inductance	L	mH	4
filter resistance	r_L	Ω	0.25
DC-link capacitance	C	μF	6000
DC-link voltage	V_{dc}	V	120
grid voltage amplitude	V_S	V	100
grid voltage frequency	$f\,(\omega/2\pi)$	Hz	50
sampling frequency	$f_s\,(1/T_s)$	kHz	5, 10
carrier frequency	$f_{cr}\,(1/T_{cr})$	kHz	5

mandatory. The AC-side current is a suitable feedback signal. To determine the effect of reference voltage changes on the converter current, the derivative of (8) with respect to the reference voltage is calculated as

$$\frac{\partial \Delta I}{\partial v_{ref}} = -\frac{T_s}{L} \tag{14}$$

As it can be seen in (14), under all circumstances, the rate of current change is inversely proportional to the change of the reference voltage. In other words, increasing the reference voltage reduces the converter current and vice versa. On the other hand, the converter current error is defined as

$$\Delta i[n] = i[n] - i_{ref}[n] \tag{15}$$

The current error sign determines whether the measured current is larger or smaller than the reference current. When the current error is positive, a decrease, and when the current error is negative, an increase in the converter current is required. As discussed earlier, an increase (decrease) in the converter current can be accomplished by decreasing (increasing) the converter voltage set-point. As a consequence, the closed-loop reference voltage is proposed to be

$$\begin{aligned} v_{ref,cl}[n] &= v_{ref,ol}[n] + k\Delta i[n] \\ &= v_s[n] - \omega L I_{ref} \cos(\omega n T_s - \theta_{ref}) + k\Delta i[n] \end{aligned} \tag{16}$$

where k is the gain of the closed-loop controller, which must be determined carefully to maintain the closed-loop stability, while ensuring a fast and accurate tracking performance. In the proposed control law of (16), the amplitude and the sign of the current error are both used to modify the open-loop reference voltage. For instance, when the converter current is greater than the reference current, the current error will be positive and the $k\Delta i$ increases the reference voltage; therefore the converter current will be reduced. From the control point of view, the open-loop term, $v_{ref,ol}$, reduces the feedback control effort, and offers faster and at the same time smoother transient responses, especially at start-ups. Simplified block diagram of the proposed digital current error control (DCEC) method, as well as the VOC strategy, is shown in Fig. 3. As depicted, the VOC utilises the SOGI technique to generate the fictitious phase signal. Furthermore, in practical implementation, the VOC is digitised using the trapezoidal approximation. A rough comparison of computational effort between the DCEC method and the VOC is summarised in Table 1. To make a clear comparison, common blocks between two techniques,

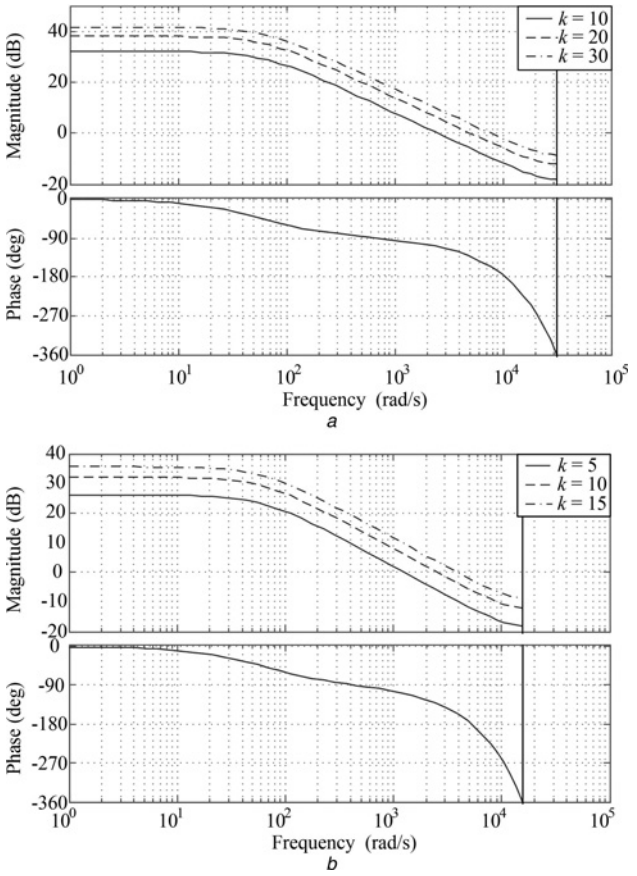

Fig. 5 *Bode plots of $G_{ol}(z)$ for three different values of k*
a $T_s = T_{cr}/2$
b $T_s = T_{cr}$

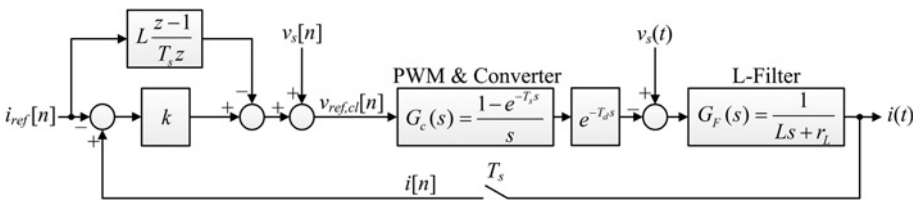

Fig. 4 *Block diagram of the closed-loop converter system in the mixed continuous-discrete domain*

such as the PLL and the PWM generator, are excluded. Obviously, the proposed technique enjoys significant reduction of the computations per sampling cycle over the VOC.

4 Stability and steady-state error analysis

In this section, an analysis of stability and steady-state error to determine the valid range of parameter k is performed. Using the voltage equation of filter (11) in Laplace domain and closed-loop reference voltage (16), the block diagram of the entire system in the mixed continuous-discrete domain can be depicted as Fig. 4. The PWM modulator and the converter at the fundamental frequency are readily modelled as a zero-order hold transfer function $G_c(s)$. The sampling and calculation time of the discrete control system are included in this model as a pure time delay, T_d.

The system of Fig. 4 is a sampled-data analogue system. Although the output, $i(t)$, is continuous in time, having a sampler in the feedback path, the analogue system essentially becomes a digital system with the pulse transfer function, $G_{fp}(z)$

$$G_{fp}(z) = \frac{i(z)}{v_{ref,cl}(z)} = \left(1 - z^{-1}\right) \mathcal{Z}\left\{ \mathrm{e}^{-T_d s} \frac{G_F(s)}{s} \right\} \tag{17}$$

where $\mathcal{Z}$ denotes the z-transform.

The closed-loop response of the output current in the z-domain considering the grid voltage effect can be computed as

$$\begin{aligned} i(z) = {} & \frac{\left(L\left((z-1)/T_s z\right) + k\right) G_{fp}(z)}{1 + kG_{fp}(z)} i_{ref}(z) \\ & - \frac{G_{fp}(z)}{1 + kG_{fp}(z)} v_s(z) + \frac{\mathcal{Z}\left\{v_s(s) G_F(s)\right\}}{1 + kG_{fp}(z)} \end{aligned} \tag{18}$$

To attain an appropriate and stable performance of the closed-loop system, the computation time of the control strategy must be less than one sampling period. In most DSPs, the PWM register can be updated at both peaks and valleys of the carrier signal; thus, when the computation time is less than half of the carrier period, the sampling of measured quantities and updating the PWM registers are performed on both peaks and valleys of the carrier waveform. In both once or twice sampling in a carrier period, the delay is equal to one sampling period. The converter pulse transfer function, $G_{fp}(z)$, considering $T_s = T_{cr}$ and $T_s = T_{cr}/2$ can be calculated from (17) as

$$G_{fp}(z) = \frac{\left(1 - \mathrm{e}^{-(r_L/L)T_s}\right)}{r_L z\left(z - \mathrm{e}^{-(r_L/L)T_s}\right)} \tag{19}$$

4.1 Stability analysis

To ensure stability, all poles of the closed-loop transfer function must lie inside the unit circle. The bilinear transformation $z = (1 + w)/(1 - w)$ transforms the inside of the unit circle to the left-half plane and allows applying the Routh–Hurwitz stability criterion to the characteristic polynomial of (18), that is, $1 + kG_{fp}(z)$, which gives the following stability range for the parameter k

$$-r_L < k < \frac{r_L}{1 - \mathrm{e}^{-(r_L/L)T_s}} \tag{20}$$

Using the first-order Pade approximation and assuming that r_L can be neglected and the sampling frequency is high enough, the range of stable k can be approximated as

$$0 < k < \frac{L}{T_s} \tag{21}$$

As it can be seen in (21), the range of admissible values

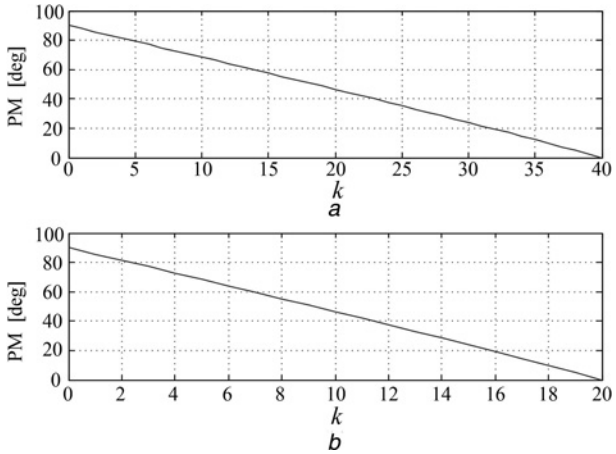

Fig. 6 *PM as a function of k*
a $T_s = T_{cr}/2$
b $T_s = T_{cr}$

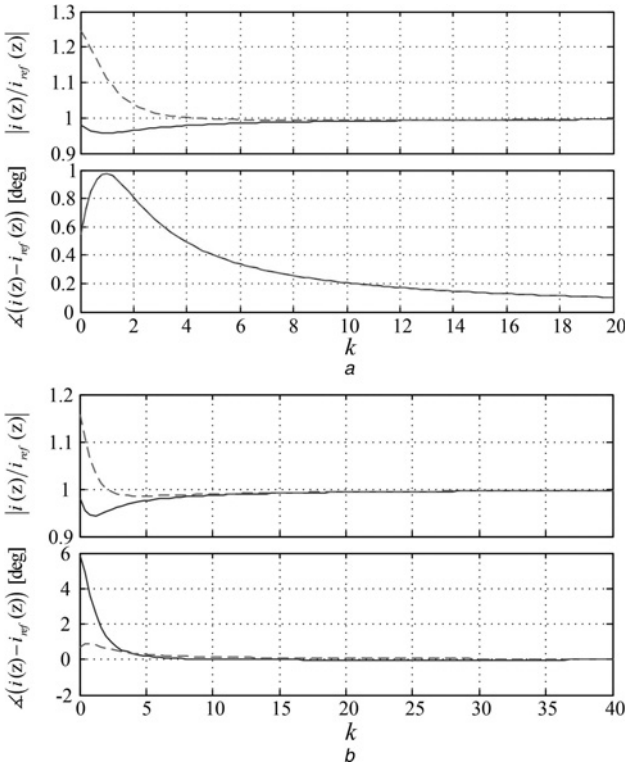

Fig. 7 *Magnitude ratio and phase difference between i(z) and i_{ref} (z) at the fundamental frequency as a function of k; ignoring (solid line) and taking account (dashed line) of $G_2(z)v_s(z)$ and $i_v(z)$ terms*
a $T_s = T_{cr}/2$
b $T_s = T_{cr}$

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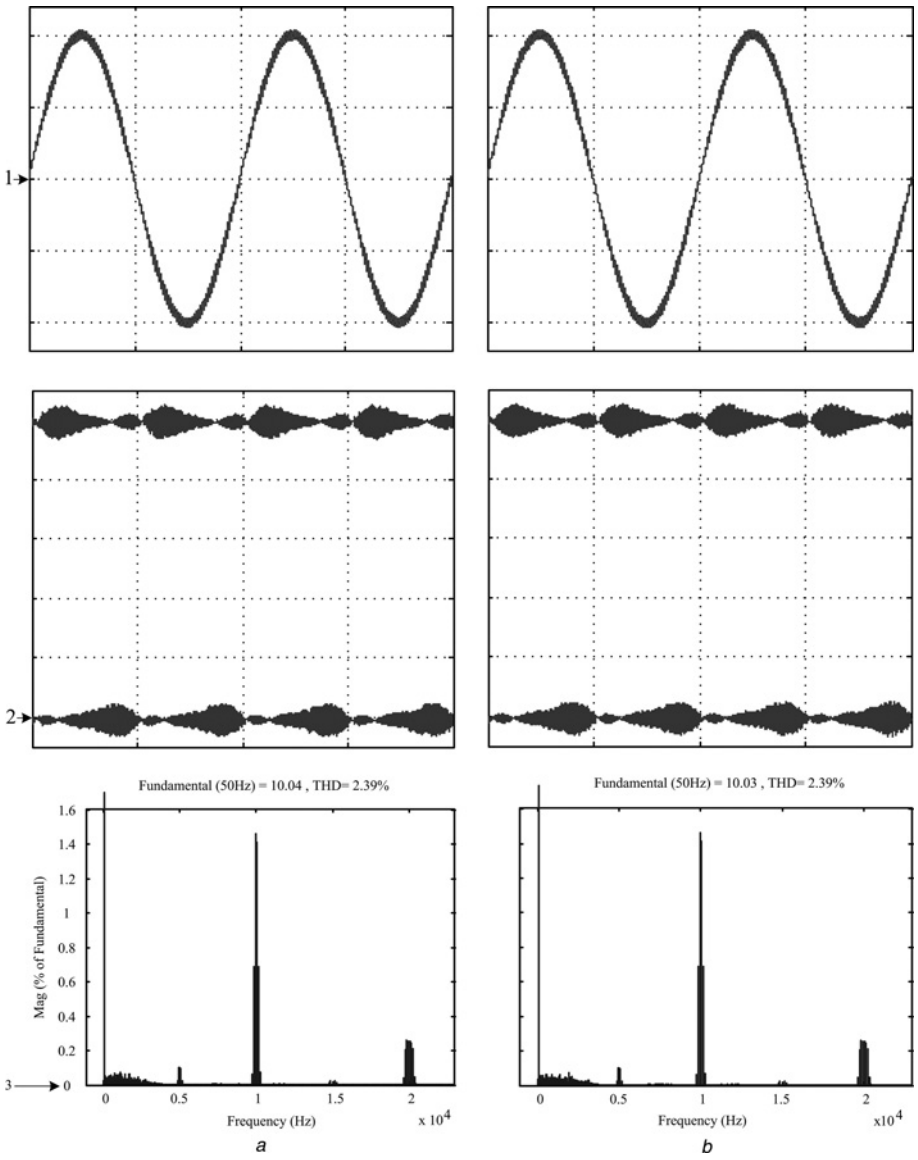

Fig. 8 *Steady-state simulated waveforms: $P_{ref} = 500$ W, $Q_{ref} = 0$ VAr*

1. Converter current (*x*-axis 50 ms/div, *y*-axis 5 A/div), 2. active and reactive powers (*x*-axis 50 ms/div, *y*-axis 100 W(VAr)/div), 3. current harmonic spectrum
a VOC
b DCEC

for the parameter k is independent of the loading conditions and only dependents on the sampling frequency and the inductor value. With a higher inductor value and a smaller sampling period (a higher sampling frequency), a wider range for k, and as a consequence, decreased control system sensitivity to the inductance variations/uncertainties is possible. Evaluating (21) with parameters of Table 2 establishes an upper limit of 40 ($T_s = T_{cr}/2$) and 20 ($T_s = T_{cr}$) for k.

The degree of stability can be examined from the open-loop transfer function $G_{ol}(z) = kG_{fp}(z)$. Fig. 5 shows the open-loop Bode plots for different values of k. It can be concluded from the plots that increasing the gain k improves the open-loop gain at the fundamental frequency (i.e. the steady-state error is reduced which will be addressed in the next subsection); however, the increase of k deteriorates the phase margin (PM) of the system. The choice of k is a compromise between the steady-state error and PM. Using the bilinear transformation and approximations mentioned earlier, PM can be calculated as

$$\mathrm{PM} = \tan^{-1}\left(\sqrt{\left(\frac{2L}{kT_s}\right)^2 - 1}\right) - \tan^{-1}\left(\frac{2\sqrt{(2L/kT_s)^2 - 1}}{(2L/kT_s)^2 - 2}\right) \tag{22}$$

Fig. 6 shows the PM as a function of k. As expected, the values beyond the constraints of (21) lead to negative PMs. A proper range for PM is $30° < \mathrm{PM} < 60°$, which translates to $10 < k < 24$ and $7 < k < 14$ for $T_s = T_{cr}/2$ and $T_s = T_{cr}$, respectively.

4.2 Steady-state error

The steady-state error of the closed-loop system is investigated in this section. Equation (18) is used to

examine the steady-state error of the converter current. For simplicity, this equation can be rewritten as (23). From Fig. 4 it is evident that when ideally T_d and T_s are both zero, the second and third terms of the right-hand side of (23) cancel out each other exactly (a perfect feedforward of grid voltage is achieved), so the closed-loop response is determined from the first term $G_1(z)i_{ref}(z)$. However, in practice because of the delay T_d and the fact that $v_s[n]$ and $v_s(t)$ are equal just at sampling instants, $G_2(z)v_s(z)$ and $i_v(z)$ make an impact on the steady-state performance. Fig. 7 studies the effect of last two terms of (23) on the steady-state magnitude and phase error of the converter current at the fundamental frequency. Ignoring $G_2(z)v_s(z)$ and $i_v(z)$ terms brings a large error in predicting the current tracking performance for small values of k. Thus it can be stated that for small values of k, $G_1(z)$ lonely cannot correctly show the performance of the system in the steady state. Eventually, as it can be seen in Fig. 7, the current error is large for $k = 0$ which corresponds to the open-loop operation, while increasing k causes the magnitude and phase errors decrease drastically and in the decided range for k to obtain a proper PM, these errors are very small and almost zero steady-state error is yielded.

$$i(z) = G_1(z)i_{ref}(z) - G_2(z)v_s(z) + i_v(z) \tag{23}$$

5 Simulation and experimental verification

The performance of the proposed DCEC technique is evaluated and the results are compared with those of the most well-known existing scheme, that is, the VOC through simulations in MATLAB®/Simulink®. As mentioned before, the performance of the VOC depends on the quality of the applied PI controllers. The tuning of PI controllers is done based on the system stability and speed of system response. The system stability and smooth transient response are guaranteed by appropriate selection of PM, which in this study is chosen to be the same as the DCEC technique. To achieve a fast dynamic response and proper switching noise rejection, a bandwidth in the range of $f_s/8$–$f_s/4$ is suggested for the VOC, which $f_s/4$ is chosen here to attain the maximum dynamic of VOC. Tuning of parameters for both methods is done considering $T_s = T_{cr}/2$. The system parameters are listed in Table 2.

Fig. 8 compares the steady-state waveforms of VOC and DCEC. The sinusoidal current with low THD_i and the regulated active and reactive powers of DCEC confirm that it can successfully achieve the excellent performance of VOC, while taking benefit of a simpler structure.

Unlike the three-phase system, in the single-phase system, the instantaneous and the average powers are not equal and are related together by (24) [22]. The dynamic performance of the converter with the VOC and the DCEC in terms of the instantaneous power is presented in Fig. 9, where several step changes in the power commands are conducted. These waveforms show the faster and smoother transient performance of the DCEC compared with the VOC.

$$p(t) = v_s(t)i(t) = P\big(1 - \cos(2\omega t)\big) - Q\sin(2\omega t) \tag{24}$$

Finally, an experimental test rig is developed to confirm the effectiveness of the proposed control scheme. The control methods are implemented on a single-chip DSP TMS320F28335 from Texas Instruments. The parameters of the experimental prototype are the same as simulations. The converter utilises a unipolar PWM modulator with 5 kHz carrier frequency. All sampling and computation times of the proposed method are lower than $T_{cr}/2$ (i.e. 100 μs), so $T_d = T_{cr}/2$. The value of k is chosen to be 19, which gives PM of 40° and the steady-state peak error of 0.7%.

Fig. 10 shows the steady-state waveforms of the VOC and the proposed DCEC method with 500 W and 0 VAr power commands. Even though the AC voltage is polluted with harmonics, highly sinusoidal currents are injected into the grid with measured THD_i of 2.9% for both methods. The results are in good agreement with the simulated steady-state waveforms. Indeed, the high-quality steady-state waveforms confirm that the performance of the DCEC is comparable with the conventional VOC method in providing high-quality sinusoidal currents.

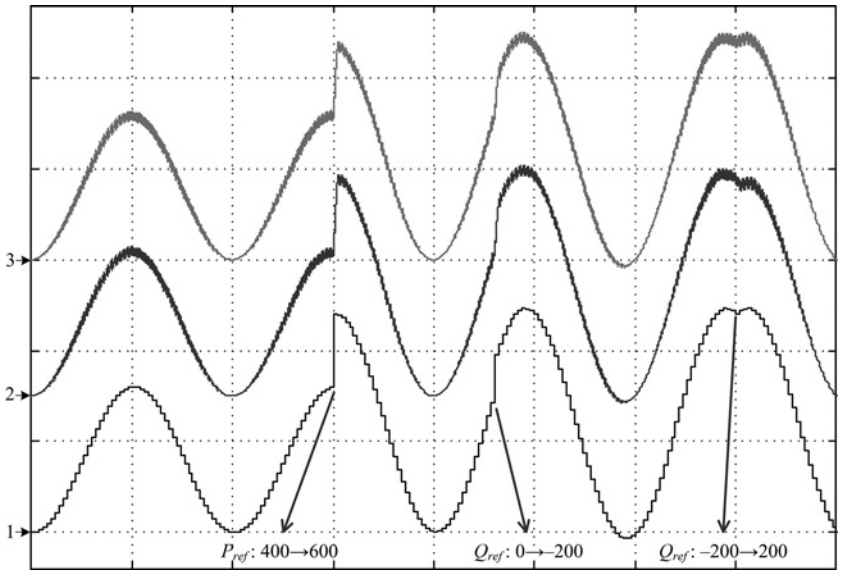

Fig. 9 *Instantaneous power simulated waveforms in response to several step changes in power commands*
1. Reference, 2. VOC, 3. DCEC (x-axis 50 ms/div, y-axis 500 VA/div)

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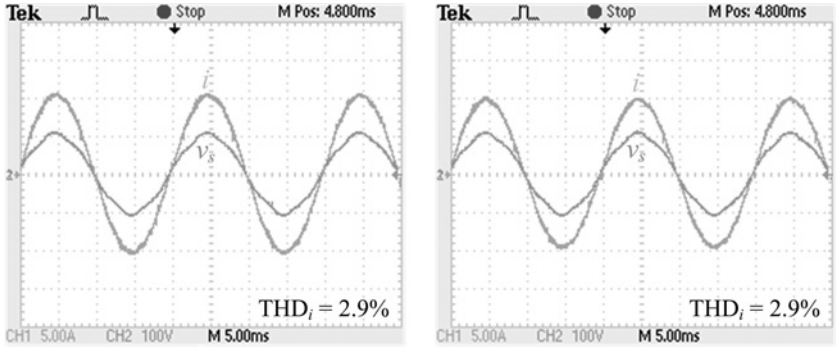

Fig. 10 *Steady-state converter current and grid voltage: P_{ref} = 500 W, Q_{ref} = 0 VAr*
a VOC
b DCEC

The transient waveforms of the single-phase converter in response to step changes of reference powers are presented in Fig. 11. It can be noted that both methods offer a fast transient response while the DCEC benefits from fewer transient oscillations.

As described in (16), the DCEC method requires the inductance value to calculate the closed-loop reference voltage. Therefore it is necessary to examine the influence of the inductance mismatch on the performance of the conveter. Fig. 12 shows the experimental results of the converter under unity power factor operation considering the mismatch. The active and reactive powers and the THD$_i$ are measured with the 'TPS2PWR1 power analysis application key' for the 'Tektronix oscilloscope'. The S_{err}% is defined as

$$S_{err}\% = \sqrt{\frac{\left(P - P_{ref}\right)^2 \left(Q - Q_{ref}\right)^2}{P_{ref}^2 + Q_{ref}^2}} \times 100 \qquad (25)$$

As one can see, the proposed method can successfully maintain the power error and the current THD small even under large mismatches in the inductance value. These results are a direct consequence of adding the $k\Delta i[n]$ term to the current control law of (16). Low dependence to the

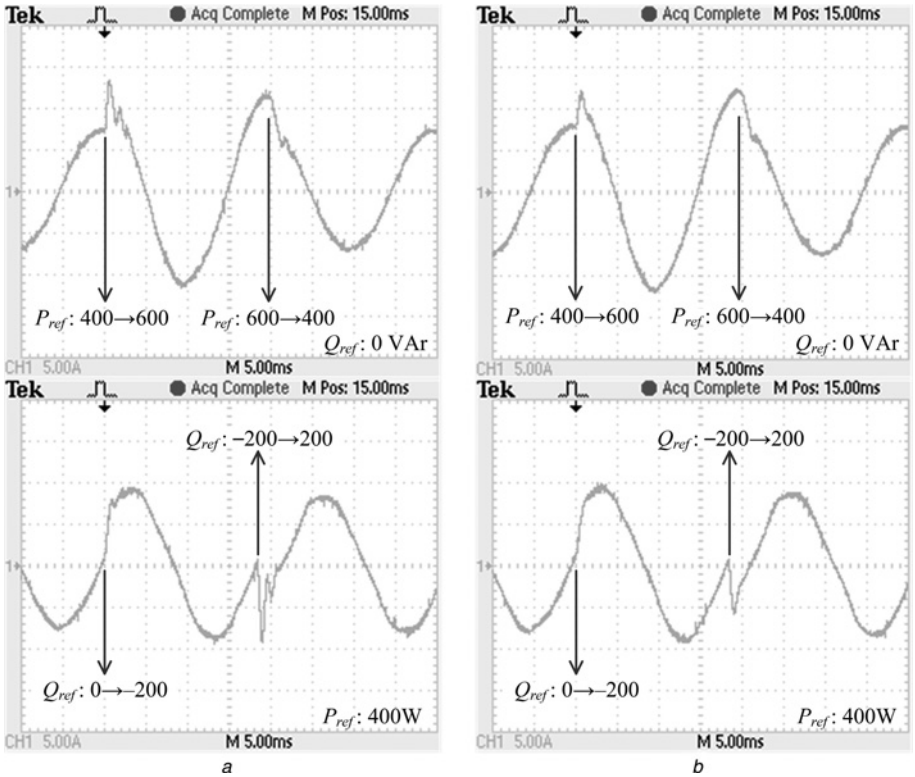

Fig. 11 *Converter current during step changes in the active and reactive power references*
a VOC
b DCEC

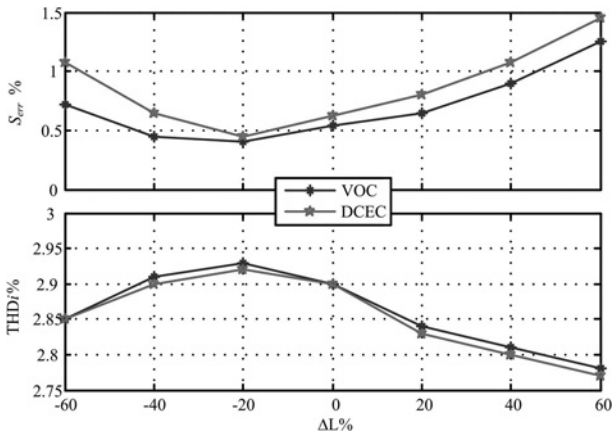

Fig. 12 *Effect of inductance mismatch on the converter current THD and the steady-state power error (P_{ref} = 500 W, Q_{ref} = 0 VAr)*

system parameters ensures the robustness of DCEC method under wide parameter mismatches.

6 Conclusions

The authors proposed a new stationary reference frame digital current control for single-phase VSCs that offer many unique features such as:

- simple algorithm besides strong theoretical background;
- highly suited for digital implementation with considering digital control problems like delays;
- no decoupling network, fictitious phase generator and reference frame transformation are required and the reference converter voltage in each sampling period is computed based on measurements and system parameters, directly;
- no PI or PR controllers are required, and it is analytically proven that the proposed technique ensures stability and a sufficiently small steady-state error using a simple proportional controller;
- higher dynamic performance because of the fast control strategy.

Besides, the simulation and experimental results confirm the superiority of the proposed DCEC scheme in comparison with the conventional VOC technique in providing sinusoidal currents with less harmonic contents and a faster and smoother transient response. Also, the converter parameter mismatch has negligible effect on THD_i and power tracking performance of the proposed technique.

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