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Simple Technique to Improve Essentially the Performance of One-Stage Op-Amps in Deep Submicrometer CMOS Technologies

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Abstract: A comparative study of one-stage-amp performance improvement based on simulations in 22 nm, 45 nm, 90 nm, and 180 nm in deep submicrometer CMOS technologies is discussed. Generic SPICE models were used to simulate the circuits. It is shown that in all cases a simple modification using resistive local common mode feedback increases open-loop gain and gain-bandwidth product, peak output currents, and slew rate by close to an order of magnitude. It is shown that this modification is especially appropriate for its utilization in current CMOS technologies since large factor improvements were not available in previous technologies. The OTAs with resistive local common mode feedback require simple phase lead compensation with a very small additional silicon area and keep supply requirements and static power dissipation unchanged.

Keywords: resistive local common mode feedback; class AB CMOS op-amps; mixed-signal circuits

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1. Introduction

Deep submicrometer CMOS technologies use sub-volt supply voltages that do not allow the use of cascode transistors in the output branch of op-amps. This is due to the fact that as feature sizes have decreased threshold voltages have not scaled down at the same rate as the supplies and they are a significant fraction of the supply voltages in current CMOS technologies. For this reason, cascode transistors in the output branches would seriously limit the output signal swing and are avoided. The lack of cascode transistors leads to low open-loop gains A_{ol} in one-stage op-amps (also denoted OTAs) on the order of $A_{ol} = g_m r_o/2 = A/2$, where g_m is the small signal transconductance gain, r_o the output resistance and $A = g_m r_o$ the intrinsic gain of a MOS transistor in a given technology. The resulting open-loop gain of a non-cascoded gate-driven one-stage op-amp (Figure 1a) is only typically around 25–30 dB. This results in op-amps with very poor accuracy since the open-loop gain of an op-amp determines its accuracy for closed loop applications. Two-stage Miller op-amps can be used to overcome the problem and to achieve a higher open-loop gain $A_{ol} = [(g_m r_o)^2]/2$ (approximately 50–60 dB) but they require an area-intensive Miller compensation capacitance C_c whose value is typically similar to the load capacitance $C_c = C_L$. Nested Miller compensated multistage op-amps can achieve higher open-loop gains but require complex compensation schemes which limit seriously their gain-bandwidth product or GB [1] and also require several silicon area-intensive capacitances. Assuming a typical design with $C_c = C_L$, both, one- and two-stage op-amps are characterized by a gain-bandwidth product given by the same expression $GB = (1/2\pi)(g_m/C_L)$ [2]. In [3], a very simple scheme using resistive local common mode feedback (RLCMFB) was used to increase A_{ol} and GB of a non-cascoded

one-stage op-amp and at the same time to provide efficient class AB operation. At the time the RLCMFB technique was introduced, only modest improvement could be achieved due to the relatively large feature sizes that MOS transistors had in those technologies. In this paper, we show that the RLCMFB technique allows essential OTA improvement in current submicrometer CMOS technologies. Section 2 of the paper discusses the basic aspects of the RLCMFB technique. Section 3 shows simulations of conventional and OTAS with RLCMFB in four submicromenter CMOS technologies. These simulations verify essential improvements in all figures of merit of non-cascoded OTAs with RLCMFB. Section 4 shows two comparison tables; one summarizing the simulation results of Section 3 and the second one comparing the OTA with RLCMFB to several recently published OTAs. Section 5 provides conclusions.

2. OTAs with Resistive Local Common Mode Feedback

The resistive local common mode feedback (RLCMF) technique uses resistors R in the input stage load (Figure 1b). It requires phase lead compensation to mitigate the effect on the OTA phase margin of the phase shift associated with high-frequency poles at nodes a,b introduced by the resistive local common mode feedback elements. Phase lead compensation uses just a resistor R_s in series with the output terminal to generate a zero with value $\omega_z = 1/(RsC_L)$ that approximately cancels the phase shift of poles at nodes a,b. These poles have values $\omega_{pa,b} = 1/(RC_{PARa,b})$ where $C_{PARa,b}$ is the parasitic capacitance at nodes a,b. In this case, the op-amp performs approximately as a one-pole system with a (dominant) pole at the output node $\omega_{pout} = 1/(R_{out}C_L) = 1/((r_o/2)C_L)$. Resistive local common mode feedback with phase lead compensation leads to an open-loop gain enhanced by the factor $K_{enh} = gm(R||r_{o1}||r_{o2})$ according to: $A_{ol} = K_{enh}g_m r_o/2$ and also to an enhanced gain bandwidth product GB = $A_{ol}\omega_{pout} = (1/2\pi)[K_{enh}g_m/C_L]$. This is a factor K_{enh} higher than for conventional one- and two-stage op-amps. The resistive (and capacitive) local common mode feedback technique has been used extensively [4–9] to improve the performance of analog circuits, e.g., in the design of super class AB op-amps [5]. In previous CMOS technologies, the improvement factor K_{enh} of A_{ol} and GB was limited to a relatively low value (few dB) due to the large minimum transistor feature sizes that introduced relatively large parasitic capacitances $C_{PARa,b}$ at nodes a and b. The large R required to achieve high K_{enh} values would lead to relatively low pole frequencies $\omega_{pa,b}$ < GB that were difficult to cancel using phase lead compensation. In this paper, we show that the approach published in [3] is especially appropriate to enhance by relatively large factors K_{enh} (>10) the open-loop gain A_{ol}, the gain-bandwidth product GB and the slew-rate SR of op-amps in modern deep submicrometer CMOS technologies. The reason being that with the reduction in feature sizes, parasitic capacitances $C_{PARa,b}$ at nodes a and b have very small values in current CMOS technologies, and even with relatively large R values, (comparable to r_o) that lead to large K_{enh} factors, the poles $\omega_{pa,b}$ at nodes a, b remain at relatively high. In this case, their phase shift (that decreases the phase margin) can be easily compensated with a phase lead compensation resistors R_s. This resistor is on chip and introduces a high frequency zero at $\omega_z = 1/(R_sC_L)$ whose phase shift improves the phase margin of the OTA as discussed in [3]. No accurate matching of ω_z and ω_{pab} is required to achieve sufficient OTA phase margin. Given that ω_z and ω_{pab} are both at frequencies higher than GB (factor 1 to 3) the pole-zero doublet does not cause long settling times as explained in [10].

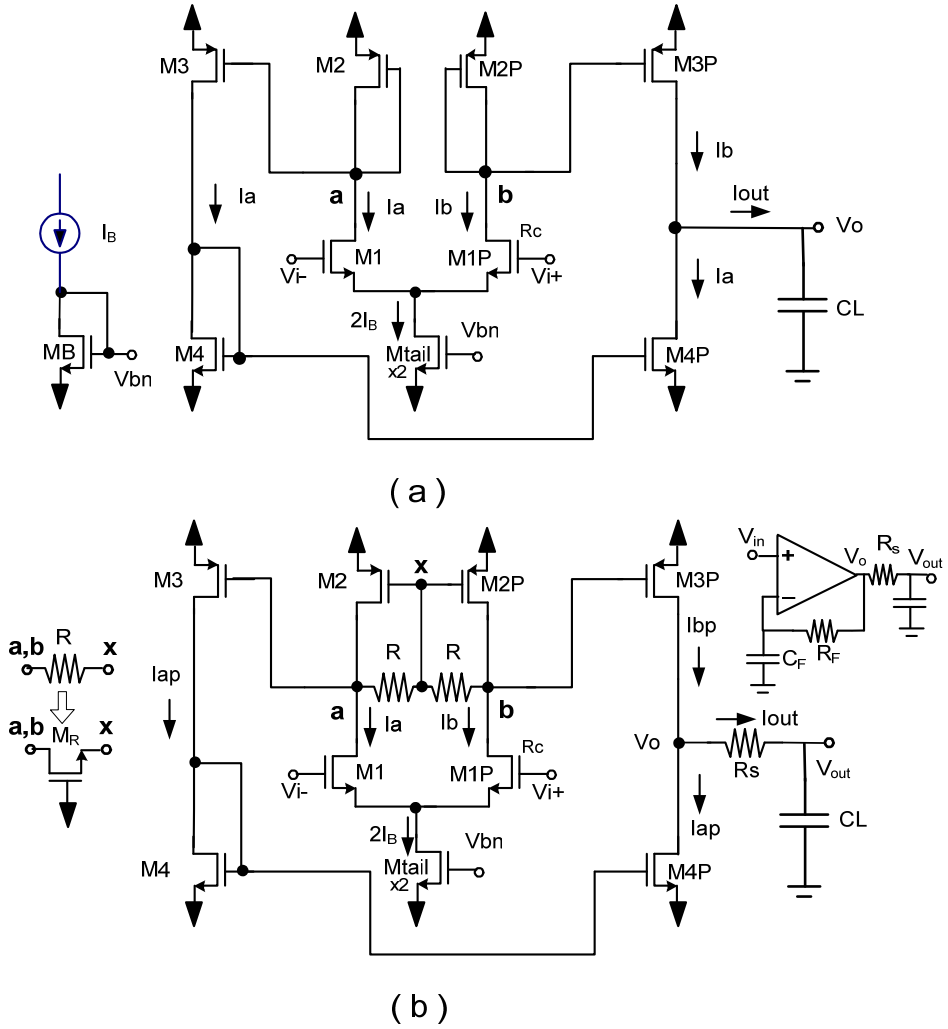

Figure 1. (**a**) Conventional one-stage op-amp without cascoding transistors. (**b**) One-stage op-amp with resistive local common mode feedback.

3. Simulation Results

A comparison among several simulations was made using 22 nm, 45 nm, 90 nm, and 180 nm CMOS technologies. The simulations in 22 nm, 45 nm, and 90 nm were performed with generic models available from North Carolina State University [11]. The simulations in 180 nm were performed using parameters of a TSMC commercial technology available through MOSIS [12]. In all cases, the bias current per branch is I_B = 2.5 µA; therefore, the total quiescent current per circuit is I_{totQ} = 10 µA. For all circuits, PMOS and NMOS transistors had dimensions W = 10 µm and L = $2L_{min}$, where L_{min} is the minimum feature size of the technology, also in all cases, the load capacitance was C_L = 2pF. The simulated open-loop AC responses are depicted in Figure 2 for 22 nm. In this case, a value R = 500 kΩ was used. The trace v(vo_cnv) refers to the conventional topology of Figure 1a and v(vo) to the enhanced topology with resistive local common mode feedback of Figure 1b. Transistors operate in subthreshold and since they have the same bias currents their transconductance gains are similar. Values of resistors R were selected to obtain similar enhancement factors K_{enh} in all cases. The values of resistors R are not equal in all technologies since the output conductance of the transistors (which also affects K_{enh} as discussed in Section 2) are different in each technology. Simulations of the open-loop gain were performed by connecting a large valued feedback element R_F (100 MΩ) from the output of the op-amp Vo (at the junction of the drains of M3P, M4P, and R_s) to the negative input as shown in Figure 1b. A grounded large valued grounded capacitance (C_F = 1F) was connected to

the OTA negative input terminal. The open-loop response displayed corresponds to the magnitude and phase of the voltage at the node labeled Vo in Figure 1.

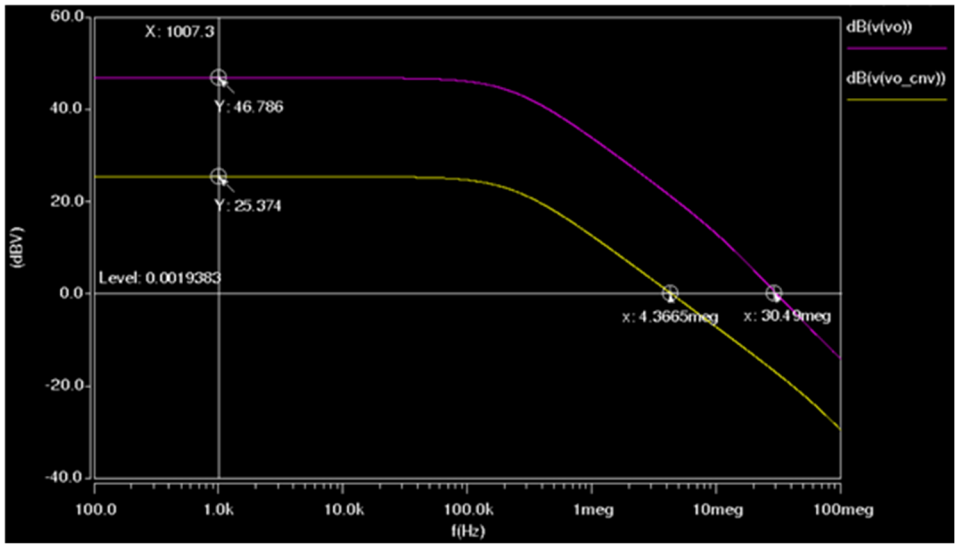

Figure 2. AC open-loop response in 22 nm.

AC simulations of the op-amp open-loop response for 45 nm, 90 nm, and 180 nm are shown in Figures 3–5, respectively. The open-loop gain test setup using a very large resistive element RF = 100 MΩ and capacitor CF = 1F is shown in Figure 1b. Values R = 300 kΩ were used for 45 nm and 90 nm CMOS technologies. Values R = 500 kΩ were used for 180 nm CMOS technologies. In all cases, as it is common practice to save silicon area, resistors were implemented with transistors M_R in triode mode as shown in Figure 1b. All of them with noticeable enhancements in A_{ol} and GB for the op-amps with resistive local common mode feedback.

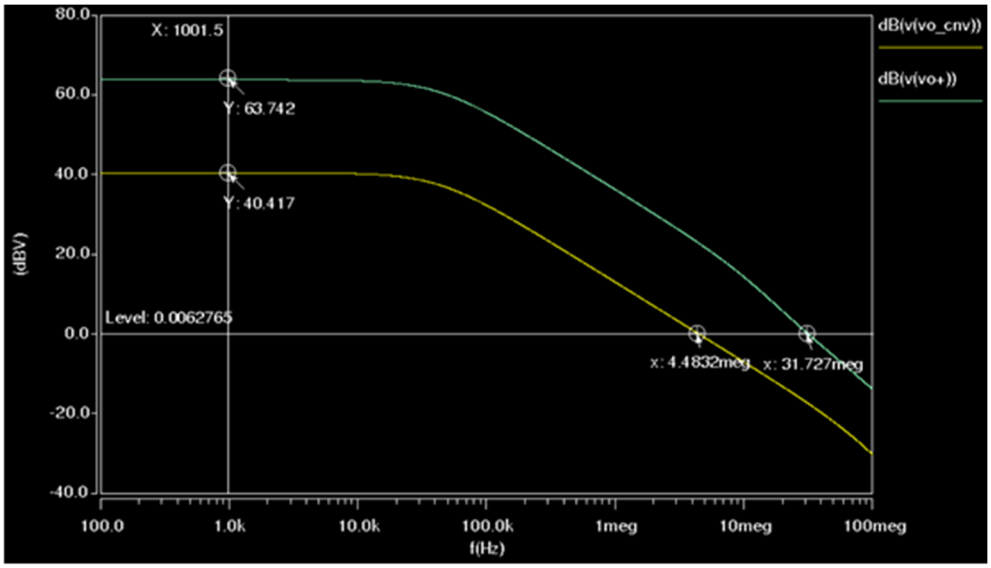

Figure 3. AC open-loop response in 45 nm.

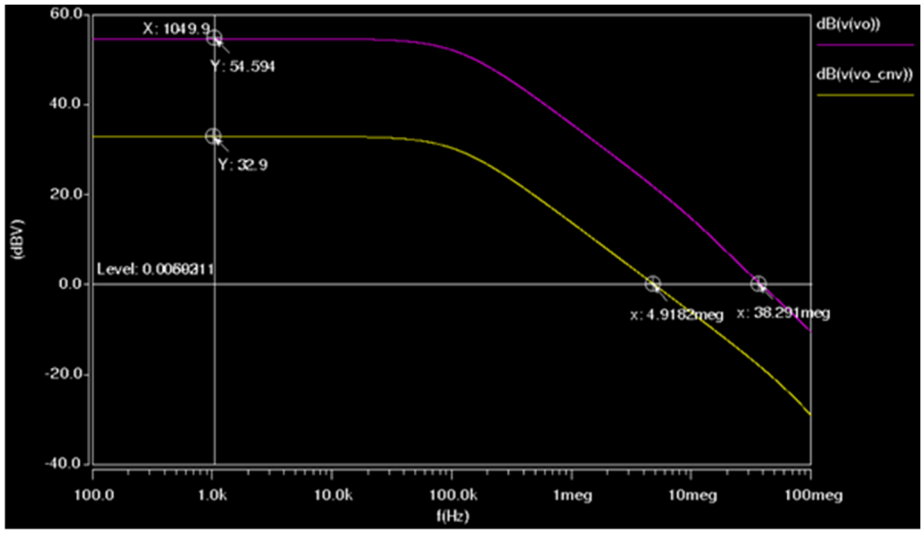

Figure 4. AC open-loop response in 90 nm.

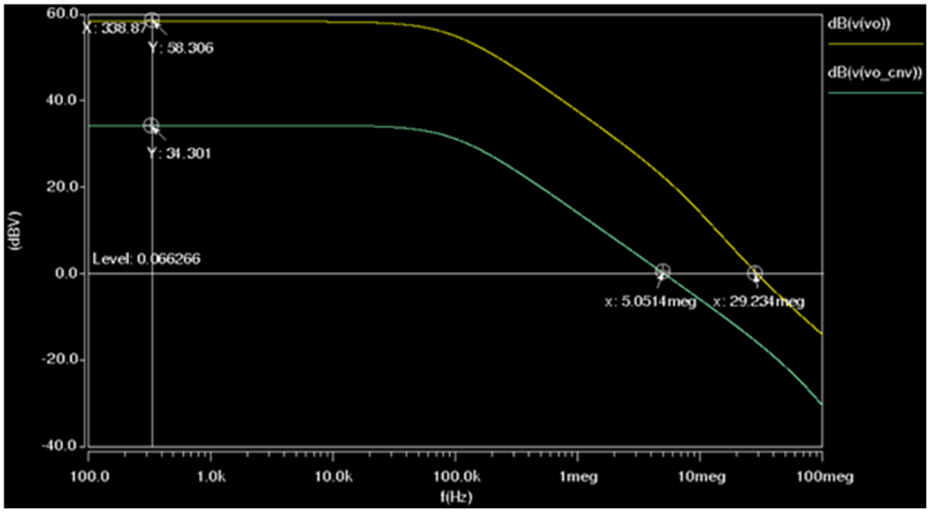

Figure 5. AC open-loop response in 180 nm.

AC simulation results of the op-amps in voltage follower configuration (by connecting directly the output labeled V_o in Figure 1b to the negative op-amp input), are depicted in the same technologies, in Figures 6–9. In all cases, the AC response of the voltage at the terminal labeled V_{out} in the circuits of Figure 1b and V_o in Figure 1a (at the ungrounded terminal of C_L) is displayed. As can be noticed, the voltage follower bandwidth is improved by 5 to 10 times w.r.t those without resistive local common mode feedback.

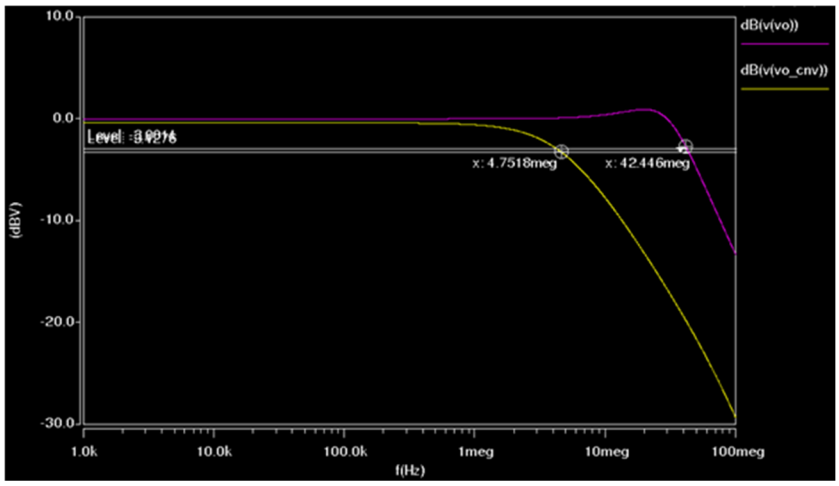

Figure 6. AC voltage-follower responses in 22 nm.

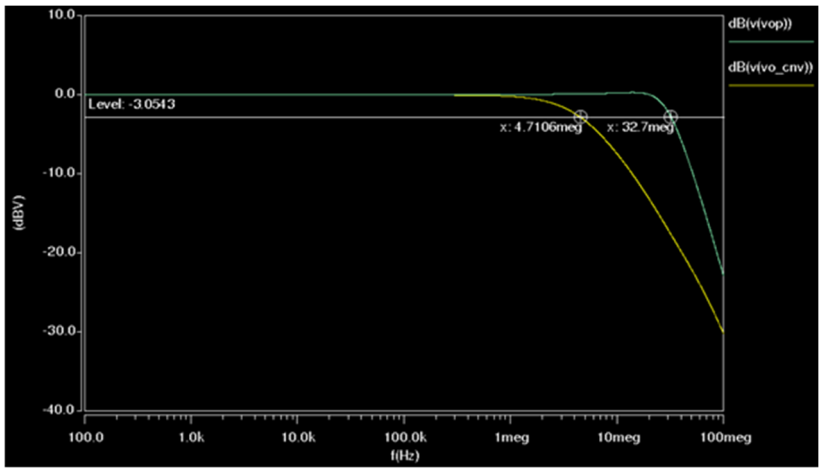

Figure 7. AC voltage-follower responses in 45 nm.

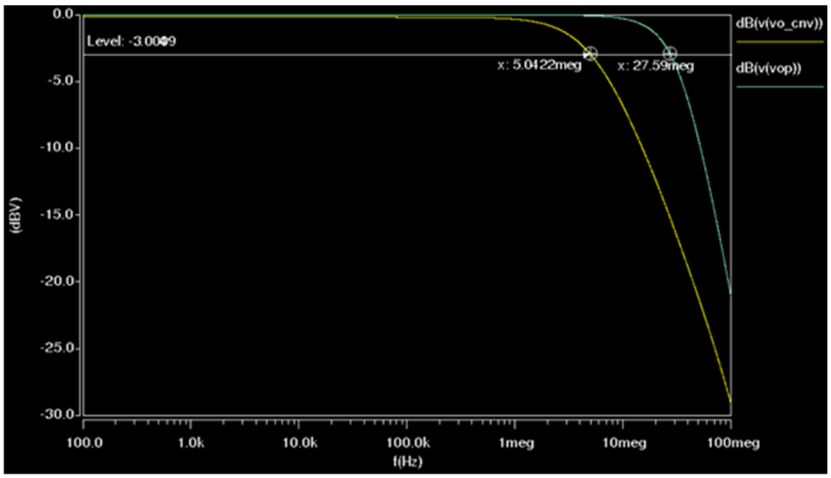

Figure 8. AC voltage-follower responses in 90 nm.

The slew rate (SR) and the peak output current capability were determined by performing transient simulations applying a 5 MHz, 0.4V_{PP} pulse input signal to the op-amps configured as voltage followers. Input and output voltage waveforms (top) as well as the

load capacitor currents (bottom) for 22 nm, 45 nm, 90 nm, and 180 nm technologies are depicted in Figures 10–13.

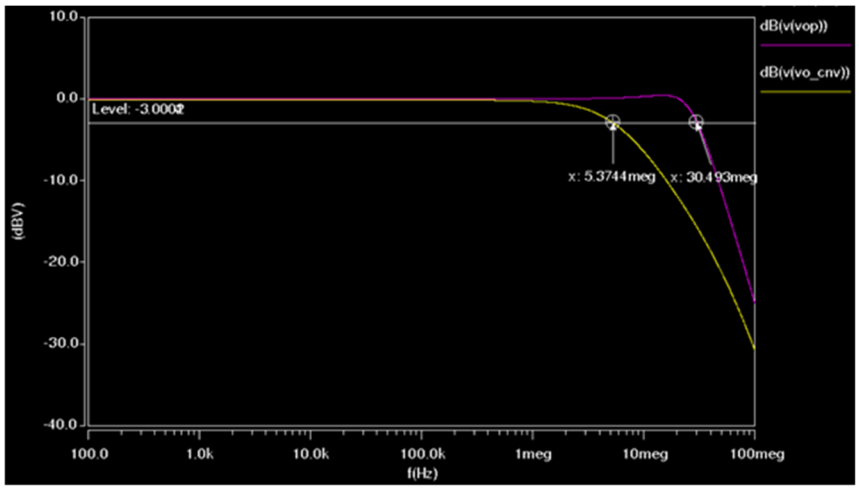

Figure 9. AC voltage-follower responses in 180 nm.

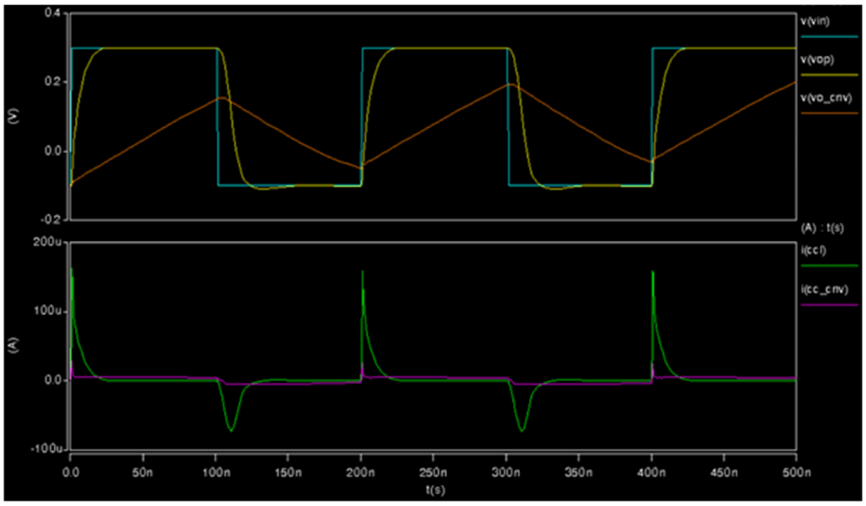

Figure 10. Transient simulation in 22 nm.

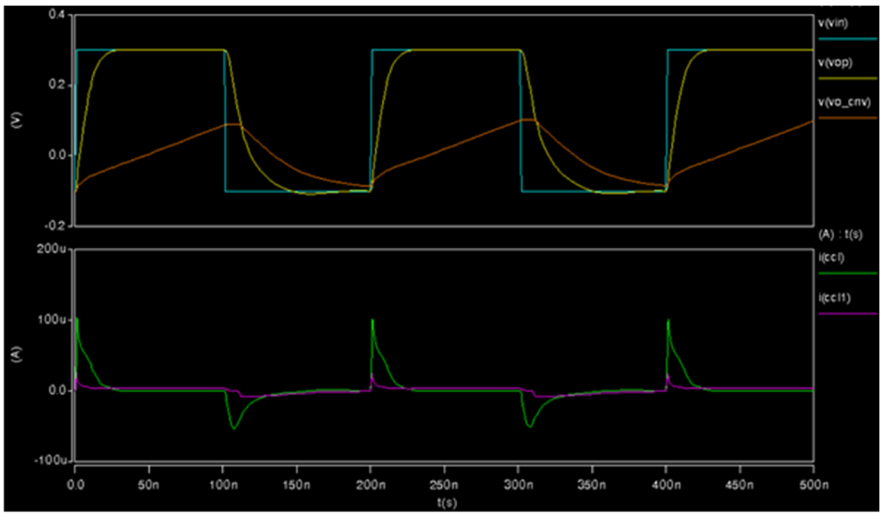

Figure 11. Transient simulation in 45 nm.

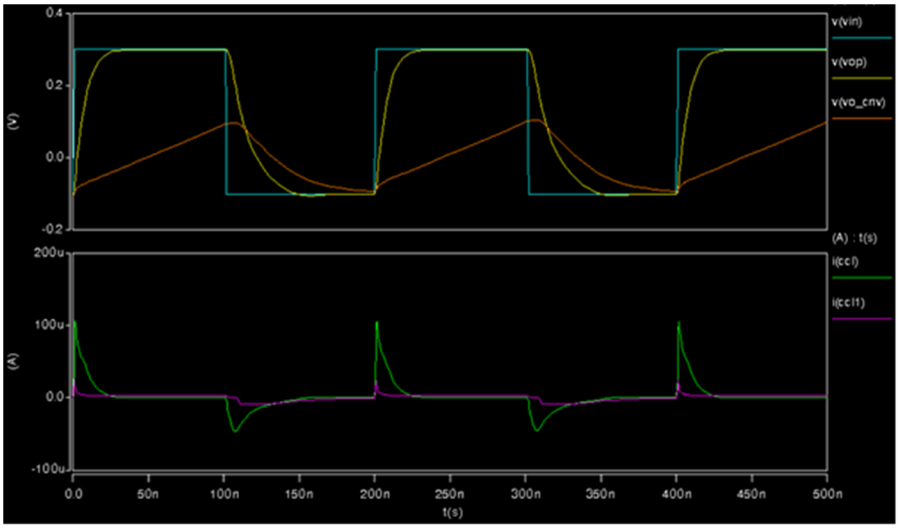

Figure 12. Transient simulation in 90 nm.

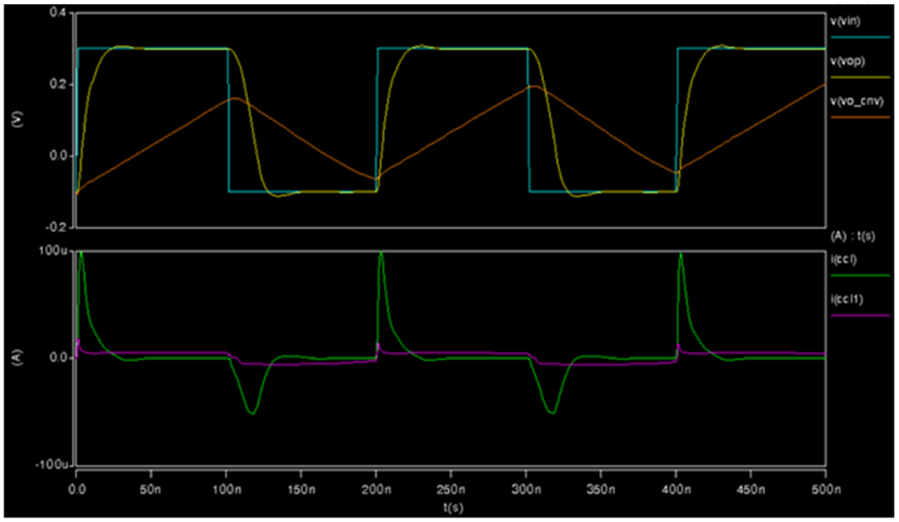

Figure 13. Transient simulation in 180 nm.

It can be seen that in all cases the conventional topology cannot follow the input signal adequately due to SR limitations, the enhanced topology with resistive local common mode feedback brings essentially higher peak output current capability (much higher than the bias current I_B) while the conventional op-amps have positive and negative peak output currents limited by the bias current to a value $I_{outPK} = 2I_B = 5$ μA.

4. Discussion

Table 1 summarizes the performance of the non-cascoded one-stage OTAs with RL-CMFB and of the conventional non-cascoded one-stage OTAs (denoted CNV in the table). GB denotes the Gain-Bandwidth product, $FOM_{SS} = GB \cdot C_L / P_{dis}$ (in MHz·pF/μW units) is the small signal figure of merit where $P_{dis} = I_{totQ} V_{supply}$ denotes static power dissipation (I_{totQ} is the total quiescent current of the OTA), $FOM_{LS} = SR \cdot C_L / P_{dis}$ (in (V/μs)pF/μW units) is the large signal figure of merit and $FOM_{GLB} = (FOM_S \cdot FOM_L)^{1/2}$ is the global figure of merit. The slew rate (SR) used for the calculation of FOM_{LS} is the minimum slew rate SR = min{SR+, SR−} (some authors use the average slew rate to calculate FOM_{LS} instead of the minimum and report higher FOM_{LS} but in practice, the minimum of the two slew rates is what limits the large signal speed of the OTA). The branch bias current I_B of all circuits is $I_B = 2.5$ μA, the total bias current of all circuits is $I_{totQ} = 10$ μA the power dissipation is P_{dis}

= $I_{totQ}(V_{DD}-V_{SS})$, and has values P_{dis} = 4 µW for 22 nm, 4.5 µW for 45 nm and 90 nm and P_{dis} = 9 µW for 180 nm. The following facts are noticeable in Table 1:

(A) The figures of merit in all technologies are a factor higher than 10 in OTAs with RLCMFB.

(B) All figures of merit of OTAs with resistive local common mode feedback increase as the feature size of a CMOS technology decrease. One of the reasons is that supply voltages and static power dissipation also decrease with decreasing feature sizes and the standard figures of merit are inversely proportional to static power dissipation.

(C) The main objective of this paper was to show that, even with relatively low C_L values, it is possible to achieve significant performance enhancement factors (~1000%) using RLCMFB in current CMOS technologies. It might be possible to achieve even larger performance improvement factors by optimizing the OTA design (W/L values, R, Ibias, Rs) for each technology.

Table 1. Summary of simulation results and figures of merit for conventional and one-stage OTAs with resistive local common mode feedback in 22 nm, 45 nm, 90 nm, and 180 nm CMOS technologies.

V_{DD}/V_{SS} (V)	Tech.	Topology	A_{ol} (dB)	PM (°)	GB/fz/fpab (MHz)	SR_+ (V/µs)	SR_- (V/µs)	$I_O{}^+{}_{peak}$ (µA)	$I_O{}^-{}_{peak}$ (µA)	R_s (kΩ)	$FOM_{SS/LS/GLB}$
±0.4	22	RLCMFB	46.7	61	30.4/39.8/53	66	−36.4	159.2	−73	2	15.2/18/16.5
		CNV	25.3	91	4.3	2	−2.2	5	−5.5	0	1/0.55/0.75
±0.45	45	RLCMFB	63.7	58	31.7/31.8/47	43.1	−22	101.8	−51	2.5	14.2/9.8/11.8
		CNV	50.7	88	4.5	2.4	−2.2	5	−5	0	1/0.55/0.74
±0.45	90	RLCMFB	60.8	68	38.4/26.5/54.9	42.1	−22.3	105.4	−45.7	3	17/9.8/12.9
		CNV	32.9	89	4.8	2.4	−2	5	−5	0	1/0.44/0.66
±0.9	180	RLCMFB	58.3	53	29/26.5/20.4	43.8	−24.9	99.3	−52.1	3	6.5/5.6/6
		CNV	34.3	87	5 M	2.2	−2.1	5	−5	0	0.55/0.24/0.36

Table 2 shows a comparison of the performance of the OTAs with RLCMFB to OTAs published recently in the literature [13–18]. It can be seen that even without optimizing the designs, in all cases the FOMs of the RLCMFB OTAs are much higher than those in [13–18].

Table 2. Comparison of RLCMFB-OTAs to recent published OTAs.

Parameters	[13] 2017	[14] 2019	[15] 2019	[16] 2020	[17] 2020	[18] 2021	This Work	This Work	This Work	This Work
CMOS process (nm)	180	180	180	180	180	180	180	90	45	22
Vsupply (V)	0.5	1.2	1.8	1.8	1.8	1.8	1.8	0.9	0.9	0.8
ItotQ (µA)	7.9	700	530	260	-	400	10	10	10	10
C_L (pF)	1	10	5	5.6	8	18	2	2	2	2
Aol (dB)	50	75	105.5	90.1	68	73.4	58.3	60.8	63.7	46.7
GB (MHz)	16.6	185	231.7	157	172.5	224	29	38.4	31.7	30.4
PM (degree)	72	71	53	62.1	48.7	69	61	56	68	53
SR+/SR− (V/µs)	4.25	99	13.2	64	212	110	44/25	42/22	43/22	66/36
FOM_{SS} (MHz pF/µW)	4.2	2.2	1.21	1.87	1.21	5.6	6.5	17	14.2	15.2
FOM_{LS} ((V/µs)pF/µW)	1.076	1.17	0.007	0.76	0.34	2.75	5.6	9.8	9.8	18
$FOM_{GLB} = (FOM_{LS}FOM_{SS})^{1/2}$	2.12	1.61	0.09	1.19	0.64	4	6	12.9	11.8	16.5

5. Conclusions

A comparative study of the performance of non-cascoded one-stage OTAs demonstrated that the inclusion of resistive common mode feedback is especially appropriate to increase significantly the OTA performance in current CMOS technologies. It is a very

simple technique that improves A_{ol}, GB, and SR and figures of merit by factors greater than 10 (or >1000%) without additional power dissipation or increased supply requirement and with very small additional silicon area and circuit complexity.

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