Research Article

Simulation and analysis of three-phase parallel inverter using multicarrier PWM control schemes

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Abstract
Simulation and analysis of three-phase parallel inverter using multicarrier pulse width modulation such as phase disposition (PD), phase opposition disposition (POD) and alternate phase alternate disposition (APOD) are presented in this article. In this proposed work, reduced active switching count, transformers, single DC input, a high degree of modularity and redundancy are key merits and also suitable for renewable energy systems. The proposed three-phase five-level multilevel inverter with single DC source using a three-phase transformer is controlled by multicarrier pulse width modulation schemes. To generate switching pulses for five-level inverter, four carrier signals can be compared with a reference signal. The performance of the inverter is examined by using PD, POD, and APOD by modulation index (MI) starting from 0.4 to 1. Furthermore, the over-modulation region is also analyzed in this paper. The effectiveness of the system is analyzed in terms of total harmonic distortion by varying the MI of the inverter. The simulation results are verified through MATLAB/Simulink.

Keywords Three-phase MLI · Reduced switch count · MC-PWM · THD

1 Introduction

In recent years, the various multilevel inverter topologies have been utilized for the power conversion purpose. But, development of the multilevel inverter topologies is growing for high power and high voltage applications especially renewable energy applications. Out of the various renewable energy sources, solar PV energy is highly preferable for electrical power generation [1]. The different types of MLIs topologies have been used for the conversion of renewable energy power into the AC power [2, 3]. MLIs topologies are offered the highest conversion efficiency, lower THD, lower electromagnetic interference and lower passive filtering requirements. Furthermore, it is possible to modify new topologies with a reduced number of components [4]. There are three kinds of MLI topologies (1) diode clamped (2) flying capacitor and (3) cascaded H-bridge inverter [5]. The many authors have been investigated cascaded H-bridge inverters for grid-connected applications. Three-phase two-level inverter is the most commonly used structure for renewable energy systems applications [6]. But it has some own drawbacks, limitation of voltage level, passive filtering requirement, and THD. To eliminate the drawbacks of the three-phase two-level inverter, three-phase inverter topology can be formed by using the six, single-phase two-level inverter that has been proposed [7]. The interesting fact in this topology is that there is no necessity for a transformer in the inverter module, but to feed power to the grid it requires a transformer owing to the common-mode current. It uses only one DC source and several single-phase transformers are connected in series at the output side. Furthermore, a three-phase inverter is presented along with a low frequency transformer [8, 9]. It is the all-encompassing variant of the

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inverters created by [8, 9]. This proposed topology is an extended version of the paper [10]. A three-phase inverter is presented by space vector PWM in [11]. A three-phase four-wire system is developed for grid application in [12]. Recently, the three-phase inverter has been introduced for PV applications [13, 14]. To solve the aforementioned problems, a new three-phase inverter has been developed in this paper, in which three-phase voltages were obtained from a single DC-link and it is possible only, secondary terminals of the transformer are star connection. Furthermore, higher-order harmonics are decreased with the help of the transformer which is highly adaptable for utility applications and isolation between input and output are remarkable benefits. Many authors have been investigated by various carrier-based PWM techniques [15, 16]. In this article, the three-phase parallel inverter can be controlled by MC-PWM (APOD, POD, and PD). The inverter performance can be evaluated in terms of THD.

2 Proposed systems

The block diagram of the proposed system is shown in Fig. 1. The proposed inverter circuit includes three single-phase five-level inverters. An individual single-phase inverter produces a five-level output voltage from a common DC-link voltage. A single-phase inverter is formed by connecting auxiliary inverter along with an H-bridge inverter. An auxiliary inverter is constructed by single IGBT along with four power diodes. In this three-phase inverter, H-bridge inverter consists of four IGBTs and out of these, S_{a3} and S_{a4} are operated at a rate of the fundamental frequency. The switches S_{a1}, S_{a2}, and S_{a5} in the auxiliary circuit are operated at the rate of the carrier frequency.

It is observed from Fig. 2, phase-A is comprised of normal H-bridge inverter (S_{a1}–S_{a4}) along with auxiliary an inverter (S_{a5}). Similarly, phase-B is comprised of S_{b1}–S_{b4} and S_{b5} and phase-C is comprised of S_{c1}–S_{c4} and S_{c5}. Each single-phase inverter is generated 325 V from the DC link when gating pulses are applied from the control circuit. The voltage of the DC link is supposed to be greater than the inverter output voltage ($>\sqrt{2}\times V_o$). Failing to meet this condition, an inverter is unable to guarantee the power flow to the load. Three single-phase five-level inverters are given to the 12 terminal of the three-phase transformer, and the neutral points are shorted. The key merits are that

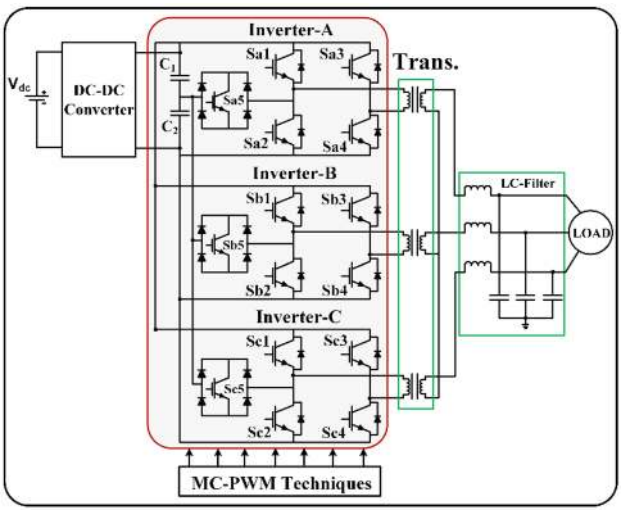
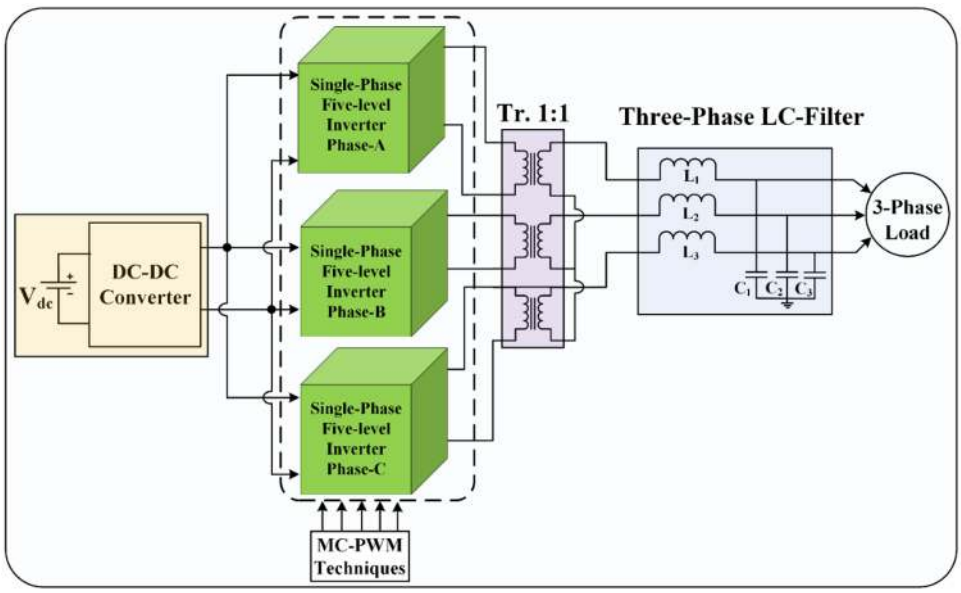


Fig. 2 Proposed power circuit

Fig. 1 Block diagram of the proposed system



it obtains a higher output voltage with a reduced number of active devices, transformer, DC input source, and simplified control circuits. They are operated in five states and corresponding voltage states are as follows: When the output voltage is equal to zero, S_{a5} is completely OFF and others are in either ON or OFF the switching table and other four modes of operation are shown in Fig. 3.

Switches S_a1, S_a2, and S_a5 operate at 20 kHz of switching frequency, and one leg of the H-bridge inverter (S_{a3} and S_{a4}) operates in the 50 Hz frequency. The proposed inverter generates a five-level output voltage from the common DC-link voltage. The fault detection and replacement of faulty devices are very easy in this inverter. Actually a generic phase-leg can be decomposed into S_{a3} switch cell and S_{a4} switch cell depending on the load current directions. There is no question that dead-time is not required for either a S_{a3} switch cell or an S_{a4} switch cell because both switch cells are configured with a controllable switch in series with an uncontrollable diode [21].

3 Multicarrier-based PWM techniques

The PWM control technique is the most effective control scheme for controlling the three-phase inverter. In this proposed method, carrier-based PWM schemes are used such as PD, POD, and APOD have been applied. These are also called constant frequency techniques; generation switching pulses for an N level inverter, an $N-1$ carrier is required. An amplitude modulation index (MI) and frequency modulation for a multilevel inverter are as follows

$$M_{inv} = \frac{A_m}{(m-1)A_c} \tag{1}$$

$$F_{inv} = \frac{f_c}{f_m} \tag{2}$$

where A_m and A_c are the peak amplitude of modulation and carrier signal, respectively.

The frequency of the carrier and modulating signals are termed as f_c and f_m, respectively. The realization of switching logic to the inverter is implemented by using logic gates. The generalized switching logic diagram is shown in Fig. 4. The reference and carrier arrangement for PD, POD, and APOD are shown in Figs. 5, 6 and 7 [20].

In the APOD technique, each carrier is phase-shifted by 180° from its adjacent carrier. In the POD technique, two carriers waves are arranged above the zero reference and other two carrier waves are arranged below the zero reference. Above the zero reference, carrier waves are in phase

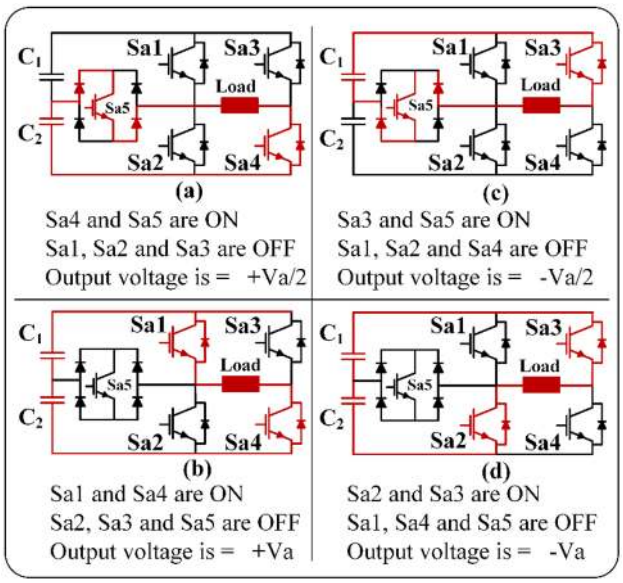


Fig. 3 Modes of operation and voltage levels

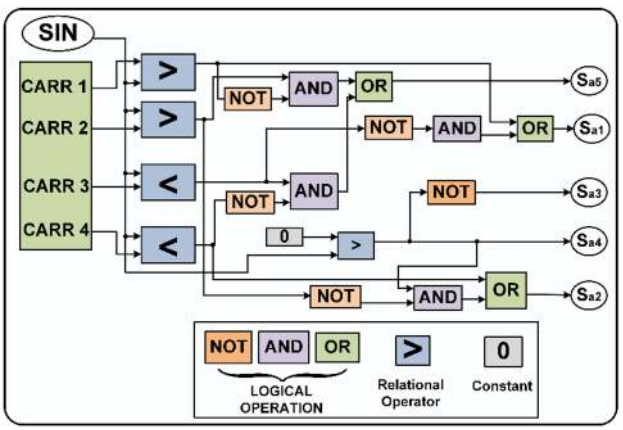


Fig. 4 Switching pattern realization using logic gates

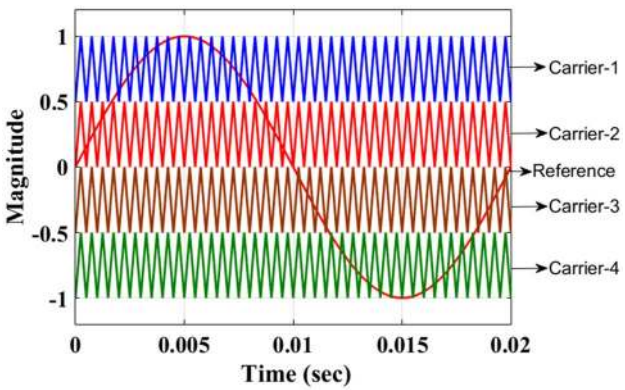


Fig. 5 Reference and carrier arrangement for PD

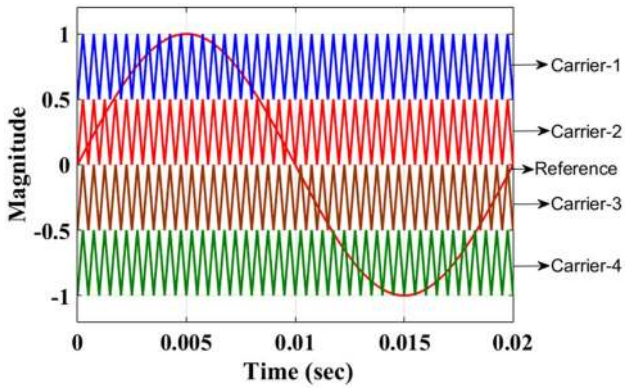


Fig. 6 Reference and carrier arrangement for POD

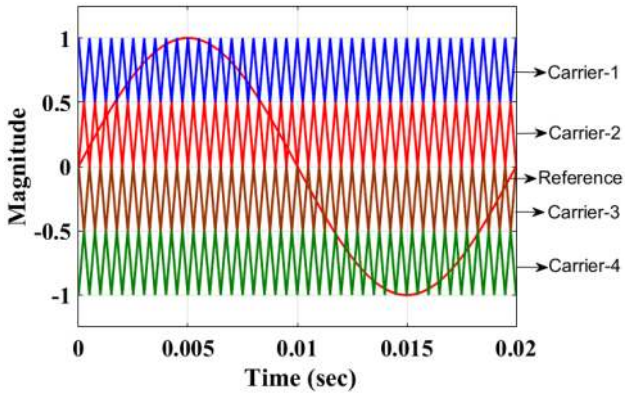


Fig. 7 Reference and carrier arrangement for APOD

with each other and below the zero reference, carrier waves maintain 180° phase shift (opposite) with the above the zero reference carrier waves. In the PD techniques, all carrier waves are in phase with each other. The switching pulses to the inverter switches are shown in Fig. 8.

4 Simulation results and discussion

The simulation of proposed PWM controlled three-phase inverter is carried out by using MATLAB/Simulink, and obtained simulation results are discussed. The inductor and capacitor values for the filter are 1 mH and 2 μF. The simulation parameters used in the proposed system are shown in Table 1.

4.1 Phase disposition (PD)

In this phase disposition technique, the four carrier signals are compared to the reference signal. These four carrier

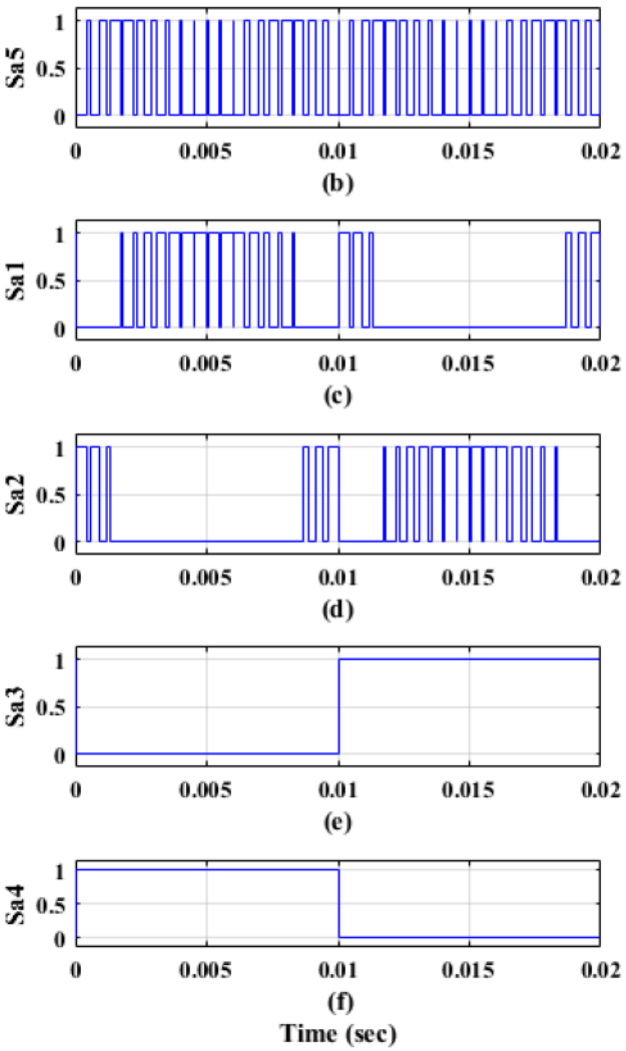


Fig. 8 Switching pulses

Table 1 Simulation parameter values

Parameters	Specifications
Inverter input voltage	340 V
Inverter output voltage per phase (RMS)	231 V
Output current (RMS)	1.44 A
Output power	997.92 W
Fundamental frequency	50 Hz
Switching frequency	20 kHz
Inductance	1e−3H
Capacitance	2e−6F
Resistive load	1000 Ω
Transformer primary and secondary voltages	400 V
Transformer rating	3 KVA

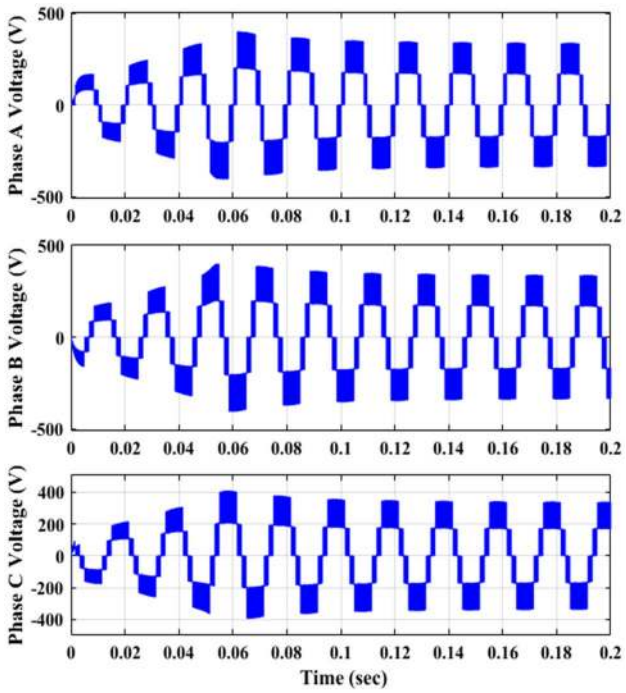


Fig. 9 Five-level waveforms of PD

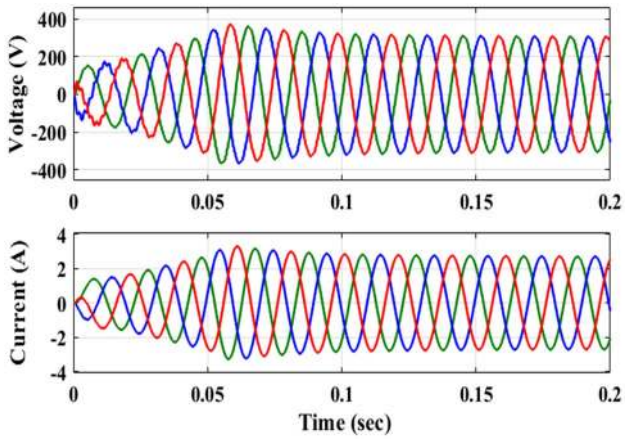


Fig. 10 Three-phase voltage and current waveforms

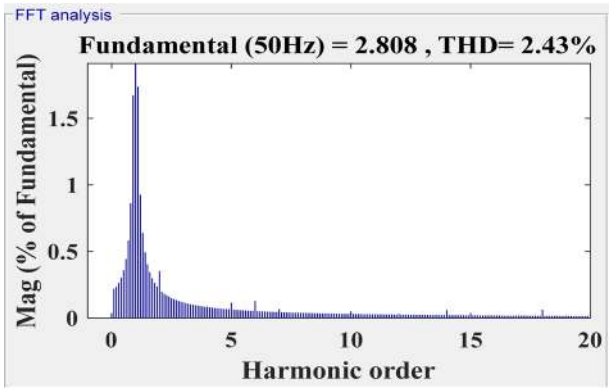


Fig. 11 THD at MI = 1

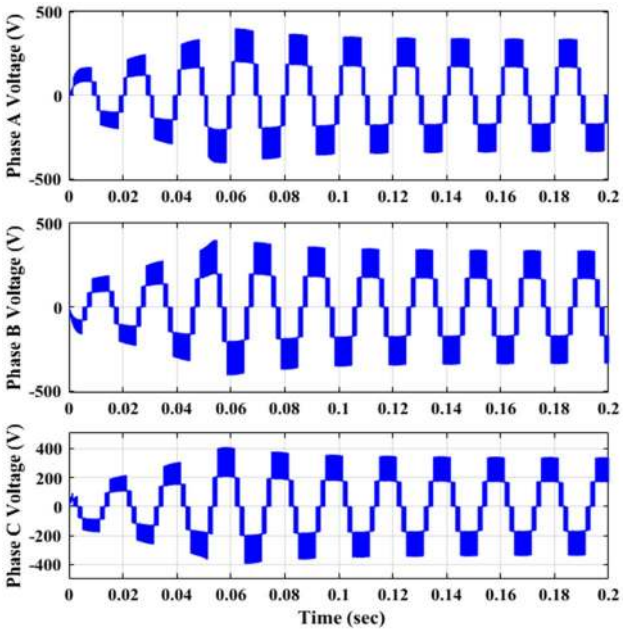


Fig. 12 Waveforms of POD (five levels)

signals are having equal amplitudes and in phase each other.

To generate appropriate pulses to the inverter, four carrier signals are compared with a sinusoidal carrier signal (50 Hz) and it is shown in Fig. 5, and the switching pattern is also given in Fig. 8; the *y*-axis is an amplitude in volts, and the *x*-axis is time in seconds. Simulation results of five-level output voltages are depicted in Fig. 9. The three-phase output voltage, current and THD profile are depicted in Figs. 10 and 11, respectively. The THD generated by the inverter is about 2.43% at MI equal to 1 using PD-PWM techniques.

4.2 Phase opposition disposition (POD)

In the POD technique, two carriers waves are arranged above the zero reference and other two carrier waves are arranged below the zero reference. Above the zero reference, carrier waves are in phase with each other and below the zero reference, carrier waves maintain 180° phase shift (opposite) with the above the zero reference carrier waves. All carrier signals are maintained equal amplitude and frequency, but the difference in phase shift is shown in Fig. 6;

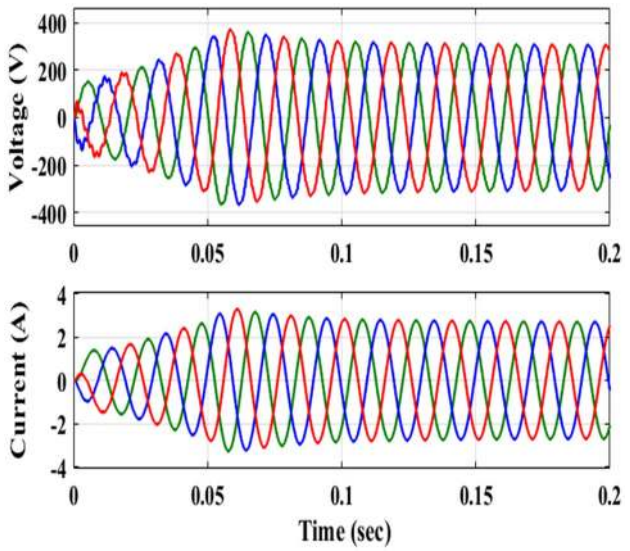


Fig. 13 Three-phase voltage and current waveforms of POD

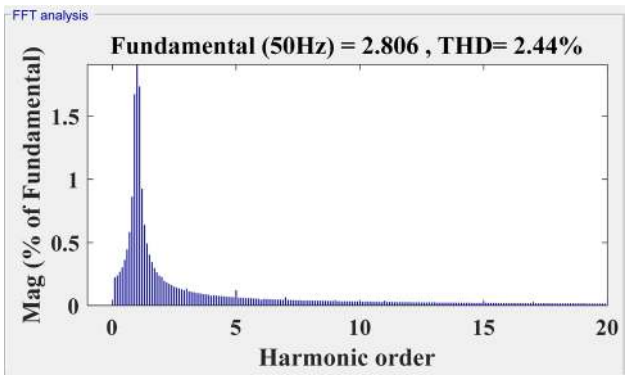


Fig. 14 THD at MI = 1

the *y*-axis is an amplitude in volts, and the *x*-axis is time in seconds.

Simulation results of five-level output voltages are depicted in Fig. 12. The three-phase output voltage, current and THD profile are depicted in Figs. 13 and 14, respectively. The THD generated by the inverter is about 2.44% at MI equal to 1 using POD-PWM techniques.

4.3 Alternate phase opposition disposition (APOD)

In this APOD technique, all the carrier signals are phase-shifted by 180° from the adjacent carriers. In APOD PWM, zero references are placed in the middle of the carriers.

Above the zero references, carriers are positive carriers and below the zero references are negative carriers. In this, all carriers are maintaining 180° shifted with each other and it is shown in Fig. 7; the *y*-axis is an amplitude in volts, and the *x*-axis is time in seconds.

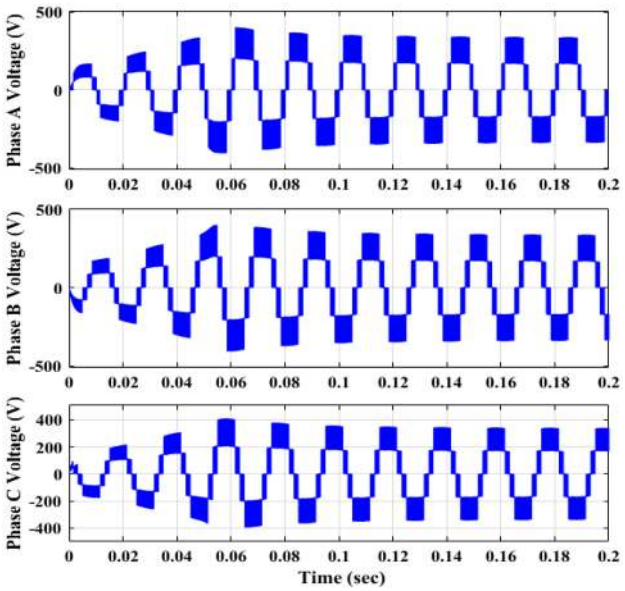


Fig. 15 Five-level waveforms of APOD

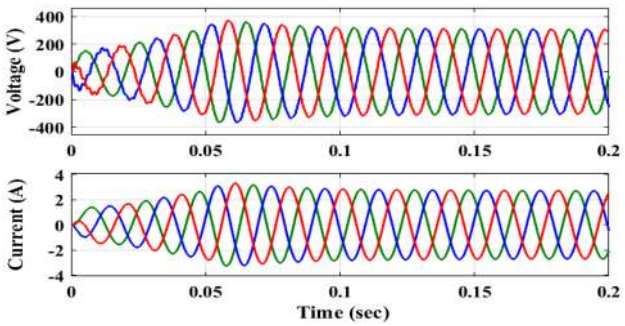


Fig. 16 Three-phase voltage and current waveforms of APOD

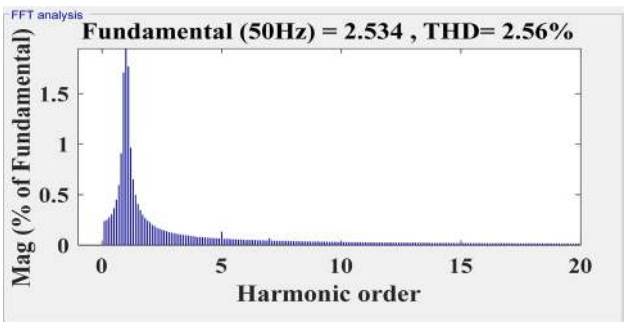


Fig. 17 THD at MI-1

Simulation results of five-level output voltages are depicted in Fig. 15. The three-phase output voltage, current and THD profile are depicted in Figs. 16 and 17,

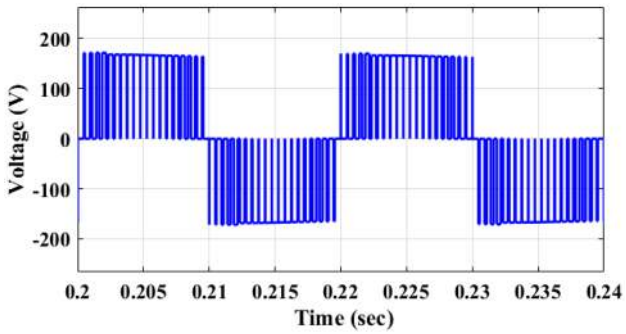


Fig. 18 Inverter output voltage at MI-0.5

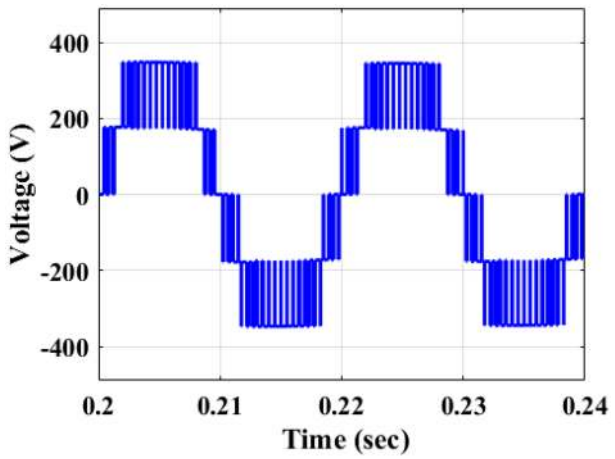


Fig. 19 Inverter output voltage at MI-0.9

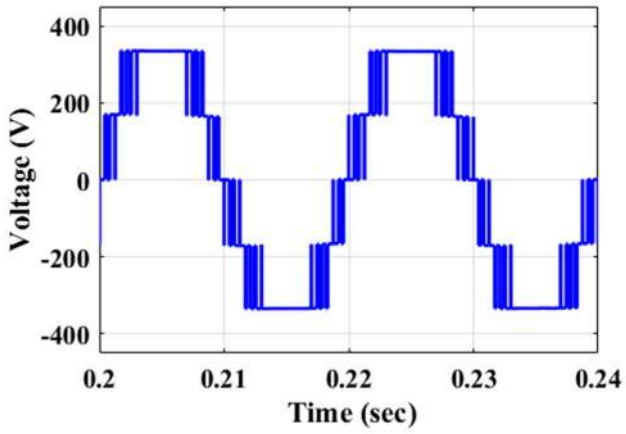


Fig. 20 Inverter output voltage at MI-1.2

respectively. The THD generated by the inverter is about 2.56% at MI = 1 using APOD-PWM techniques. Figures 18, 19 and 20 show the inverter output voltage with an MI of 0.5, 0.9 and 1.2, respectively.

Table 2 Device and components comparison

Device and components	References			Proposed
	[18]	[5]	[19]	
DC bus capacitors	06	01	03	03
Diodes	–	–	–	12
Input DC source	06	01	03	01
Transformers	–	06	01	01
Active switches	24	24	18	15
No. of levels	05	07	05	05

The different components are used in the three-phase inverter, and it is tabulated in Table 2. In [18], the five-level inverter has been proposed by the authors. In this topology, six input DC sources and 24 switches are used. Similarly, components are utilized in [5, 19]. The proposed inverter uses only 15 switches, single DC input, and three-phase transformer.

5 Interpretation of simulation results

In this section, interpretation of simulation results of PD-PWM, POD-PWM and APOD-PWM techniques is presented in Tables 3, 4 and 5, respectively. The carrier-based PWM (PD, POD, and APOD) techniques have been applied to examine the performance of the inverter with different modulation index. In this, a star-connected resistive (1000Ω) load is considered, so phase voltage, line voltage, and current values are taken in Tables 3, 4 and 5 with different MC-PWM techniques. From Table 3, the percentage of voltage and current THD is obtained from the various modulation indexes starting from 40 to 100%. Percentages of THDs are obtained from inverter without a filter. 15.74% is obtained from the inverter for the modulation index 1 (one), whereas 38.59% of THD is obtained at 0.4. From Table 4, the percentage of voltage and current THD is obtained from the various modulation indexes starting from 40 to 100%. Percentages of THDs are obtained from inverter without a filter. 19.87% is obtained from the inverter for the modulation index 1 (one), whereas 61.81% of THD is obtained at 0.4. From Table 5, the percentage of voltage and current THD is obtained from the various modulation indexes starting from 40 to 100%. Percentages of THDs are obtained from inverter without a filter. 23.42% is obtained from the inverter for the modulation index 1 (one), whereas 61.81% of THD is obtained at 0.4. From the simulation results, harmonic content developed by the inverter is a minimum of 15.74% compared to the other PWM techniques. Hence, it is concluded PD-PWM techniques significantly improve the performances of the inverter compared to the others and current THD is also

Table 3 Simulation results summary of PD

MI	V_{Ph}		V_L		I_L (% THD)	
	Voltage	% THD	Voltage	% THD	Current	% THD
1	215.3	15.74	372.9	15.72	1.876	2.43
0.9	194.9	16	337.5	16	1.697	2.46
0.8	175	20.2	303.1	20	1.514	2.65
0.5	114.3	32.62	198	32.61	0.959	3.86
0.4	94.96	38.59	164.5	38.56	0.781	3.14

Table 4 Simulation results summary—POD

MI	V_{Ph}		V_L		I_L (% THD)	
	Voltage	% THD	Voltage	% THD	Current	% THD
1	216.8	19.87	375.5	19.87	1.875	2.44
0.9	199.6	27.46	345.8	27.53	1.697	2.57
0.8	180.7	32.71	312.9	32.80	1.514	2.79
0.5	115.9	36.84	200.7	36.89	0.959	3.88
0.4	104.1	61.81	180.4	61.82	0.781	3.56

Table 5 Simulation results summary—APOD

MI	V_{Ph}		V_L		I_L (% THD)	
	Voltage	% THD	Voltage	% THD	Current	% THD
1	218.5	23.42	378.4	23.44	1.876	2.48
0.9	199	26.27	344.7	26.35	1.697	2.56
0.8	177.9	27.27	308.2	27.30	1.514	2.71
0.5	115.9	36.84	200.7	36.89	0.959	3.88
0.4	104.1	61.81	180.4	61.82	0.781	3.56

within the recommended standard of IEEE. Compared to the existing topologies, the proposed three-phase five-level inverter has been developed with 15 active switches and only one three-phase transformer along with the single DC (SDC) source. The proposed inverter generates a five-level output voltage. Therefore, lower THD profile and lesser passive filtering requirement and higher reliability can be attained since each phase is acting independently. Hence, fault identification and rectification are very easy.

Figure 21 shows the percentage of voltage and current THD with different modulation index (from Tables 3, 4, 5).

Table 6 represents the comparison of THD with the proposed system and the existing system. The proposed system produced 2.43% of THD so as compared to other systems the proposed system produces less THD. Similarly. Figure 22 represents the bar chart of THD proposed system and existing system.

5.1 Future work

The future work of this research work is to implement experimental setup for grid-connected applications by using field programmable gate array (FPGA) to verify the simulation results and inverter performance.

6 Conclusion

The MC-PWM control based modified three-phase inverter with minimized switch count using SDC input has been presented in this paper. MC-PWM technique has been used to obtain switching pulses for the inverter switches for the proposed inverter. The switching pulses, $(N-1)$ carrier signals were compared with a single reference signal. Finally, THD comparison has been carried out for simulation results of the proposed system with a different modulation index from 40 to 100%. Finally, the device and the utilization of the components of an inverter were also investigated with existing research findings. The results of the proposed inverter have been analyzed using MATLAB/Simulink.

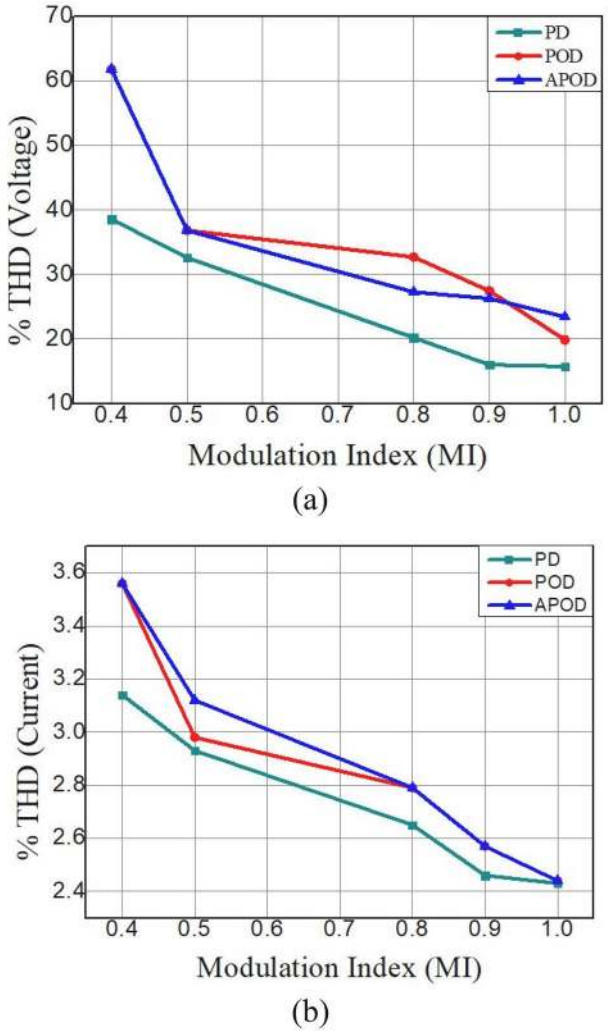


Fig. 21 Inverter THD, **a** voltage, **b** current

Table 6 THD comparison

References	% THD	PWM technique
[1]	5.46	MC-PWM
[2]	5.69	MC-PWM
[8]	3.39	PS-PWM
[17]	7.25	PWM
[18]	4.16	SPWM
Proposed	2.43	MC-PWM

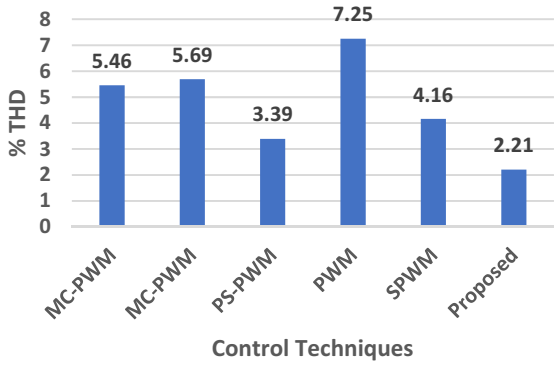


Fig. 22 Bar charts of % THD with the proposed system and existing system

Compliance with ethical standards

Conflict of interest The authors declare that there is no conflict of interest.

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